Fermi National Accelerator Laboratory

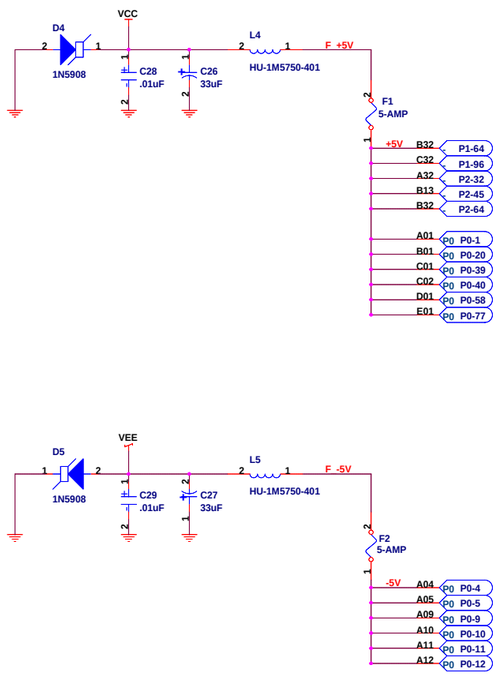
SVX II Silicon Strip Detector Upgrade Project Readout Electronics

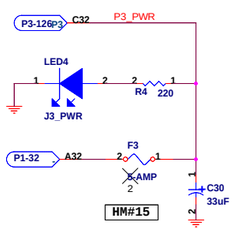
Electrical Schematic of the FIB SUBRACK FANOUT MODULE (FFO) Revision B

November 15, 1999

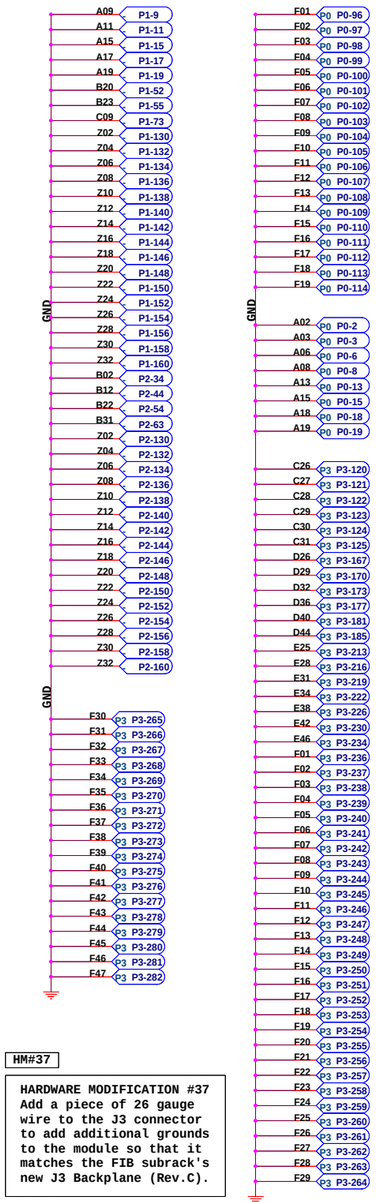
John Anderson, Kerry Woodbury, John Chramowicz, Stefano Rapisarda

Document # ESE-SVX-990909



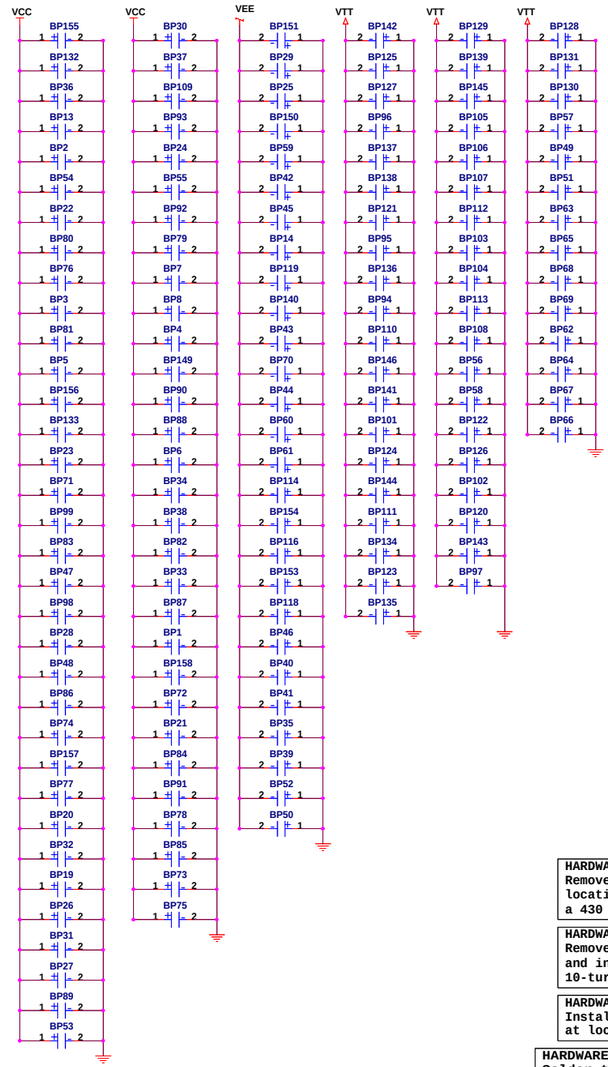


HARDWARE MODIFICATION #15
Remove the fuse at location F3 (J3 Power) and replace it with a 2-Amp fuse. Carefully scratch the "5" off the silkscreen under the fuse.



HM#37

HARDWARE MODIFICATION #37
Add a piece of 26 gauge wire to the J3 connector to add additional grounds to the module so that it matches the FIB subrack's new J3 Backplane (Rev.C).



HARDWARE MODIFICATION #19
Remove resistor at location R42 and install a 430 Ohm resistor.

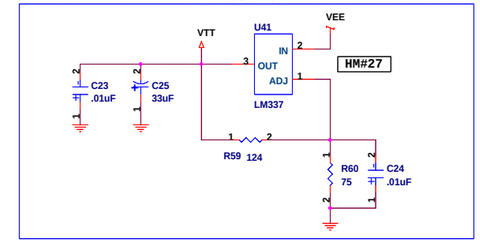
HARDWARE MODIFICATION #20
Remove potentiometer R44 and install a 10 Ohm 10-turn potentiometer.

HARDWARE MODIFICATION #21
Install a 75 Ohm resistor at location R43.

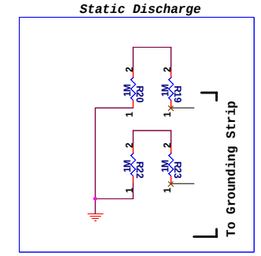
HARDWARE MODIFICATION #27
Solder the tabs of the 2 voltage regulators (U23, U41) to the copper area under them on the circuit board.

HARDWARE MODIFICATION #29
Adjust R44 so that VBB is equal to -1.28 Volts.

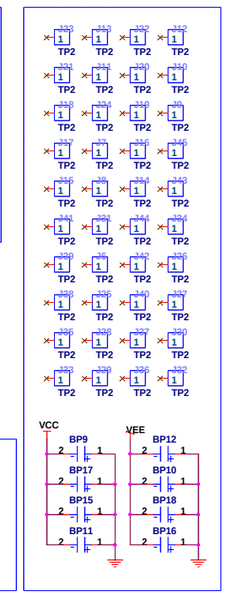
-2V REGULATOR



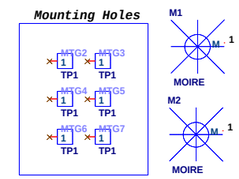
Static Discharge

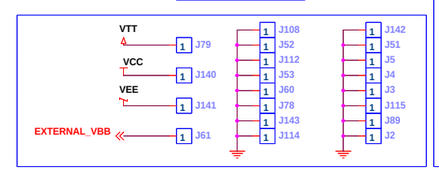


Kludge Area

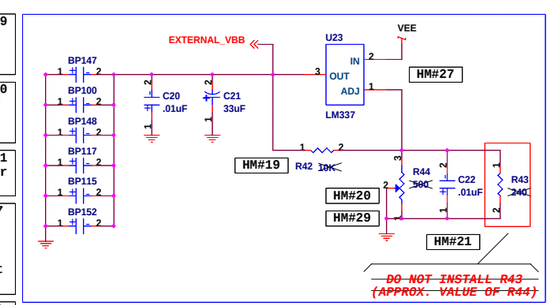


Mounting Holes



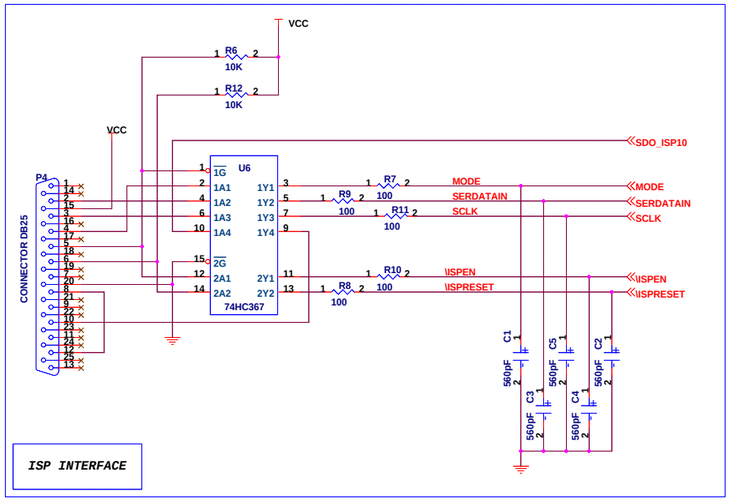


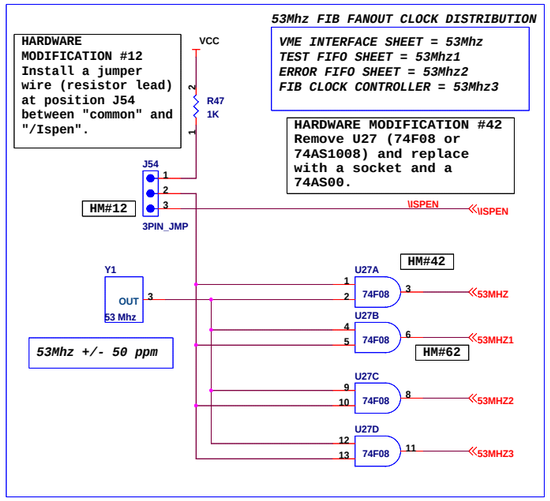
Supply Voltage Test Points

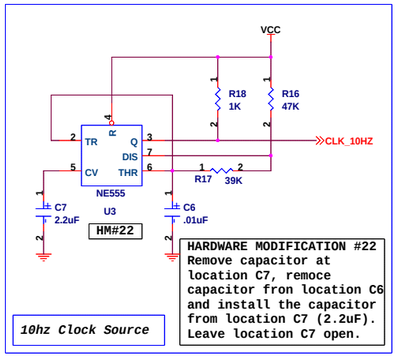


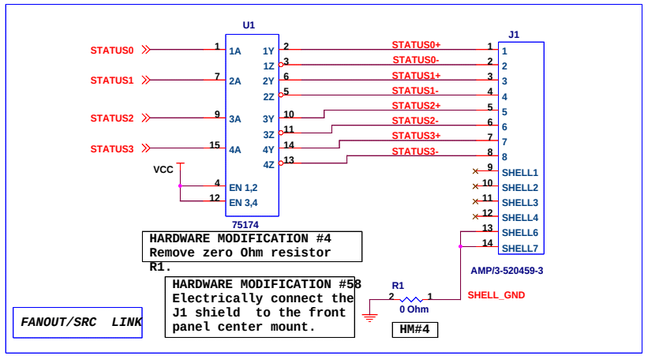
"EXTERNAL VBB" REGULATOR

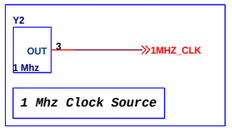
Title	FERMILAB / CD/ESE Fib Fanout Power, Ground, & Bus Signals
Size D	Document Number
Rev B	
Date: Tuesday, October 17, 1999	Sheet 1 of 9





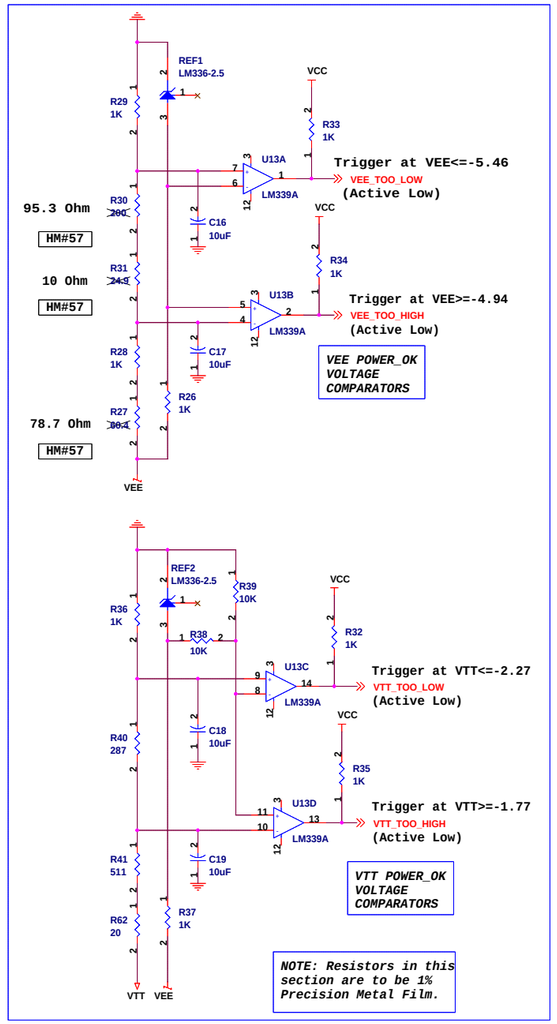


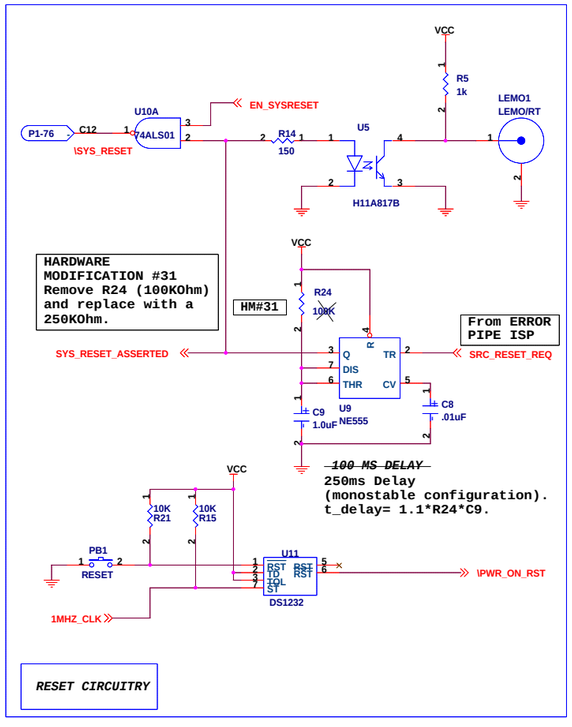


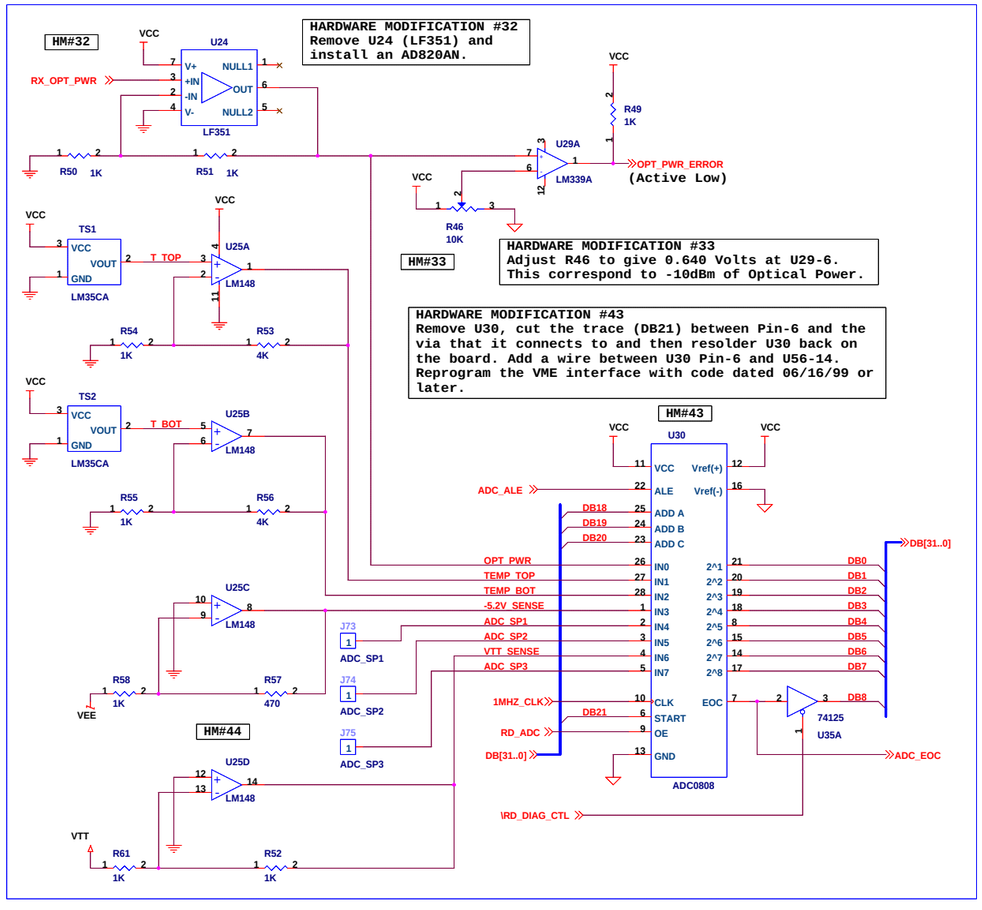


HARDWARE MODIFICATION #57
R27, R30 and R31 need to be changed to get the correct VEE error trigger levels.

HARDWARE MODIFICATION #62
Lift U27-6, cut the pin. Connect a wire from the pad U27-6 to test point J55 (it goes to U28-7).

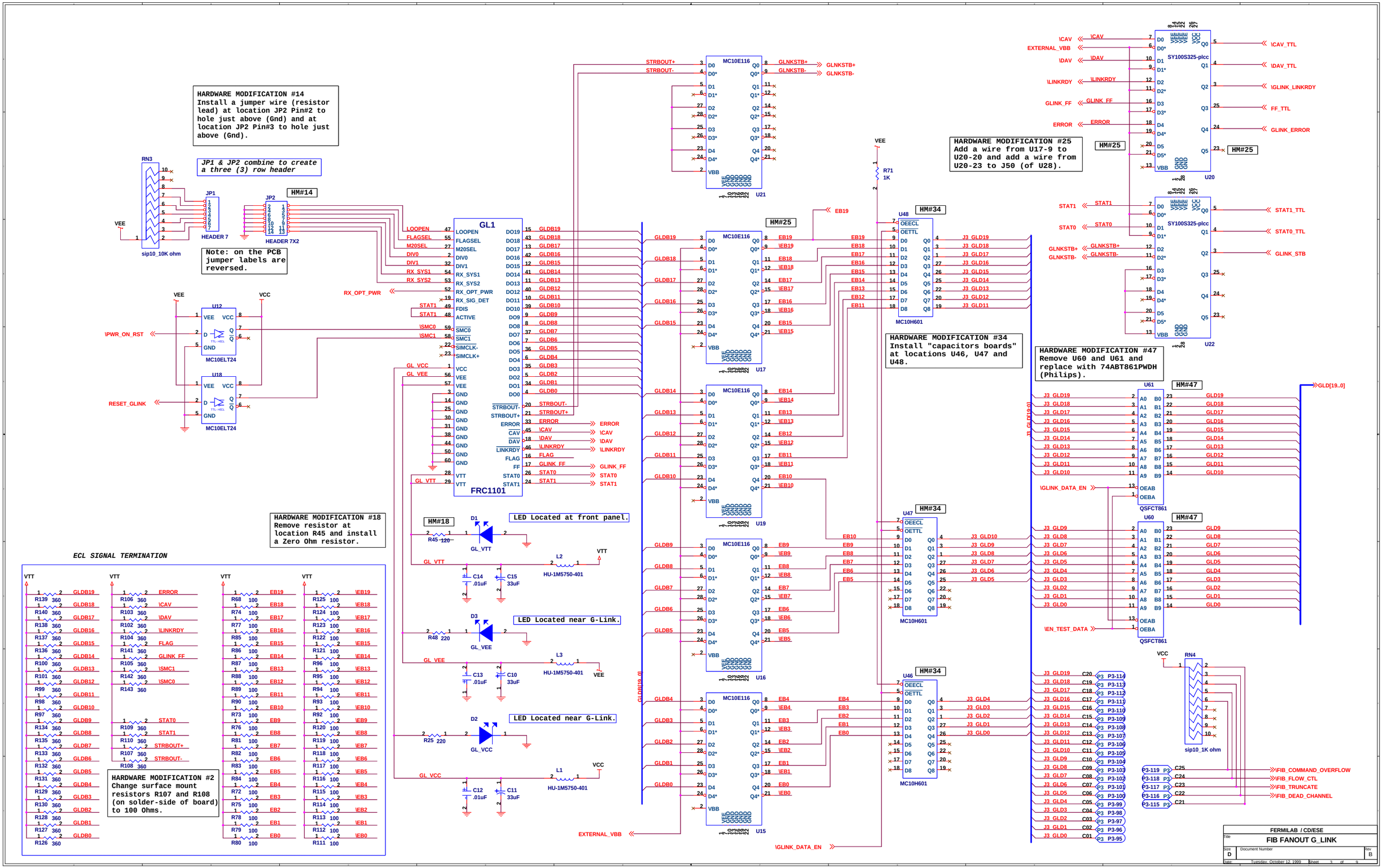


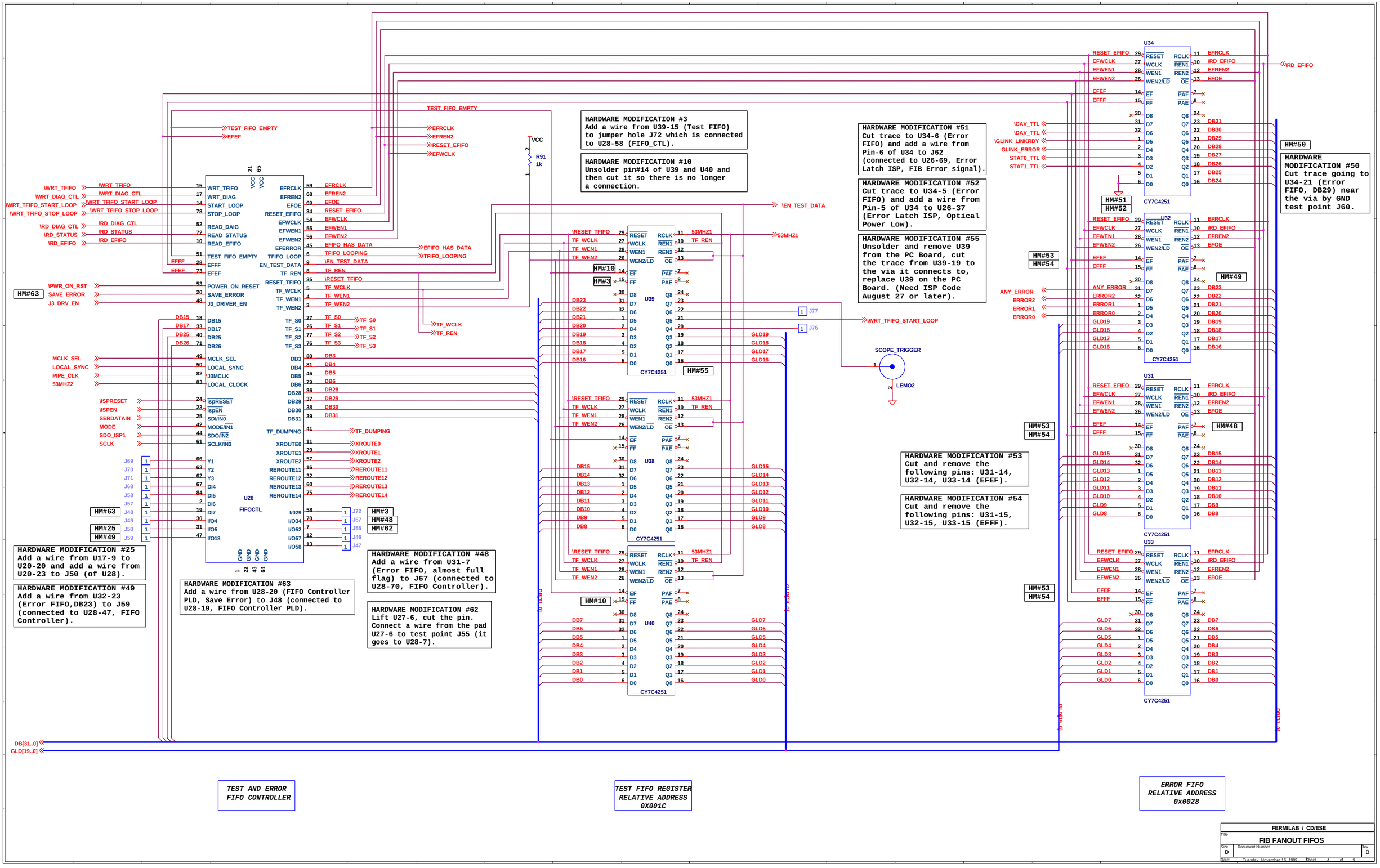


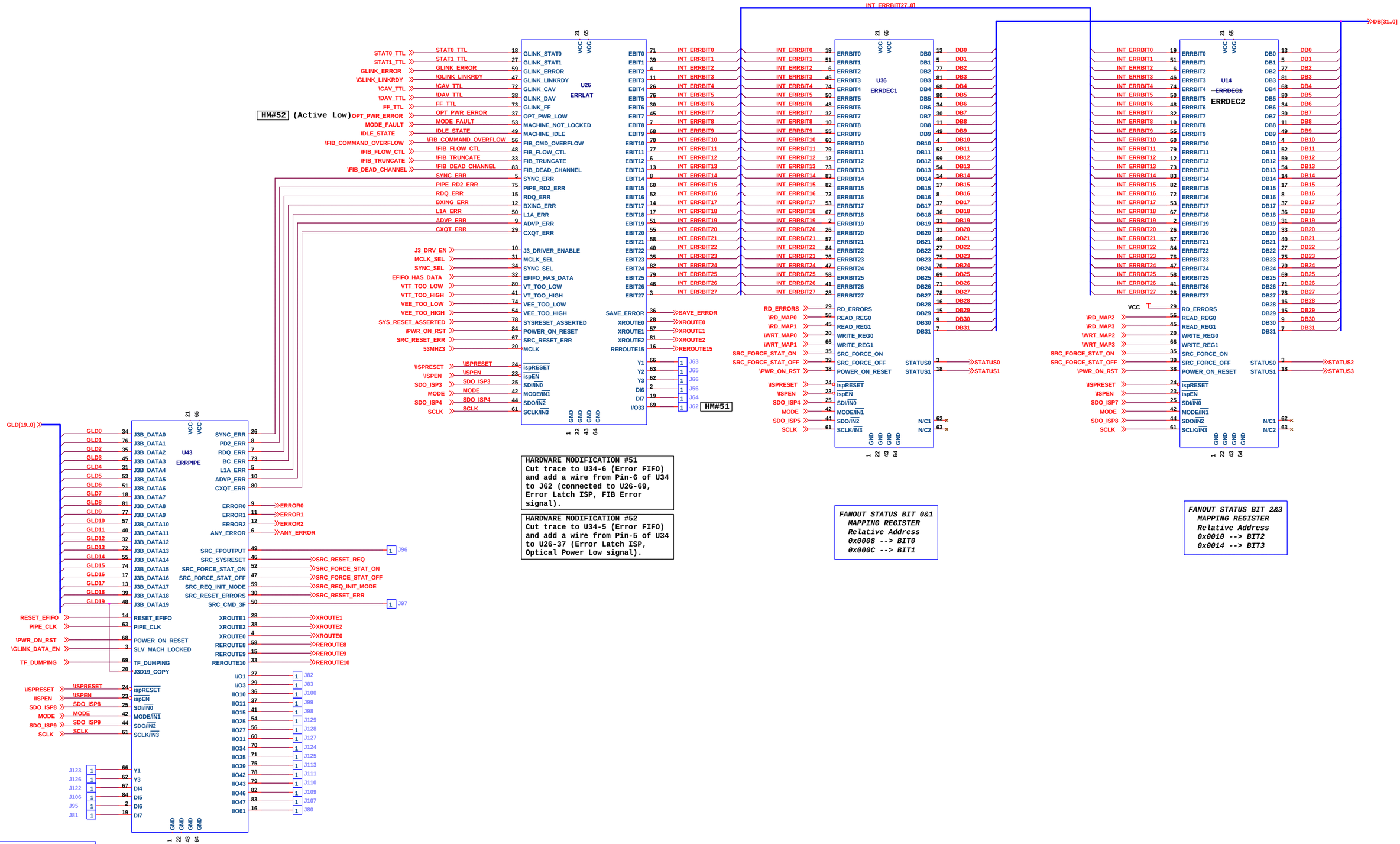


A -5.2V input to the -5.2V sense circuit will produce a +2.4V input to the ADC, providing steps of approximately 10mV at the output of the ADC.

FERMILAB / CD/ESE		
Title: FIB FANOUT MISC		
Size: D	Document Number	Rev: B
Date: Tuesday, November 16, 1999	Sheet 2 of 9	


HARDWARE MODIFICATION #14
Install a jumper wire (resistor lead) at location JP2 Pin#2 to hole just above (Gnd) and at location JP2 Pin#3 to hole just above (Gnd).
JP1 & JP2 combine to create a three (3) row header
HM#14
Note: on the PCB jumper labels are reversed.
HARDWARE MODIFICATION #18
Remove resistor at location R45 and install a Zero Ohm resistor.
ECL SIGNAL TERMINATION
HARDWARE MODIFICATION #2
Change surface mount resistors R107 and R108 (on solder-side of board) to 100 Ohms.
HM#18
LED Located at front panel.
LED Located near G-Link.
LED Located near G-Link.
HM#25
HM#34
HARDWARE MODIFICATION #34
Install "capacitors boards" at locations U46, U47 and U48.
HARDWARE MODIFICATION #25
Add a wire from U17-9 to U20-20 and add a wire from U20-23 to J50 (of U28).
HM#25
HARDWARE MODIFICATION #47
Remove U60 and U61 and replace with 74ABT861PWDH (Philips).
HM#47
FERMILAB / CD/ESE
FIB FANOUT G_LINK
Size D
Document Number
Rev B
Date: Tuesday, October 12, 1999
Sheet 3 of 9


U28
FIFOCTL
U39
U38
U40
U34
U32
U31
U33
CY7C4251
HARDWARE MODIFICATION #3
Add a wire from U39-15 (Test FIFO) to jumper hole J72 which is connected to U28-58 (FIFO_CTL).
HARDWARE MODIFICATION #10
Unsolder pin#14 of U39 and U40 and then cut it so there is no longer a connection.
HARDWARE MODIFICATION #51
Cut trace to U34-6 (Error FIFO) and add a wire from Pin-6 of U34 to J62 (connected to U26-69, Error Latch ISP, FIB Error signal).
HARDWARE MODIFICATION #52
Cut trace to U34-5 (Error FIFO) and add a wire from Pin-5 of U34 to U26-37 (Error Latch ISP, Optical Power Low).
HARDWARE MODIFICATION #55
Unsolder and remove U39 from the PC Board, cut the trace from U39-19 to the via it connects to, replace U39 on the PC Board. (Need ISP Code August 27 or later).
HARDWARE MODIFICATION #50
Cut trace going to U34-21 (Error FIFO, DB29) near the via by GND test point J60.
HARDWARE MODIFICATION #53
Cut and remove the following pins: U31-14, U32-14, U33-14 (EFEF).
HARDWARE MODIFICATION #54
Cut and remove the following pins: U31-15, U32-15, U33-15 (EFFF).
HARDWARE MODIFICATION #25
Add a wire from U17-9 to U20-20 and add a wire from U20-23 to J50 (of U28).
HARDWARE MODIFICATION #49
Add a wire from U32-23 (Error FIFO,DB23) to J59 (connected to U28-47, FIFO Controller).
HARDWARE MODIFICATION #63
Add a wire from U28-20 (FIFO Controller PLD, Save Error) to J48 (connected to U28-19, FIFO Controller PLD).
HARDWARE MODIFICATION #48
Add a wire from U31-7 (Error FIFO, almost full flag) to J67 (connected to U28-70, FIFO Controller).
HARDWARE MODIFICATION #62
Lift U27-6, cut the pin. Connect a wire from the pad U27-6 to test point J55 (it goes to U28-7).
TEST AND ERROR FIFO CONTROLLER
TEST FIFO REGISTER RELATIVE ADDRESS 0X001C
ERROR FIFO RELATIVE ADDRESS 0x0028
DB[31..0]
GLD[19..0]
FERMILAB / CD/ESE
FIB FANOUT FIFOS
Size D
Document Number
Rev B
Date: Tuesday, November 16, 1999
Sheet 4 of 9

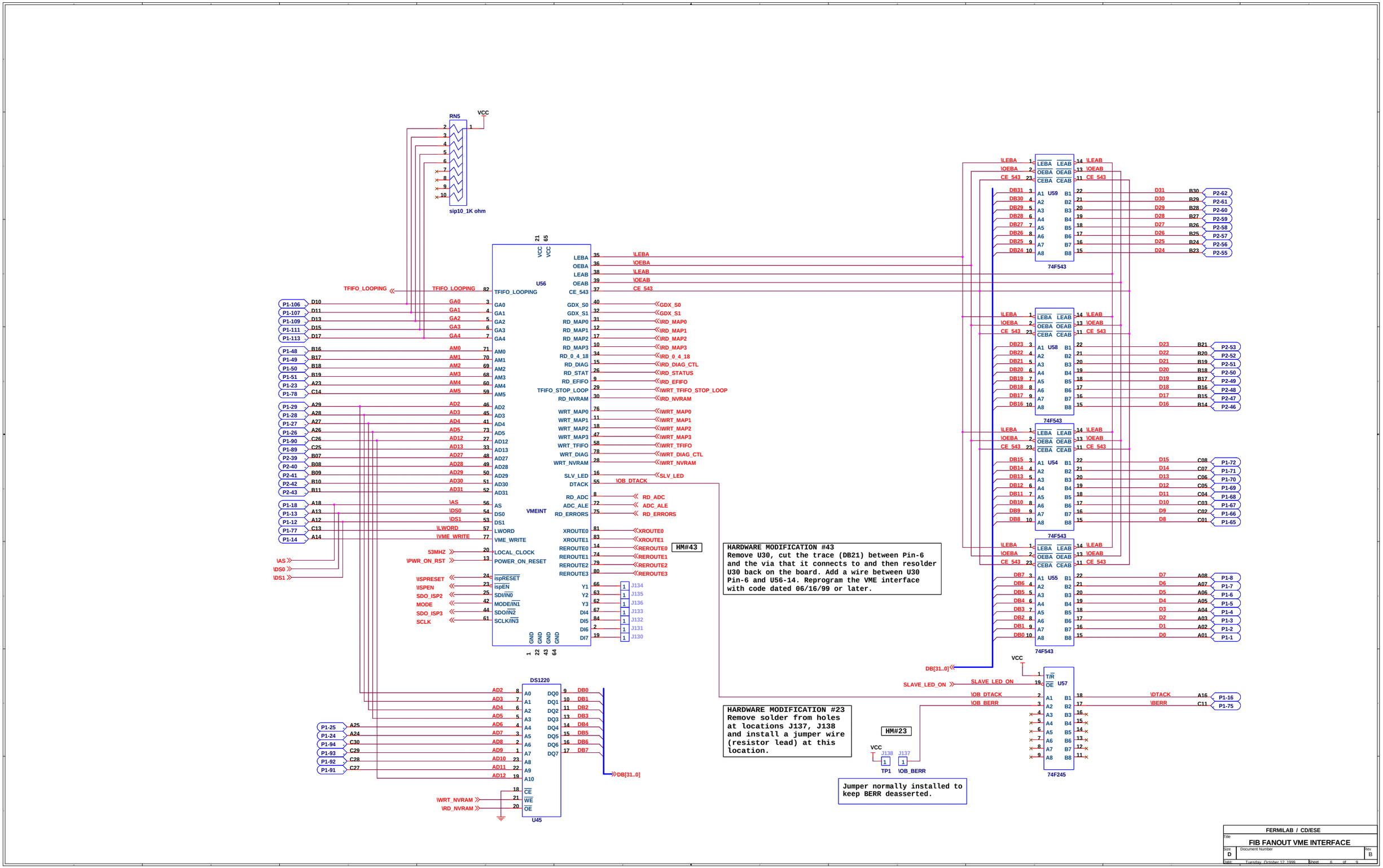


FERMILAB / CD/ESE

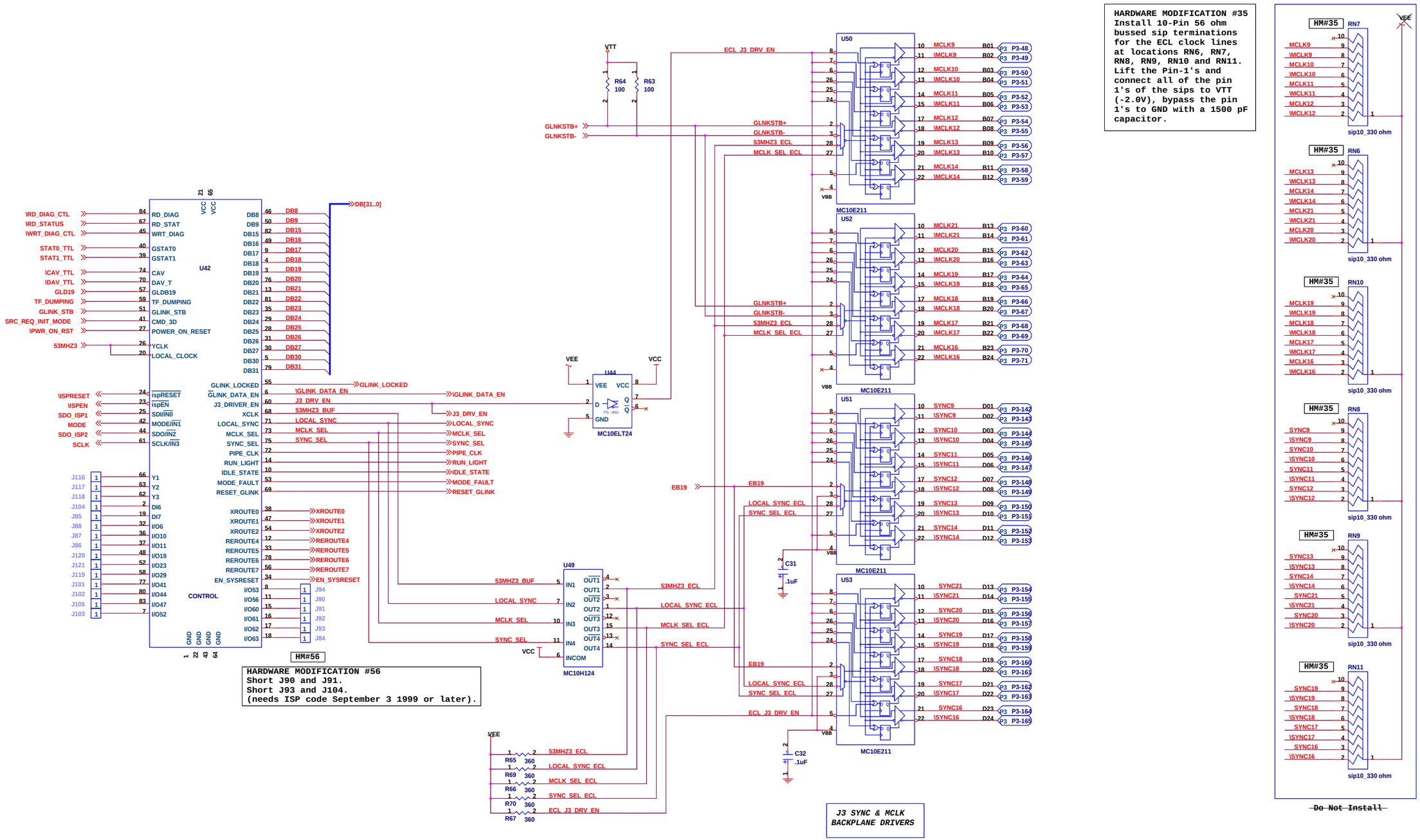
Title: ERROR-DECODER

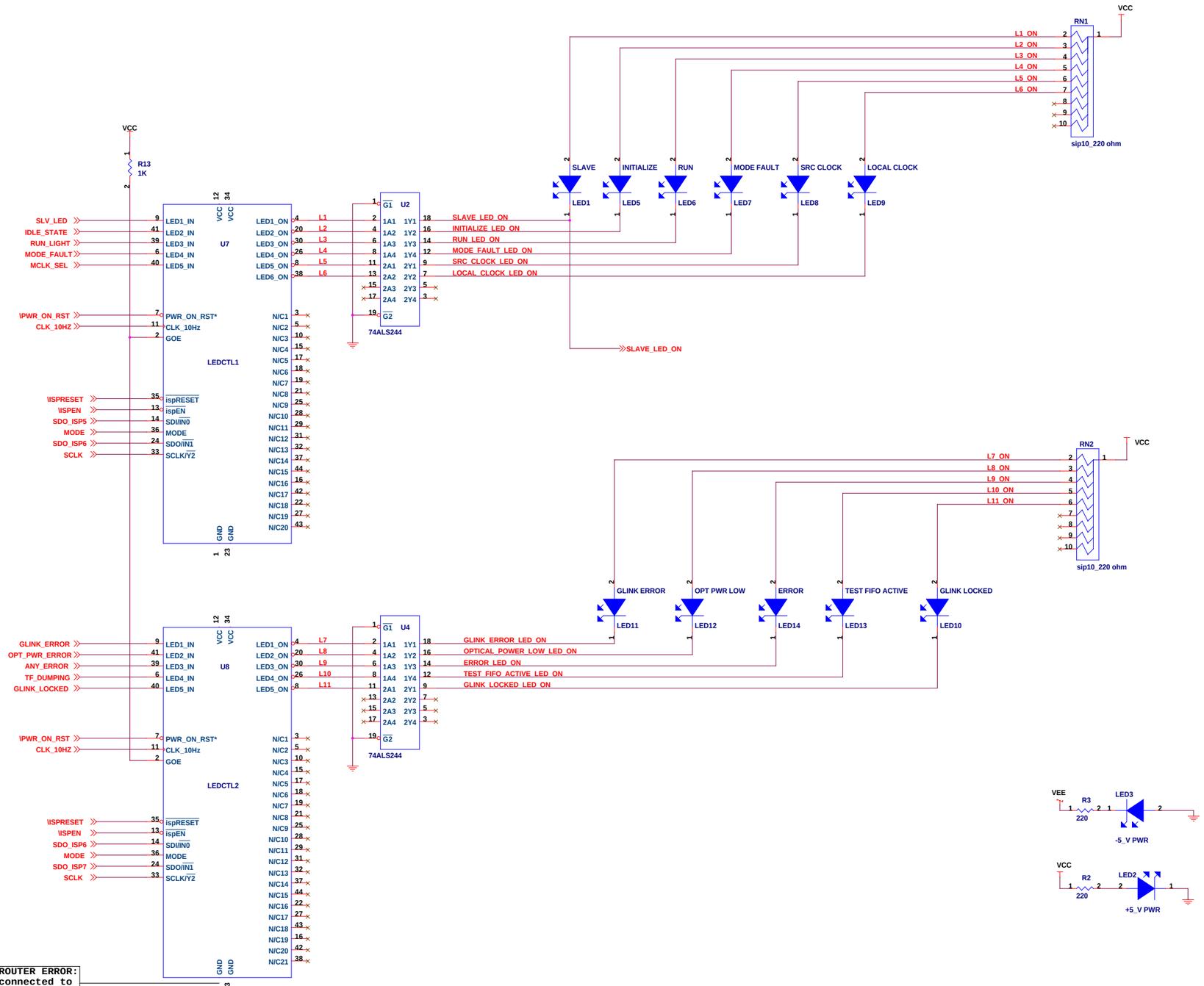
Size: D | Document Number | Rev: B

Date: Friday, October 01, 1999 | Sheet 5 of 9



RN5
VCC
sip10_1K ohm
U56
TFIFO_LOOPING
VMEINT
HM#43
HARDWARE MODIFICATION #43
Remove U30, cut the trace (DB21) between Pin-6 and the via that it connects to and then resolder U30 back on the board. Add a wire between U30 Pin-6 and U56-14. Reprogram the VME interface with code dated 06/16/99 or later.
HARDWARE MODIFICATION #23
Remove solder from holes at locations J137, J138 and install a jumper wire (resistor lead) at this location.
HM#23
Jumper normally installed to keep BERR deasserted.
DS1220
U45
U59
U58
U54
U55
U57
74F543
74F245
DB[31..0]
SLAVE_LED_ON
TP1
\OB_BERR
FERMILAB / CD/ESE
FIB FANOUT VME INTERFACE
Size D
Document Number
Rev B
Date: Tuesday, October 12, 1999
Sheet 6 of 9

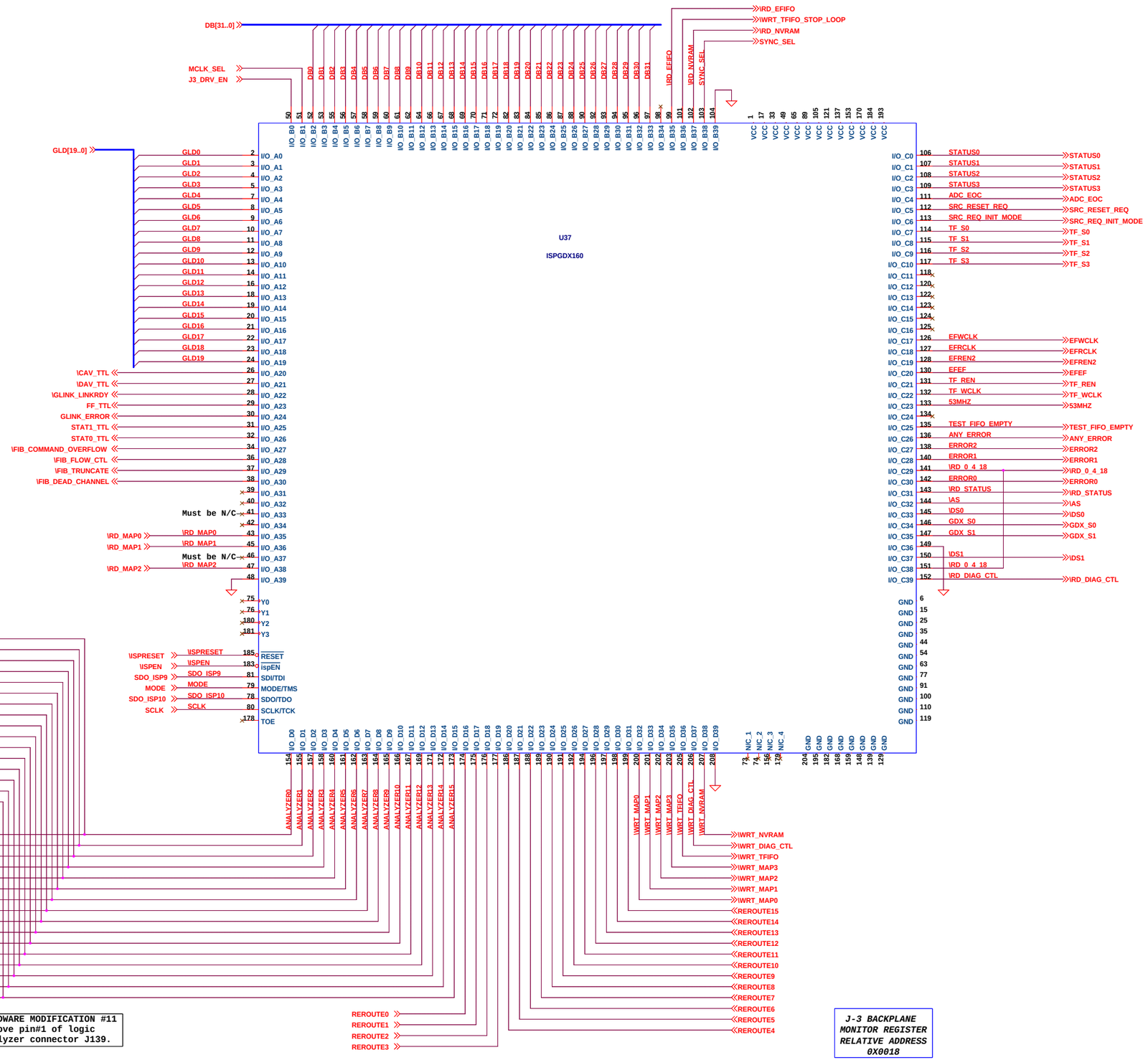

U42
U50
U52
U51
U53
U44
U49
MC10E211
MC10ELT24
MC10H124
R64 100
R63 100
VTT
VEE
VCC
GLNKSTB+
GLNKSTB-
53MHZ3_ECL
MCLK_SEL_ECL
LOCAL_SYNC_ECL
SYNC_SEL_ECL
ECL_J3_DRV_EN
EB19
C31 .1uF
C32 .1uF
R65 360
R69 360
R66 360
R70 360
R67 360
DB[31..0]
GLINK_LOCKED
\GLINK_DATA_EN
J3_DRV_EN
LOCAL_SYNC
MCLK_SEL
SYNC_SEL
PIPE_CLK
RUN_LIGHT
IDLE_STATE
MODE_FAULT
RESET_GLINK
XROUTE0
XROUTE1
XROUTE2
REROUTE4
REROUTE5
REROUTE6
REROUTE7
EN_SYSRESET
CONTROL
HM#56
HARDWARE MODIFICATION #56
Short J90 and J91.
Short J93 and J104.
(needs ISP code September 3 1999 or later).
HARDWARE MODIFICATION #35
Install 10-Pin 56 ohm
bussed sip terminations
for the ECL clock lines
at locations RN6, RN7,
RN8, RN9, RN10 and RN11.
Lift the Pin-1's and
connect all of the pin
1's of the sips to VTT
(-2.0V), bypass the pin
1's to GND with a 1500 pF
capacitor.
HM#35
RN7
RN6
RN10
RN8
RN9
RN11
sip10_330 ohm
Do Not Install
J3 SYNC & MCLK
BACKPLANE DRIVERS
FERMILAB / CD/ESE
FIB FANOUT FIB CLOCK CONTROLLER
Size D
Document Number
Rev B
Date: Tuesday, October 12, 1999
Sheet 7 of 9



PCB LAYOUT AUTOROUTER ERROR:
PIN-1 (GND) is connected to PIN-20 (L8).

HARDWARE MODIFICATION #6
Unsolder and remove U8 from the PC Board, cut the trace from U8-1 to the via it connects to, replace U8 on the PC Board and add a wire from U8-1 to the ground side (-) of C7.

FERMILAB / CD/ESE	
Title	FIB FANOUT INDICATOR LED'S
Size D	Document Number
Rev. B	
Date: Friday, October 01, 1999	Sheet 8 of 9



Title	FERMILAB / CD/ESE
	FIB FANOUT DIAG
Size D	Document Number
Rev B	
Date: Wednesday, September 29, 1999	Sheet 9 of 9