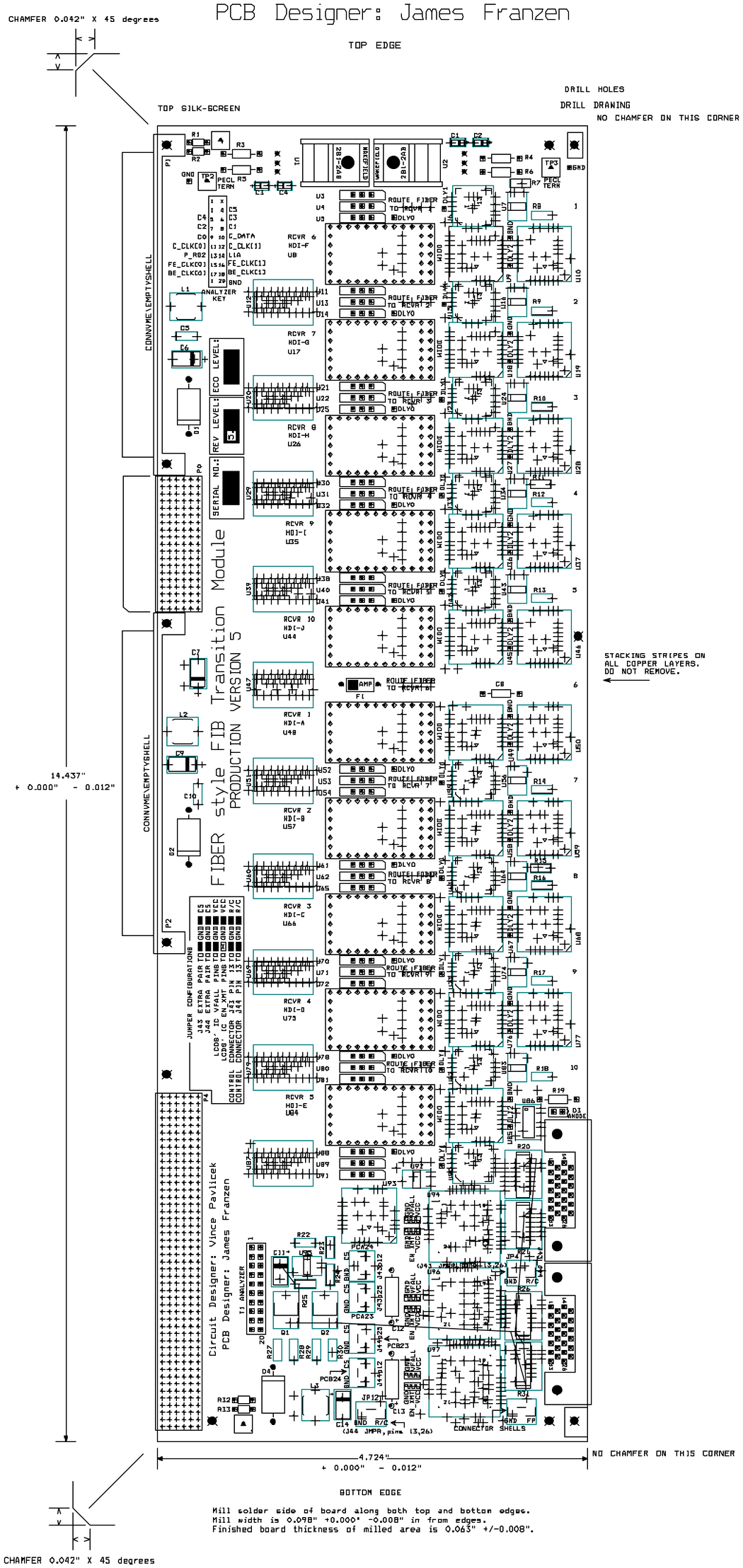
FIB TRANSITION MODULE--FIBER OPTIC VERSION

FERMILAB/Computing Division

PCB Designer: James Franzen



LAYER STACKUP:
LAYER 1: TOP SIGNAL (*CONTROLLED IMPEDANCE)
LAYER 2: GROUND PLANE
LAYER 3: SIGNAL A (*CONTROLLED IMPEDANCE)
LAYER 4: GROUND PLANE
LAYER 5: SIGNAL B (*CONTROLLED IMPEDANCE)
LAYER 6: GROUND PLANE
LAYER 7: VCC PLANE
LAYER 8: VTERM1 PLANE
LAYER 9: VTERM2 PLANE
LAYER 10: VCC PLANE
LAYER 11: GROUND PLANE
LAYER 12: SIGNAL C (*CONTROLLED IMPEDANCE)
LAYER 13: GROUND PLANE
LAYER 14: SIGNAL D (*CONTROLLED IMPEDANCE)
LAYER 15: GROUND PLANE
LAYER 16: BOTTOM PADS (*CONTROLLED IMPEDANCE)
*REGARDING THE CONTROLLED IMPEDANCE OF THIS BOARD:
1) THE FINISHED THICKNESS OF THIS BOARD SHALL BE 0.093"+/-0.008"
2) THE TARGET IMPEDANCE FOR ALL IMPEDANCE CONTROLLED LAYERS SHALL BE AS HIGH
AS ACHIEVABLE WITHOUT EXCEEDING 100 OHMS.
3) THE STACKUP OF THIS BOARD SHALL BE SUCH THAT THE IMPEDANCE
OF ANY IMPEDANCE CONTROLLED LAYER SHALL HAVE NO GREATER DEVIATION THAN
10% FROM THE MEDIAN VALUE OF ALL THE CONTROLLED IMPEDANCE LAYERS.

FINISHED BOARD THICKNESS 0.093" +.000"/-.008"
MILLING AND CHAMFERING INFORMATION ON THIS LAYER

Material: FR-4 with Tg of 140 or greater.

Horizontal etch limits: No greater than -.001" in 1/2 oz. Cu layers.
No greater than -.002" in 1 oz. Cu layers.
No greater than -.004" in 2 oz. Cu layers.
Copper plating on PTH walls: Minimum 1 mil plating in the hole.
Drill Hole Tolerance: ◊.050 in. dia. or less: +/- 0.003 in.
Drill Hole Tolerance: 0.050 in. dia. or more: +/- 0.007 in.
No drill hole shall breakout from any pad. Min. annular copper ring radius: 0.002 in.
SMOBC
LPI Soldermask
Silkscreen color: White
HASL

PERMISSION IS GIVEN TO REMOVE UNUSED PADS ON INTERNAL LAYERS.

ANY PAD EMPLOYING A 0.016" HOLE IS A VIA, AND THE PLATING PROCESS FOR VIAS
MAY BE SUCH THAT THE FINISHED PTH SIZE IS 0, 9D LONG AS THE 1 MIL HOLE PLATING SPECIFICATION IS MET.

Testing Required: ☐ None
■ Flying Probe
☐ Clamshell

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Gerber List:

■	TAP (Drill Tape)	■	APP (Aperture List)
	FAB (Fabrication Drwg)	■	DRD (Drill Drwg)
■	DTS (Drill Tape Summary)	■	GTD (OrCAD Extended Gerber)
■	AST (Top Assembly)	■	ASB (Bottom Assembly)
■	SPT (Solder Paste Top)	■	SPB (Solder Paste Bottom)
■	SST (Silkscreen Top)	■	SSB (Silkscreen Bottom)
■	SMT (Solder Mask Top)	■	SMB (Solder Mask Bottom)
■	TOP (Top Signal)	■	BOT (Bottom Signal)
■	GND (Ground Plane)	■	PWR (Power Plane)
■	IN1 (Inner Signal 1)	■	IN5 (Inner Signal 5)
■	IN2 (Inner Signal 2)	■	IN6 (VTERM PLANE)
	IN3 (Inner Signal 3)	■	IN7 (VTERM2 PLANE)
■	IN4 (Inner Signal 4)		IN8 (Inner Signal 8)

DRILL CHART

SYM	DIAM	TOL	QTY	NOTE
+	0.016		1851	
⊕	0.020		18	
+	0.025		396	
◇	0.026		390	
○	0.031		4	
⊠	0.034		52	
⊞	0.038		174	
△	0.045		4	
×	0.054		6	
⊠	0.057		2	
⊙	0.060		6	
╳	0.100		11	
◈	0.110		4	
⊕	0.147		2	
TOTAL			2920	