

Fermi National Accelerator Laboratory

CDF Run IIb

MINI PORT CARD, PIGTAILS AND WING

Document # ESE-CDF-20011104

-PRELIMINARY-

November 4, 2001

Jeff Andresen, Guilherme Cardoso, Sergio Zimmermann

1	INTRODUCTION	3
2	SVX4 ESTIMATED CURRENTS	6
3	MINI PORT CARD.....	7
3.1	ELECTRICAL LAYOUT	7
3.1.1	<i>MPC ground and Hybrid digital ground.....</i>	7
3.1.2	<i>Layer Stackup.....</i>	7
3.1.3	<i>Voltage Drop of the ϕ Side Power Traces.....</i>	8
3.1.4	<i>Signal Simulation.....</i>	9
3.1.5	<i>Transceiver and Single Ended Signals.....</i>	11
3.1.6	<i>RTD.....</i>	12
3.1.7	<i>Detector Bias.....</i>	12
3.2	MECHANICAL LAYOUT	13
3.2.1	<i>MPC Profile.....</i>	13
3.2.2	<i>Transceiver Power Dissipation and Thermal vias.....</i>	13
4	WING CABLE:	14
4.1	TERMINATION RESISTORS ON THE WING CABLE	16
5	TRANSCEIVER CHIP TESTING	19
6	APPENDIX	21
7	REFERENCES	28

1 Introduction

The Mini Port Card (MPC) for CDF Run IIb is used to interface the Junction Port Card (JPC) to the hybrids (see Figure 1). All the communication between the JPC is done differentially, and with the hybrids is done using single ended or differential signals as required by the SVX4 chips. The MPC will be mounted at the end of the stave and electrically connected to the end of the ϕ and z side stave buses with wire bonds. The MPC, as the hybrids, will be a fine pitch thick film circuit on a BeO substrate. All active circuitry will be on one side of the MPC. Each MPC will contain five bare transceiver chips, and by-passing and termination components. Figure 2 shows a drawing of stave assembly with the MPC and the hybrids for the ϕ side. The hybrids for the z side are in the opposite side of the stave.

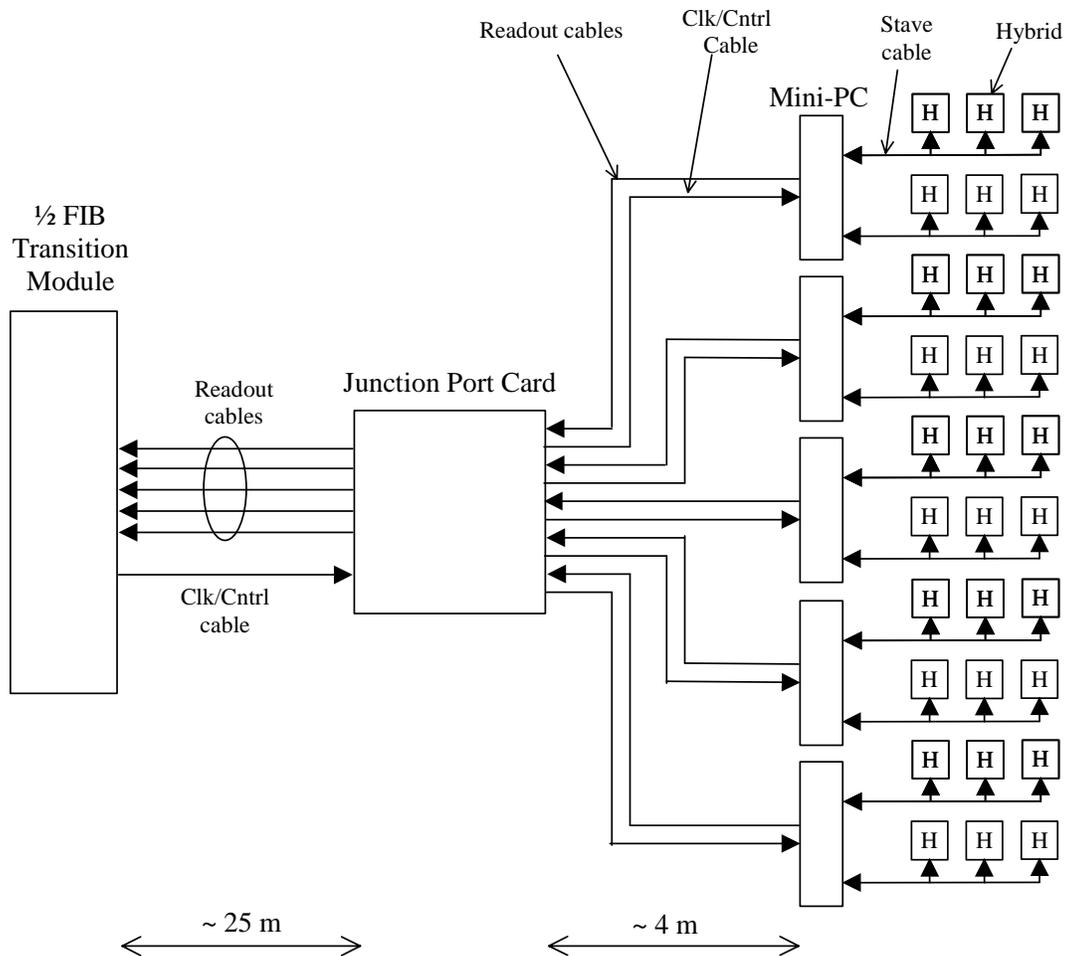


Figure 1. MPC Interconnected With Other Devices

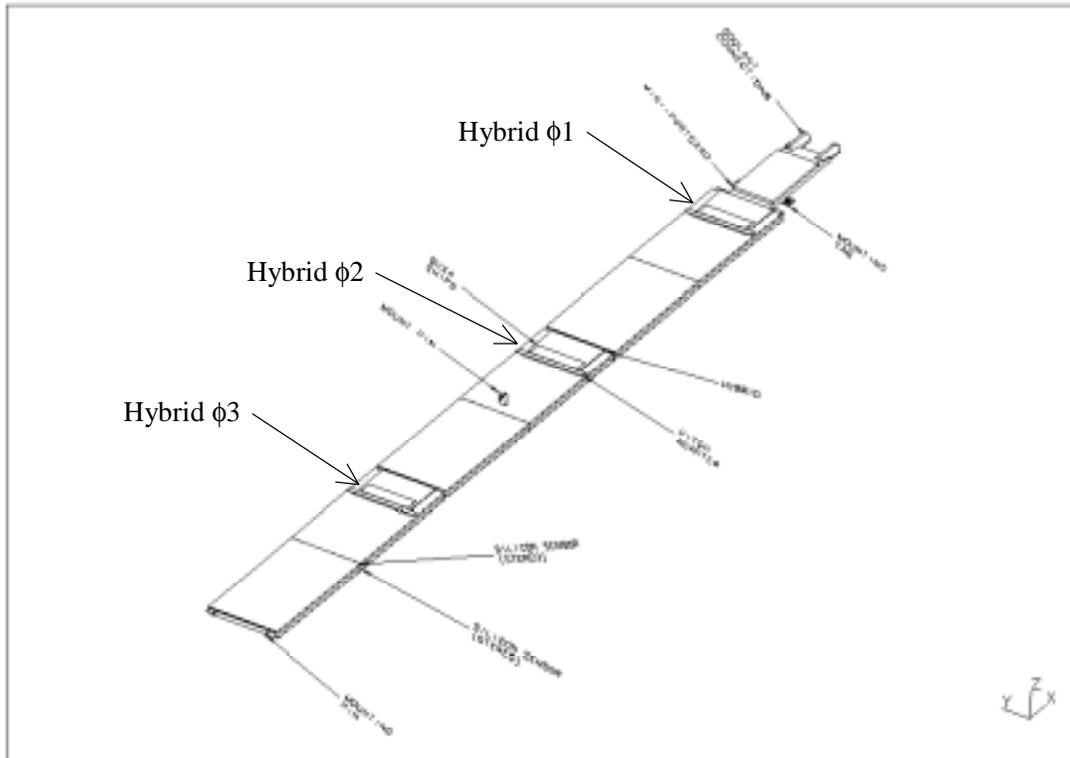


Figure 2. Stave Assembly

Figure 3 shows the block diagram of the MPC and interconnection with stave cable and hybrids. All communication between the MPC and the JPC use LVDS since the JPC's will be relatively far ~ 4 m from the staves. The clock lines (front-end and back-end) are regenerated on the MPC and sent to each hybrid using dedicated drivers and dedicated differential lines. The clock termination is mounted directly on the hybrids. The SVX4 single ended control signals (CHMODE, L1A, etc.) are transformed from differential to single ended on the MPC. Most are bussed to all hybrids in parallel but those with critical timing (L1A and PRD2) are driven individually to the ϕ and z sides of the stave. The data lines are shared between the two stave cables and terminated on the last hybrid of each stave bus. Bus 0:3 lines are bi-directional and the differential drivers regenerate the data in both directions, from the JPC to the hybrids and vice-versa. Several of these details will be reviewed and expanded along this document.

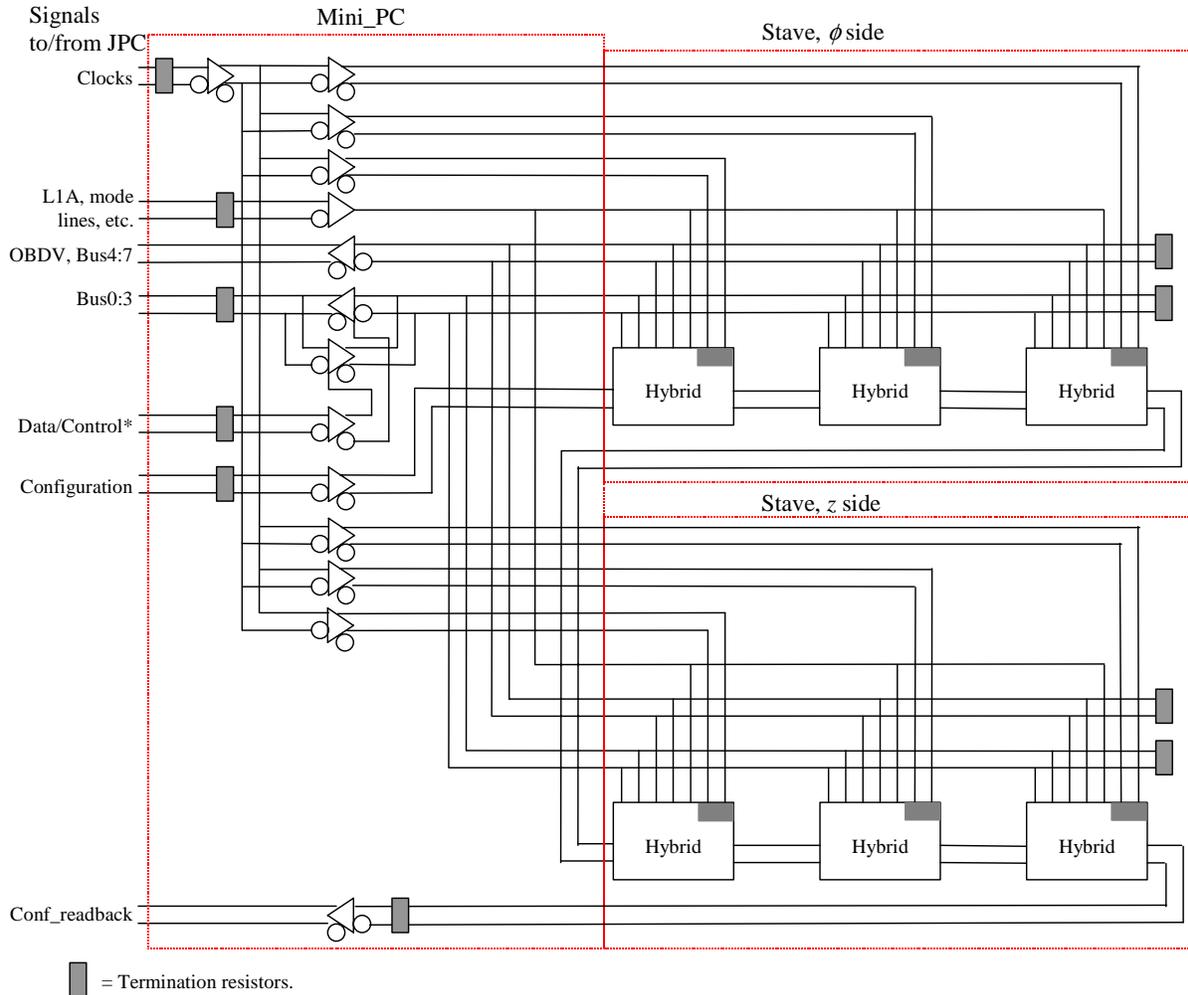


Figure 3. Block Diagram of the MPC and Stave Cable

A pair of short external flex cables (pigtailed) will connect the MPC to a longer cable set from the Junction Port Card. A wire bond pad field will enable connection to the ϕ side stave bus. An additional flex cable (the “wing”) will be solder to the MPC and bend around to the back side for bonding contact to the z side stave bus. Fabrication and assembly/test issues are similar to that of the hybrids. Figure 4 shows a sketch of the MPC connected to the associated pigtailed and the wing. This document also includes the description of these cables. The stave cable is described elsewhere. Approximately 200 MPC will be required to readout the Run IIb detector.

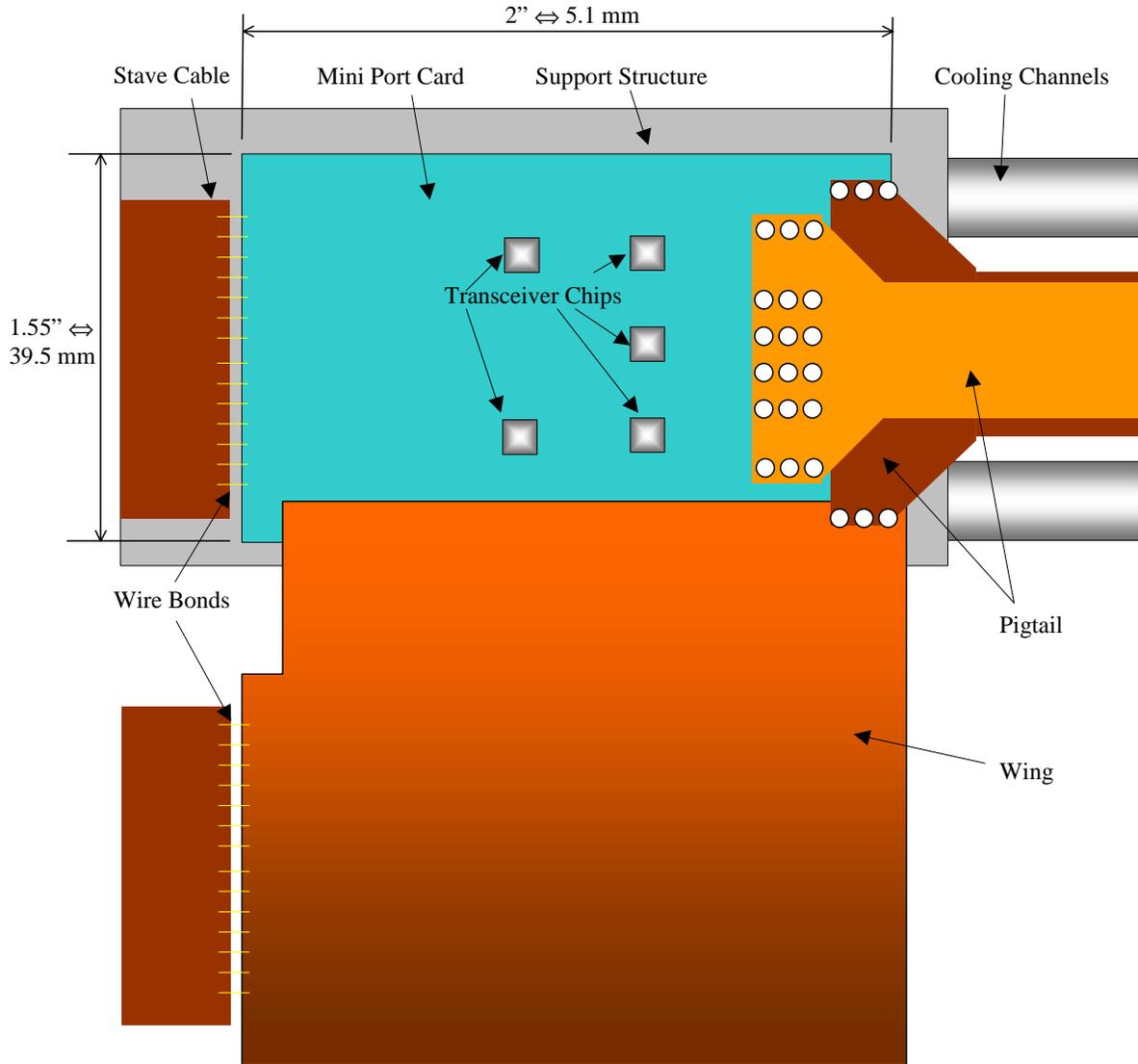


Figure 4. MPC, Wing, Stave Cable and Pigtails

2 SVX4 Estimated Currents

There is resistive voltage drop in the power and ground traces in the MPC, wing and pigtail. Table 1 shows the expected currents for the SVX4 chip, the hybrids and stave cable.

Table 1. Estimated SVX4 Currents

	SVX4	Hybrid	Stave Cable
A_{IDD}	0.1	0.4	1.2
$D_{IDD(\text{quiescent})}$	0.1	0.4	1.2
$D_{IDD(\text{readout})}$	0.2	0.5	1.3

3 Mini Port Card

3.1 Electrical Layout

3.1.1 MPC ground and Hybrid digital ground

This prototype of the MPC should allow for flexible testing of ground configurations between the hybrids, the MPC and voltage regulators. The MPC has its own ground and three more sets of digital and analog ground for the top three hybrids. Power and ground for the bottom hybrids are connected directly from the pigtail to the wing. The MPC generate single ended signals to control the hybrids and these signals require a ground path connection from the hybrid digital ground to the MPC ground.

For the top stave cable the MPC has three sets of wire bond pads distributed on the MPC. When the wire bond is assembled, it short-circuits that specific digital ground with the MPC ground. The pads are big enough to allow for multiple wire bonds to reduce the inductance.

For the wing and bottom stave the MPC has 3 solder pads that correspond to the digital grounds from the wing. The wing has also 3 through hole pads that are soldered to the pads in the MPC. In the MPC wire bond pads allow the connection these grounds together with the MPC ground. The trace from the solder pad to the wire bond pad in the MPC is as short and as wide as possible to reduce inductance. This also solves the wing's mechanical problem of not having any attachment to the MPC in that corner.

3.1.2 Layer Stackup

The list below describes the MPC layer stackup (starting from the top):

- Top solder mask layer providing the top dielectric
- Top metal layer with top pads and traces
- Dielectric layer
- Metal layer 2 (layer 2 of traces)
- Dielectric layer
- Metal layer 3 (layer 3 of traces and MPC power)
- Dielectric layer
- Ground: metal layer 4 providing ground for MPC transceivers and digital signal return currents.
- Beryllia board
- Power: metal layer 5 providing stave powers
- Dielectric layer
- Bottom metal layer 6 providing stave grounds
- Solid layer of dielectric.

3.1.3 Voltage Drop of the ϕ Side Power Traces

The MPC dimensions are shown in Figure 4. The two layers in the bottom of the MPC have the power traces that provide power and ground for the top stave hybrids. The power traces of the stave cable are designed to allow a 60 mV voltage drop for the hybrids farther from the MPC (hybrids $\phi 2$ and $\phi 3$ in Figure 2). The voltage drop in the power traces of the stave cable for the hybrid closer to the MPC (hybrid $\phi 1$ in Figure 2) is negligible because it is mounted very close to the MPC. For this reason, the power traces in the MPC connected with hybrid $\phi 1$ will allow for an additional 60 mV voltage drop and, therefore, minimize the voltage drop for the other hybrids.

A 60 mV additional voltage drop corresponds to additional resistance of $0.15 \Omega @ 0.4A$. The typical resistance of the gold for these two bottom layers is $5 m\Omega$ [1]. Figure 5 shows a sketch of the power traces with their widths w_1 and w_2 . The objective is to find these widths so that the voltage drop in DVDD_ $\phi 1$ and AVDD_ $\phi 1$ be 60 mV bigger than in DVDD_ $\phi 2$, DVDD_ $\phi 3$, AVDD_ $\phi 2$ and AVDD_ $\phi 3$.

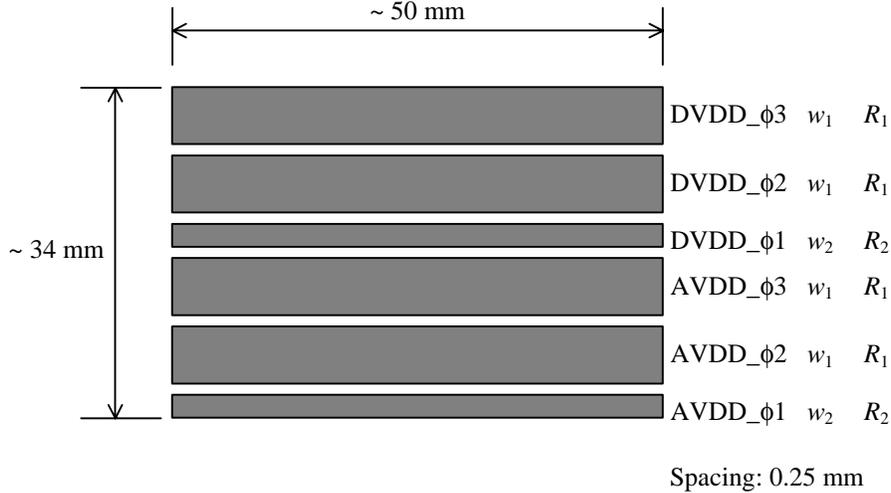


Figure 5. Power Traces for the ϕ Side Hybrid

Considering that $R = \frac{5l}{w} (m\Omega)$, that $l = 50$ mm and that the sum of the width of the traces (excluding the 0.25 mm spacing between each trace) is 32.75 mm allow us to write the following set of equations:

$$R_1 = \frac{2.5 \times 10^{-4}}{w_1} (\Omega)$$

$$R_2 = R_1 + 0.15 = \frac{2.5 \times 10^{-4}}{w_2} (\Omega)$$

$$4w_1 + 2w_2 = 32.75 \times 10^{-3} (m)$$

Solving these equations result in:

$$w_1=7.5 \text{ mm} \Rightarrow R_1=33 \text{ m}\Omega \Rightarrow \Delta V=13 \text{ mV @ } 0.4\text{A}$$

$$w_2=1.36 \text{ mm} \Rightarrow R_2=0.18 \text{ m}\Omega \Rightarrow \Delta V=73 \text{ mV @ } 0.4\text{A}$$

Of course, to consider the total voltage drop one has to add the drop for the power and ground, which doubles the voltages found above.

3.1.4 Signal Simulation

An important aspect of the interconnection of the MPC with the stave flex cables is the proper termination of the differential signals to avoid reflection on the lines. We have performed simulations to understand the termination schemes [2]. A particularly critical signal is the differential Odd Byte Data Valid (OBDV). If a glitch occurs in these lines, the DAQ system may store incorrect information. Figure 6 shows the result of such simulation with OBDV terminated as shown in the block diagram of Figure 3. The plot shows the two differential signals (OBDV and OBDV*) arriving to the OBDV differential input gate. These simulations were done using Spice and the circuit used is shown in Figure 7. The hybrid closer to the MPC is driving the OBDV. The driver used was the Spice description model of the transceiver differential driver; the MPC, stave cables (ϕ and z sides) and wing were simulated with a Spice lump transmission line; the wire bonds by 2 nH inductors and the chip inputs by 2 pF capacitors.

Table 2 shows the characteristics of each transmission line of this chain. In the simulation, the stave busses on both the ϕ and z sides are 35 cm long. One can observe that, after the signals switch, there is voltage ringing but it is small enough to display a minimum differential voltage between OBDV and OBDV* of ~ 350 mV, which insures that no glitch will happen. The ringing is produced by discontinuities on the transmission line caused by hybrids, wire bonds, capacitive load of the chips and impedance discontinuities from one type of transmission line to another (e.g., from stave cable to wing, etc.).

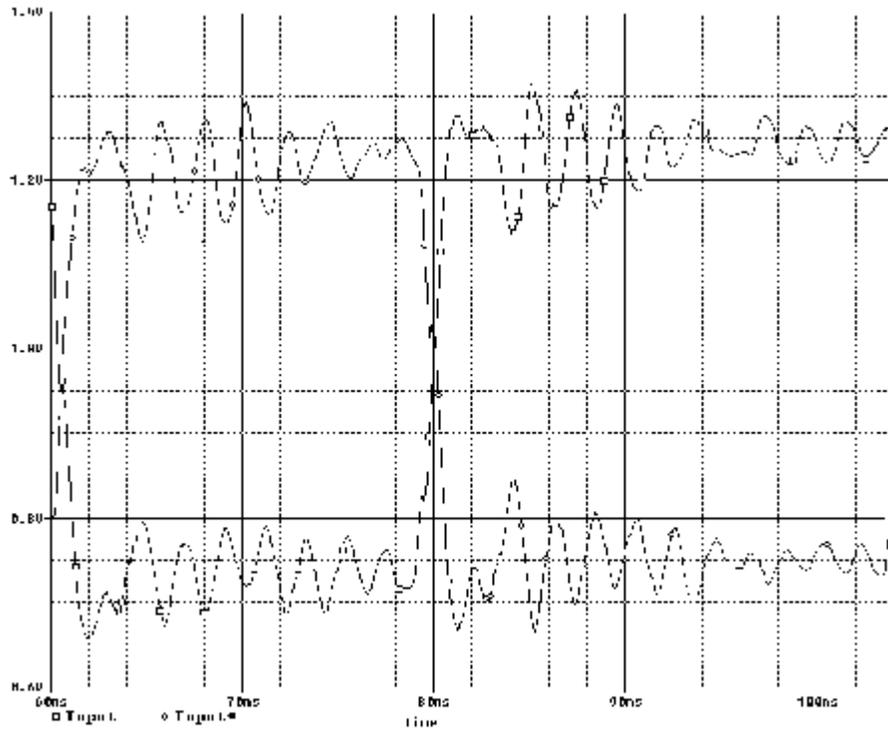


Figure 6. OBDV and OBDV* at the MPC

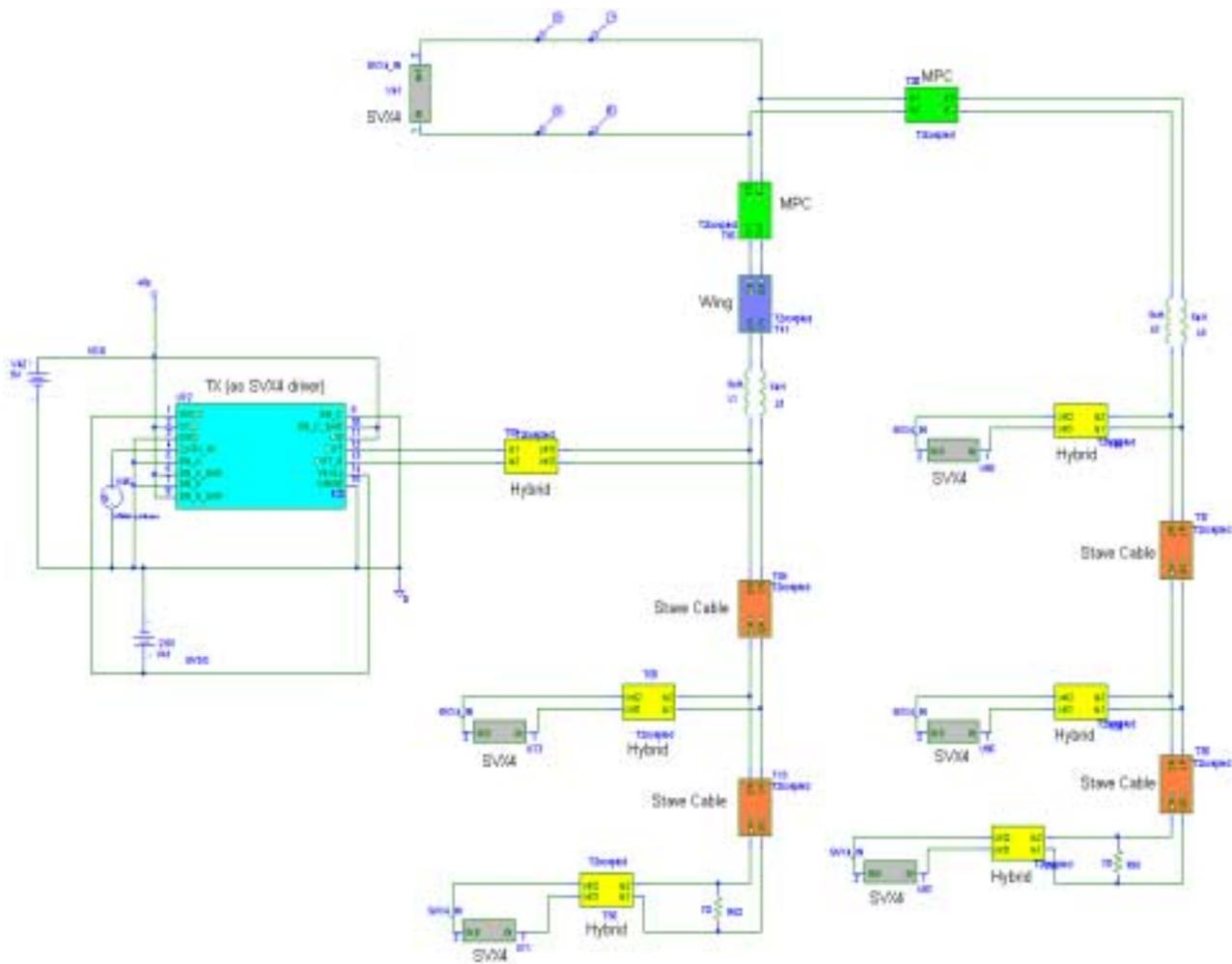


Figure 7. Circuit Used for Spice Simulations

Table 2. Configuration of Elements in the Data Chain

	Impedance (diff., Ω)	Substrate ϵ	Ground Plane		Traces			
			Top	Bottom	Length	Width	Separation	Thickness
Hybrid	68 Ω	7	-	80 μm	2.5cm	50 μm	50 μm	10 μm
Wing	83 Ω	3.9	-	100 μm	5cm	75 μm	100 μm	18 μm
Stave Cable	85 Ω	3.9	75 μm	75 μm	35.5cm	75 μm	100 μm	18 μm
Mini Port Card	70 Ω	7	-	120 μm	5cm	75 μm	75 μm	10 μm

3.1.5 Transceiver and Single Ended Signals

The MPC will use the Run IIA transceiver chips to generate the single ended 2.5V CMOS signals needed to control the SVX4 chips. Sufficient transceiver chips remain from the Run IIA project and are available to use in Run IIB. The transceiver chip was designed to operate with a 5.0V power supply. To use Run IIA chips, the MPC supplies 2.5 V power to a dedicated pad on the transceiver chip connected to the output stage, thus controlling the voltage swing of each differential output. Further enabling the maximum output current of the output stage (VFALL=2.5V, VRRISE=gnd and enable all output resistors) produces a reasonably powerful single ended driver.

Table 3 shows how the rise and fall times (10-90%) of the single ended transceiver output varies with different capacitive load when configured to convert a 5.0V input to a 2.5V output. This timing was measured using a transceiver irradiated by 18 Mrad (Co60 source). The capacitive load represented by all six hybrids, top and bottom stave cable, MPC and wing cable is estimated in 200 pF. The achieved speed for 220 pF is fast enough for most SVX4 single ended inputs. However, those with critical timing (e.g., L1A and PRD2) are driven individually to the ϕ and z sides of the stave to reduce the capacitance to one half ~100 pF and, thus, increase the speed.

Table 3. Timing of Single Ended Transceiver Output with Capacitive Load

Capacitive Load (pF)	Rise Time (ns)	Fall Time (ns)
82	15.5	16.2
220	36.2	42.5

3.1.6 RTD

Each hybrid has space for one RTD to measure its own temperature. Just one RTD will be assembled and readout per stave. To select the RTD from the ϕ or z side the MPC has wire bond pads which allow for wire bonding the top stave RTD, the bottom stave RTD or even connecting both top and bottom RTD in series or in parallel. Figure 8 shows a sketch of this pad field.



Figure 8. Pad Field for RTD Selection

3.1.7 Detector Bias

The maximum voltage for the detector bias is 500 V. The dielectric layer used by CPT supports 1000V/mil (1 mils ~ 25 μ m) and each dielectric layer has about 40 μ m. The high voltage traces on the MPC are laid out using the three top metal layers (see Figure 9). The top layer is the detector ground, the second layer has the high voltage trace and the third layer has the detector ground again. With this scheme the two detector grounds virtually shield the high voltage trace. The high voltage trace uses minimum trace width allow for this technology because very small currents flow through the trace.



Figure 9. High Voltage Layout

The separation between the high voltage traces in the inner layers of the MPC follows the IPC-2221 (Feb. 98) specifications for printed circuit boards and it is 10 mils (0.25 mm). For the solder field that connects the MPC with the flex cable the MPC follows the IPC-D-244 (Jan. 87) specifications for flex cables. It requires 100 mils separation (2.5 mm) for uncoated circuit, from sea level air pressures up to 10,000 ft. For the stave bus bond field the separation also follows the same specs for flex circuits for cover layered boards at any elevation: 30 mils (0.75 mm). The bond field will be protected by some epoxy.

3.2 Mechanical Layout

3.2.1 MPC Profile

Figure 10 shows the profile of the MPC and the maximum height of the components in different regions [3].

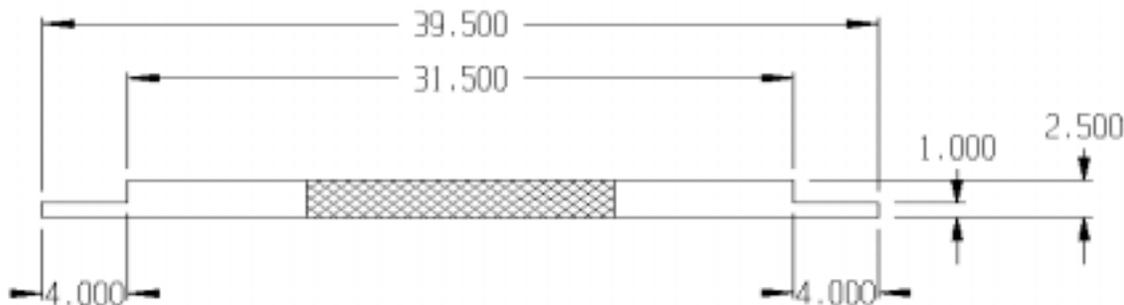


Figure 10. MPC Profile

3.2.2 Transceiver Power Dissipation and Thermal Vias

The dissipation of the transceiver chip will depend on its use. The worst case is when all outputs are used for differential signal. In this case proper resistive termination always requires some current to keep the differential voltage over the termination resistors. We have measured that the maximum output current when the chip is powered up with 2.5 V is ~7 mA. Considering that the chip has 10 gates, the maximum power dissipation of the differential output driver is 175 mW. The current of the differential input stage (powered by 5 V) of the transceiver was measured and

is 30 mA. Therefore, the total power dissipation of the transceiver is 325 mW. For the sake of the dimension of the thermal vias we will consider 500 mW.

For the study of the thermal vias we have three layers to be concerned with. The first is the top dielectric on which the chips are mounted. Since the dielectric has a poor conductivity and the area between the chip and dielectric is small, this is where we benefit most from thermal vias. For the substrate body, Beryllia (148 W/mK) have conductivities much better than the dielectric. What we want in this region is to spread the heat out away from the chip in order to maximize the effective surface area for subsequent heat transfer steps. Thermal vias do not really help here. In the bottom side dielectric, we can take advantage of larger surface areas than we had on the top, so the W/Area values are smaller. Once the heat arrives to the skin of the stove, it can funnel the heat to the cooling channels. The substrate thickness considered for the calculations was 0.5 mm. The result of the estimation is described in Table 4. The rate of return starts to get small after about 20 mils.

Table 4. Thermal Via Diameter \times Temperature Difference

Diameter (mils)	Temperature Difference (°C)
5	5.2
10	2.5
15	1.3
20	0.8
25	0.5
30	0.4
35	0.3
40	0.2

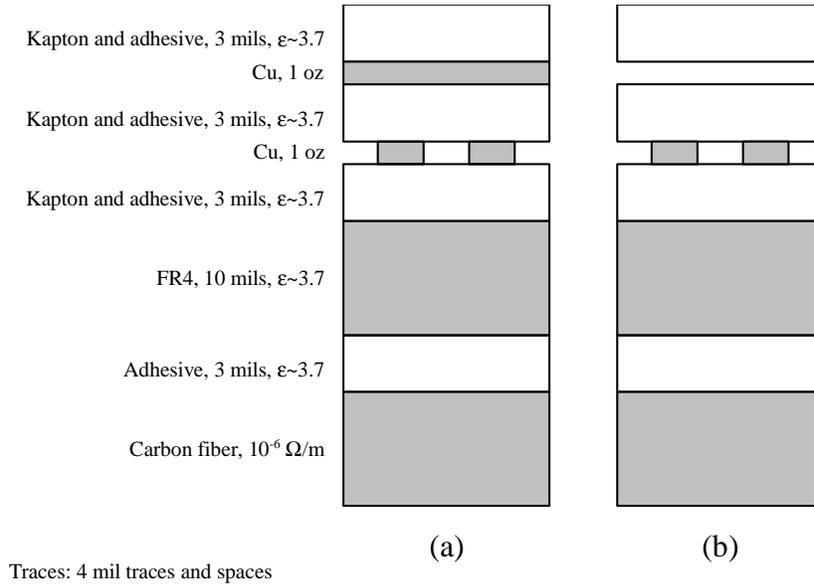
ADD THE PRIORITY RETURN GOING TO THE DAQ FROM THE PHI SIDE.

4 Wing cable:

The signals have 4 mil traces and spaces. We will assume a cable with 1 ounce/foot² thickness. The approximate dimensions of the Wing are 2200 x 1900 mils².

4.1 Characteristic Impedance of the Traces

The traces are 1 ounce/foot² Copper, 4 mil traces and spaces. The differential traces are in the same plane. There are four different cross sections as shown in Figure ??? with their correspondent characteristic impedance.



CASE (a)

```

Differential Z    = 77.2 ohms
Common-mode Z    = 55.8 ohms
Line-to-ground Z = 47.2 ohms
Characteristic Impedance Matrix [ohms]:
  1      2
  1  47.2  8.6
  2   8.6  47.2
Capacitance Matrix [pF/m]:
  1      2
  1 140.568 -25.664
  2 -25.664 140.568
Inductance Matrix [nH/m]:
  1      2
  1 302.969 55.315
  2  55.315 302.969
  
```

If separation between traces is 6 mils, the characteristics are:

```

Differential Z    = 84.2 ohms
Common-mode Z    = 53.1 ohms
Line-to-ground Z = 47.6 ohms
Characteristic Impedance Matrix [ohms]:
  1      2
  1  47.6  5.5
  2   5.5  47.6
Capacitance Matrix [pF/m]:
  1      2
  1 136.643 -15.725
  2 -15.725 136.642
  
```

Inductance Matrix [nH/m]:

	1	2
1	305.327	35.138
2	35.138	305.327

CASE (b)

Differential Z = 96.6 ohms

Common-mode Z = 149.7 ohms

Line-to-ground Z = 99.0 ohms

Characteristic Impedance Matrix [ohms]:

	1	2
1	99.0	50.7
2	50.7	99.0

Capacitance Matrix [pF/m]:

	1	2
1	85.885	-45.380
2	-45.380	85.885

Inductance Matrix [nH/m]:

	1	2
1	607.138	301.157
2	301.157	607.138

If separation between traces in case (c) is 3 mils the characteristics are:

Differential Z = 86.0 ohms

Common-mode Z = 153.7 ohms

Line-to-ground Z = 98.4 ohms

Characteristic Impedance Matrix [ohms]:

	1	2
1	98.4	55.4
2	55.4	98.4

Capacitance Matrix [pF/m]:

	1	2
1	93.626	-54.138
2	-54.138	93.626

Inductance Matrix [nH/m]:

	1	2
1	603.196	330.036
2	330.036	603.196

4.2 Termination Resistors on the Wing Cable

For testing the stave with just the top portion assembled (without the bottom....

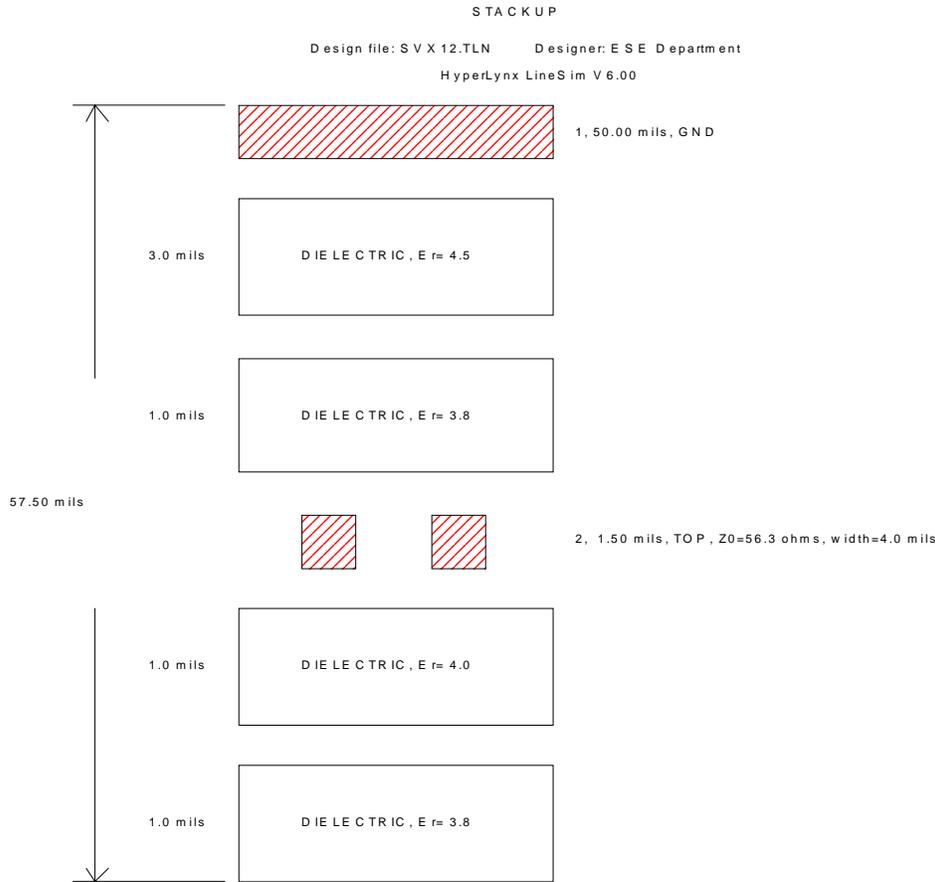


Figure 11. Stack Up of the Wing Cable

4.3 Voltage Drop of the r Side Power Traces

The digital and analog power traces are treated differently: the digital power traces are laid out in just one side of the wing, while the analog power and ground are laid out in both. Both use 1 ounce/foot² copper.

Figure 12 shows a sketch of the digital power traces. The digital power traces are laid out with approximately the same length of 52 mm. We will consider w_1 and R_1 the width and resistance of the traces with bigger width and w_2 and R_2 width and resistance of the traces with smaller width. Also, we will allow an additional 60 mV voltage drop (similar to power traces in the MPC, see Section 3.1.3) for the traces with w_2 width.

There is a region where the traces can be laid out in the top and bottom of the wing with vias interconnecting both sides. In this region, the traces with w_1 width can be a half of the original width; the cross section area will be the same. The traces with w_2 width have the same width and no trace on the bottom because they already are quite narrow.

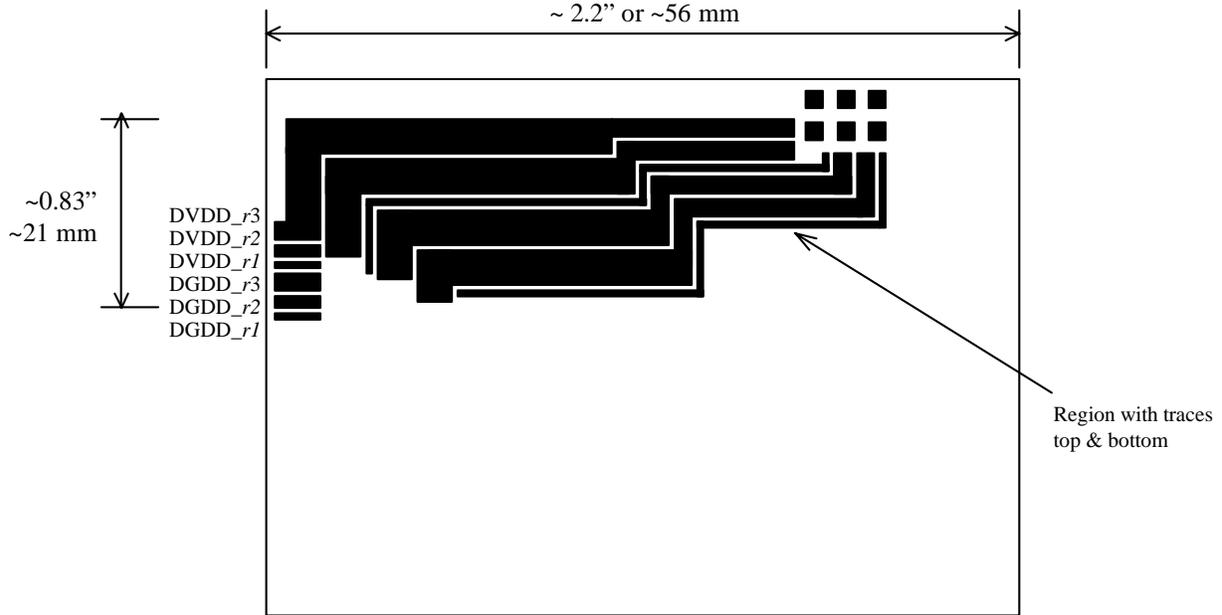


Figure 12. Sketch of the Digital Power Traces

With all these considerations in place, we can now calculate the width of the traces in the region with no “half widths”. A 60 mV additional voltage drop corresponds to additional resistance of $0.15 \Omega @ 0.4A$. The typical resistance of 1 ounce/foot² copper is $R = 0.46 m\Omega \square$. The objective is to find these widths so that the voltage drop in DVDD_r1 and DGDD_r1 is 60 mV bigger than in DVDD_r2, DVDD_r3, DGDD_r2 and DGDD_r3. Considering that $R = \frac{0.46l}{w} (m\Omega)$, that $l = 52$ mm and that the sum of the width of the traces (excluding the 0.1 mm (4 mils) spacing between each trace) is 20.5 mm allow us to write the following set of equations:

$$R_1 = \frac{2.4 \times 10^{-5}}{w_1} (\Omega)$$

$$R_2 = R_1 + 0.15 = \frac{2.4 \times 10^{-5}}{w_2} (\Omega)$$

$$4w_1 + 2w_2 = 20.5 \times 10^{-3} (m)$$

Solving these equations result in:

$$w_1 = 5 \text{ mm} \Rightarrow R_1 = 4.8 \text{ m}\Omega \Rightarrow \Delta V = 2 \text{ mV} @ 0.4A$$

$$w_2 = 0.16 \text{ mm} \Rightarrow R_2 = 0.155 \Omega \Rightarrow \Delta V = 62 \text{ mV @ } 0.4 \text{ A}$$

5 Transceiver Chip Testing

The transceiver chip has been extensively tested for the 2.5 V output level. Figure 13 shows the circuit configuration used to test the single ended output operation mode. Figure 13 and Figure 14 show the rise time of the output for a capacitive load (C_{load}) of approximately 220 pF and two levels of irradiation: 1 and 18 Mrad.

The radiation tolerance of the transceiver chips was studied by irradiating them upto a dose of 18 Mrad (Co60 source) [4]. Little degradation was seen in the signal quality for chips operated with 2.5 V output level, set to be compatible with the SVX4 chip. Figures~\ref{tek220pf_rise} and \ref{tek9r220} show the results for 1 and 18 Mrad with 220 pF capacitive load. These studies are detailed in a referenced document (refer to M.T.'s paper).

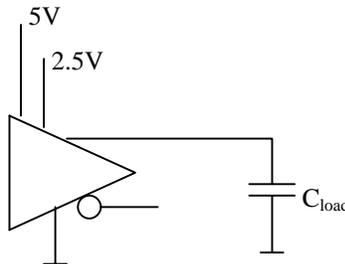


Figure 13. Single Ended Test Circuit

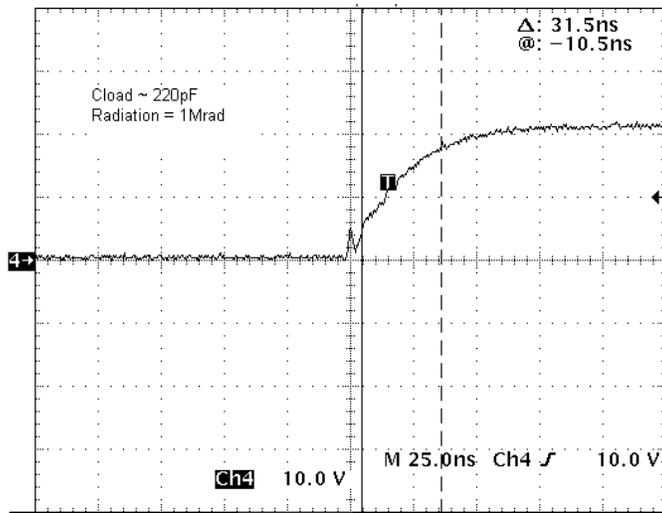


Figure 14. Cloud ~220pF, Radiation = 1 Mrad, $t_r \sim 31.5$ ns

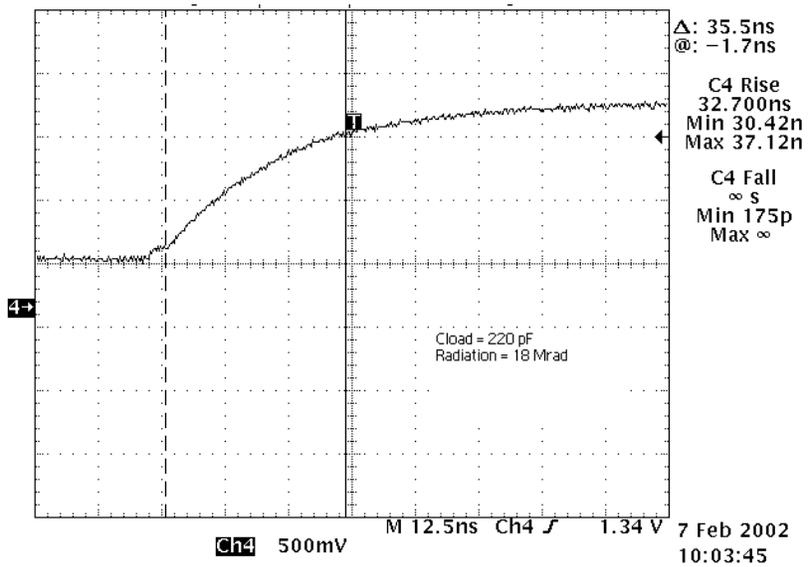
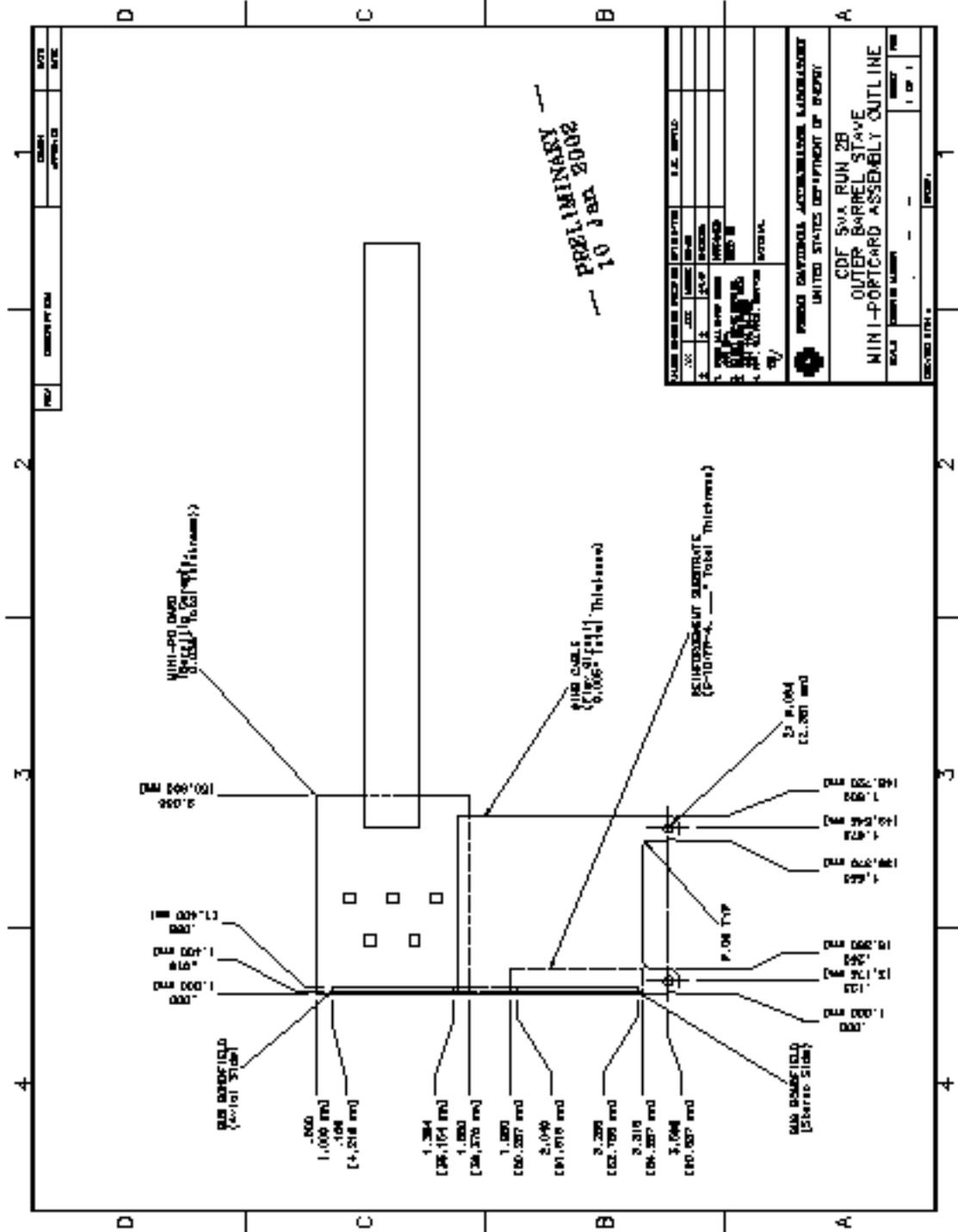


Figure 15. Cloud ~220pF, Radiation = 18 Mrad, $t_r \sim 31.5$ ns

6 Appendix A



7 Cables

There are three different types of cables: low voltage, high voltage and signal. Each hybrid will have its own analog and digital power and its own high voltage power supply.

7.1 Low Voltage

Each stage has six hybrids. Therefore, a total of 12