LANL Eight-Chip Calibration Results

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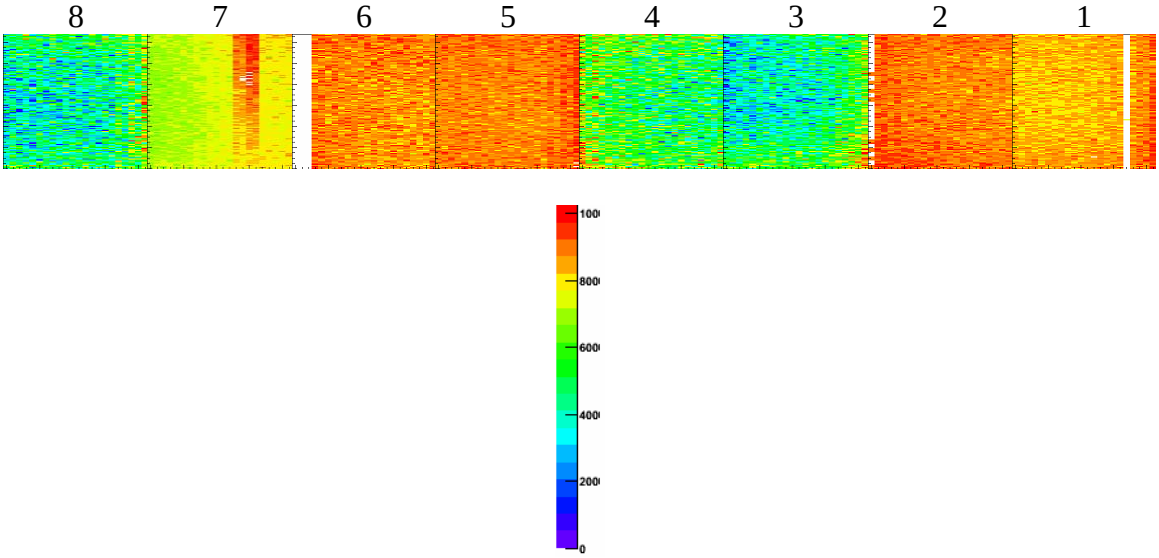
Hit Maps



Experimental Setup

For this calibration, an eight-chip HDI module was placed on a cold-plate. The software application, Pinga, was used to control the chips and to conduct the calibration. The parameters of the calibration can be found below.

Calibration Parameters

- Room Temperature: 23ºC
- Cold-Plate Temperature: 12ºC
- VDD: 2.5 V @ 420 mA
- VDA: 2.3 V @ 282 mA
- Master Clock: 25 MHz
- BCO Clock: 11 MHz

Results and Conclusions

Each of the eight chips will be discussed below. A conclusion will be drawn as to whether the chip was found to be "Good" or "Bad." Note that, unless otherwise specified, the register values for each chip's Vref, Vfb2, and VTH0 were set to 230, 200, and 200 respectively.

<u>Chip 8</u>

Parameters:

- Chip Temperature: 25.2ºC

Results:

Thr = 6792.1 ± 279.3 [e]
Noise = 108.1 ± 5.9 [e]

Conclusion:

"Good." No problems were detected with this chip. A second test was run on Chip 8 in which the register values were optimized such that the threshold mean was minimized. The results if this test can be found through the Phenix Online Resources in the Calibration Raw-Data section under the filename *LANL_C8_Vt200_Vr_210.**. To summarize, with the registers Vref, Vfb2, and VTH0 set to the values 210, 180, and 200 respectively, the threshold was found to be 2350 ± 240.8 [e], with a noise of 96.4 ± 5.3 [e].

Chip 7

Parameters:

- Chip Temperature: 26.3ºC

Results:

Thr = 8390.4 ± 542.6 [e]
Noise = 133.7 ± 9.7 [e]

Conclusion:

"Bad." Two peaks formed in the Threshold Dispersion plot. The first peak was centered on a high threshold, while the second peak was centered on an even higher threshold. Four columns were compromised.

Chip 6

Parameters:

- Chip Temperature: 27.7ºC
- Vref: 220, Vfb2: 190

Results:

Thr = 8742.9 ± 439.5 [e]
Noise = 202.0 ± 8.1 [e]

Conclusion:

"Bad." The register standards had to be changed for this chip; otherwise, the chip would become unstable. Three columns were compromised.

Chip 5

Parameters:

- Chip Temperature: 27.6ºC

Results:

Thr = 6497.3 ± 269.5 [e]
Noise = 112.7 ± 5.8 [e]

Conclusion:

"Good."

Chip 4

Parameters:

- Chip Temperature: 27.3ºC

Results:

Thr = 6274.0 ± 247.3 [e]
Noise = 106.1 ± 5.2 [e]

Conclusion:

"Good."

<u>Chip 3</u>

Parameters:

- Chip Temperature: 29.6ºC

Results:

Thr = 6536.6 ± 299.0 [e]
Noise = 107.1 ± 6.3 [e]

Conclusion:

"Good."

<u>Chip 2</u>

Parameters:

- Chip Temperature: 34.0ºC

Results:

Thr = 6422.7 ± 273.2 [e]
Noise = 120.0 ± 6.2 [e]

Conclusion:

"Good." However, one column was observed to have a high threshold.

<u>Chip 1</u>

Parameters:

- Chip Temperature: 42.0ºC

Results:

Thr = 6422.7 ± 273.2 [e]
Noise = 120.0 ± 6.2 [e]

Conclusion:

"Bad." The temperature observed for this chip causes the most concern. It is believed that this chip was responsible for the temperature gradient across the other seven chips. One column was compromised, and one pixel in this column was found to be extremely noisy.

Final Thoughts

Only five of the eight chips were considered useable based on the results of the calibration. Obviously, this is not an acceptable ratio. The major cause of this poor ratio was not pre-testing the chips before application to the HDI module. These results serve to emphasize the need for such an undertaking prior to chip installation.