

Fermi National Accelerator Laboratory

**D-Zero Detector Central Fiber Tracker (CFT) Axial Project
Readout Electronics**

Central Tracker Trigger (CTT) Mixer System

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1. People and acknowledgements

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2. Introduction

This document describes the mixer system, part of the readout electronics of the D-Zero detector Central Fiber Tracker (CFT) at Fermilab. More information on the experiments performed at Fermilab is available on the laboratory web page: <http://www.fnal.gov/>

More information on the D0 Detector is available on: <http://www-d0.fnal.gov/>

The designers welcome suggestions and corrections [Ref. 41], which can be addressed directly to the engineer responsible of the project. Contact information is available on the Electronics System Engineering Department (ESE) web page: <http://www-ese.fnal.gov/>

More information and documentation on the Mixer Project are available on:

http://www-ese.fnal.gov/D0_CTT_MIXER/

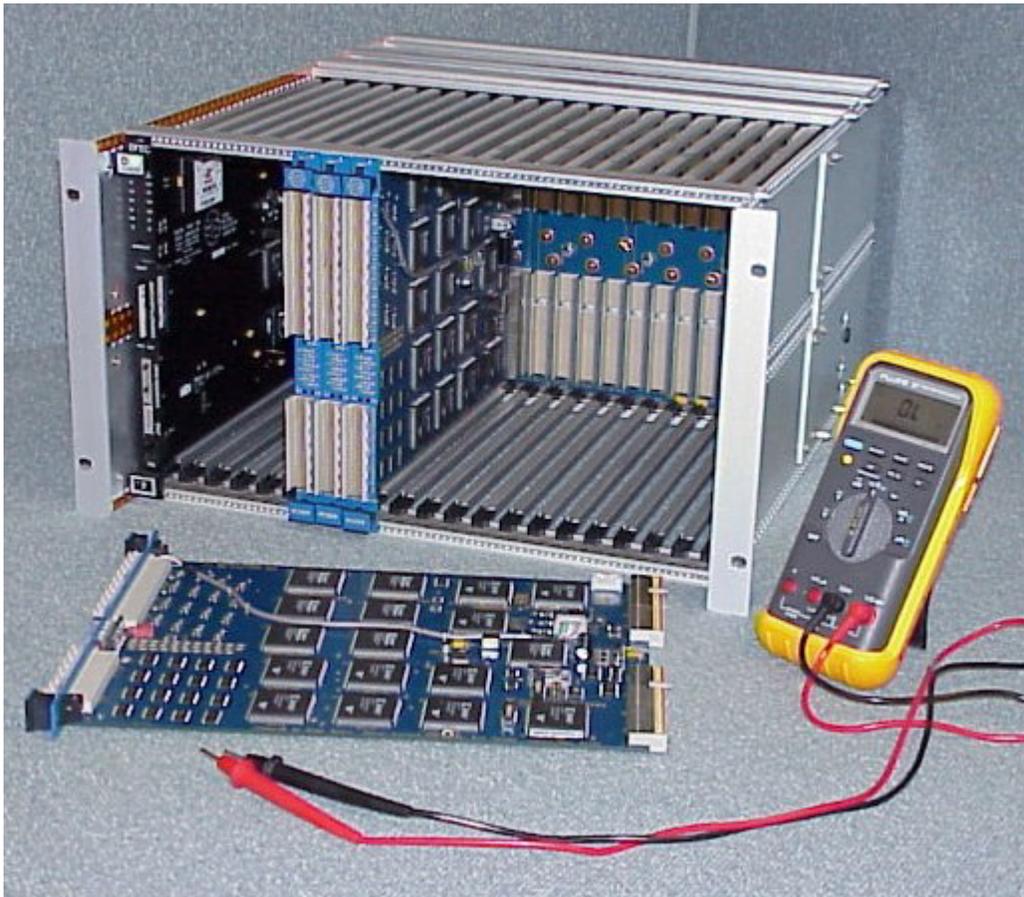


Figure 2.1, picture of the mixer system subrack.

A custom digital data Mixer System has been designed to reorganize, in real time, the data produced by the Fermilab D0 Scintillating Fiber Detector. The data is used for the level 1 trigger generation. The Mixer System receives the data from the front-end digitization electronics over 320 Low Voltage Differential Signaling (LVDS) links running at 371 MHz. The input data is de-serialized down to 53 MHz by the LVDS receivers, clock/frame re-synchronized and multiplexed in Field Programmable Gate Arrays (FPGAs). The data is then re-serialized at 371 MHz by LVDS transmitters over 320 LVDS output links and sent to the electronics responsible for level 1 trigger decisions. The Mixer System processes 311 Gigabits per second of data with an input to output delay of 200 nanoseconds.

To find a conceptual design solution that would comply with the design specification a software tool was designed and implemented. The tool allowed us to graphically visualize and analyze the data information and investigate possible design architectures. The tool was also used to generate the portion of VHDL code defining data multiplexing.

The Mixer System diagnostics allow monitoring input links, clock frequency, frame markers, control bits, clock synchronization, frame realignment and detecting/sending test patterns. The input links test pattern recognition and output links test pattern transmission is used by the trigger system diagnostic to verify the integrity and correctness of the cabling. The Mixer System diagnostic is remotely accessible. A simplified version of the diagnostic using bi-color LEDs on the Mixer board's front panel allow the user to view in real-time the status of signals and flags.

A component of the D0 Detector at Fermilab is the *Central Fiber Tracker (CFT)*. The CFT is constructed of scintillating fibers that are organized together in a very precise array of ribbons, placed onto a structure formed by eight co-axial cylinders. The energy deposited into the scintillating fibers by particle interactions is transformed into visible light. The light travels through the scintillating fiber and through an optical (clear) fiber connected to it, reaching a very sensitive light detector, the *Visible Light Photon Counter (VLPC)*, hosted in a liquid helium cryostat. The VLPCs are a derivative of solid-state photomultipliers and are used to convert the scintillation light into electrical signals. These are discriminated and digitized by the *Analog Front-End boards (AFEs)*. The Mixer System receives the digitized data from the AFEs, then processes and re-organizes it in real-time with minimal delay from cylindrical geometry into 80 azimuthal wedges or sectors. The restructured data are transmitted to the *Digital Front End (DFE)* board system. The DFE system uses the data to contribute to level 1 and level 2 trigger decisions.

Because the Mixer System was specified as a late addition to a previously designed system, there were many design constraints forced on the system. The most challenging constraints were the limited space available, the restricted access location, the system timing requiring minimal input to output delay, the number of input/output links, the clock/frame resynchronization of the input links data streams. A particular demanding constraint was the already fixed throughput of the Mixer System I/O links, just barely sufficient for the detector's data throughput. Due to limited budget and time available for the project, the specification also called for a custom design with minimal flexibility. Furthermore, the possible flavors of the Mixer board had to be based on the same hardware, so that only one board design would be needed. The fact that the system was to be installed in a limited access area also suggested a need for the capability to remotely run diagnostics and remotely update the system firmware.

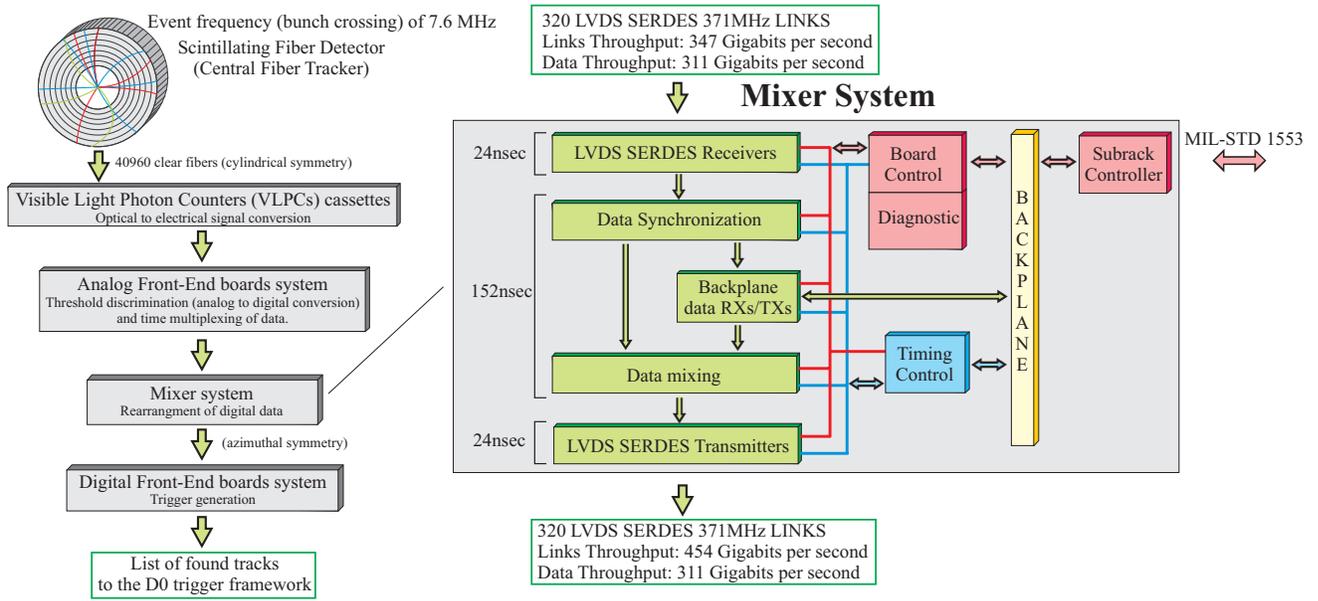


Figure 2.2, Data flow

The Mixer System consists of a 21-slot 6U subrack with a custom backplane. The subrack type was an initial constraint resulting from limited rack space available for a new component of the trigger system. The Mixer subrack first slot hosts a custom subrack controller, and the remaining slots host twenty Mixer boards. These twenty Mixer boards can be logically partitioned in five subsystems of four boards. This partitioning matches the fiber detector partitioning in five 72° wide sections or supersectors. This mechanical symmetry allows each supersector to be considered identical from the Mixer System's point of view. Each Mixer subsystem exclusively handles the data of one supersector, and because of detector symmetry, all five subsystems can use the same firmware. A portion of the data received by each of the Mixer boards, needs to be routed to another board in order to be part of the output data stream to which it belongs. The input links to the Mixer System have been arranged in such a way as to limit each Mixer board's data exchange to only the two adjacent boards. Furthermore, the five Mixer subsystems can be considered independent, because no data exchange is needed between them.

The Mixer System receives the data from the Analog Front-End boards over 320 Low Voltage Differential Signaling (LVDS) serializer/deserializer (SERDES) links, running at 371 MHz. The input links are of two types. 300 are 21 bits wide and 20 are 28 bits wide. The input data is de-serialized down to 53 MHz by the LVDS receivers, clock/frame re-synchronized and multiplexed in Field Programmable Gate Arrays (FPGAs), and then re-serialized at 371 MHz by the LVDS transmitters. The system has 320 LVDS SERDES output links, all are running at 371 MHz and all are 28 bits wide. Of the 320 output links only 240 carry unique data. The remaining 80 links have replicated data, and are needed to transmit some of the data to more than one DFE system's module. The Mixer System processes 311 Gigabits per second of data, with an input to output delay of 200 nanoseconds. Of this, 48 nanoseconds are used for data de-serialization/serialization, and 152 nanoseconds are used for data synchronization and mixing.

To find a conceptual design solution that would comply with the design specification, a software tool was designed and implemented. The tool is based on Microsoft Excel™ software package and makes extensive use of routines written in Visual Basic™ for Applications (VBA). The

tool allows graphical visualization and analysis of the data. It also permits arranging of the data in order to minimize the required number of interconnections between inner elements of the Mixer System to reorganize the data into azimuthal trigger sectors. The tool was also used to decide between possible hardware architectures, and after the architecture was chosen, to generate the portion of VHDL code defining how the system's FPGAs should "mix" data.

The Mixer board uses a total of 17 FPGAs. One FPGA is used as the board controller and is programmed at power-up by an on-board EEPROM. It implements the interface with the custom subrack controller, providing access to board's controls, diagnostics and a means to configure the remaining 16 FPGAs. The FPGA configuration files are stored on a CompactFlash™ memory card hosted by the subrack controller. The system firmware can be updated by replacing the memory card, or when the system is not accessible, downloading the configuration files to the memory card using the subrack controller MIL-STD-1553 interface. Of the 16 remaining FPGAs, 6 are used as the board front-end to perform data clock synchronization and frame realignment, 4 are used to exchange data through the backplane, and 6 as the board back-end to perform the data mixing and drive the output link transmitters. One of the 4 backplane FPGAs is also used as clock controller, and handles the board's clock and frame timing signals. One of the four Mixer boards in each subsystem acts as a timing master, and propagates clock and frame marker signals through the subsystem, allowing synchronous operations.

One critical component of a Mixer board is the diagnostic firmware. It allows monitoring input links, clock frequency, frame markers, control bits, clock synchronization, frame alignment and detecting/sending test patterns. The input links test pattern recognition and output links test pattern transmission is used by the trigger system diagnostic to verify the integrity and correctness of the cabling. The Mixer diagnostic is remotely accessible through the MIL-STD-1553 system interface. A simplified version of the diagnostic uses the reset push-button and 16 bi-color LEDs on the Mixer board front panel. This allows the user to view, in real-time, the status of 256 signals and flags, by scrolling through 16 "monitoring modes". The front panel accessible diagnostic has proven to be extremely useful during system testing and installation.

The Mixer System was comprehensively exercised before the commissioning phase using a test system which, aside from a limited data throughput, emulates closely the real data environment.

The system commissioning phase ended in February of 2002, support for system integration is ongoing at D0, and at this time only minor firmware changes are foreseen.

3. DAQ System Components

Scintillating Fiber Detector

Scintillating fibers are organized together in a very precise array of ribbons, placed onto a structure formed by eight co-axial cylinders (or layers). When a particle passes through a scintillating fiber, a brief flash of light occurs. The light travels through the scintillating fiber and through an optical (clear) fiber connected to it, reaching a very sensible light detector, a Visible Light Photon Counter (VLPC). The light generated in each of the 40960 detector's scintillating fibers goes to an independent VLPC.

Visible Light Photon Counters (VLPCs)

The VLPCs are a derivative of solid-state photomultipliers (SSPM) but different than their predecessor in that they are blind in the infrared region. VLPCs are solid-state detectors capable of detecting single photons having wavelength of 0.4 to 28 μm . Their operational temperature is between 6 and 14 K, requiring a cryogenic environment to operate. They are used in the CTT system to convert the scintillation light into an electrical signal, which is discriminated and digitized by the Analog Front-End boards (AFEs).

Analog Front-End Boards (AFEs) [Ref. 7]

The AFEs, process the analog signals from the VLPC channels, and supply the generated data to the mixer system. Originally the Central Fiber Tracker system was supposed to have two flavors of Analog Front-End (AFE) boards, one with 8 Multichip Modules (MCMs) to read the axial fiber and a 12 MCMs board flavor to readout the preshower fibers. Due to technical issues the final system uses only 8 MCMs boards. The mixer system design started with the assumption of a CTT system having two types of AFEs and even if this is no more the case, that assumption affected design decisions and is the reason for choices that may not look clear in today's light. Being that the mixer system design was already completed at the time the decision to use only 8MCM AFEs was made, this document will still reflect in several parts the original assumption of two types of AFE boards.

The digital data generated by the analog front-end will be used by the logic responsible for the level 1 trigger decisions. But before the data can be used for trigger generation it needs to be reorganized into trigger sectors, this is done by the mixer system.

Mixer system [Ref. 8]

The mixer system was conceived well after all the other CTT system components. The reasons for its existence are:

- a) The need for the logic generating the level 1 trigger (Digital Front-End boards) to receive the data organized in "trigger sectors".
- b) The difficulties arise in reorganizing the optical fiber in "trigger sectors" before the VLPCs. The mechanical design of the detector did not allow for the fiber ribbons to be arranged as desired/needed and the best option was the reorganization of the data after the digitizing process (AFEs).

Being the mixer system part of the electronics handling data used to generate a trigger, the data must be processed (re-organized) in real-time and with the minimum possible delay. The mixer system consists of a 21 slot 6U VME type subrack with custom backplane. Slot 1 is occupied by a custom subrack controller, slot 2 to slot 21 hosts twenty mixer boards.

Digital Front-End Boards (DFEs) [Ref. 5]

The "trigger sector organized" data produced by the mixer system is passed to the Digital Front End boards (DFEs) system that does the triggering. Following the Digital Front End, there is other electronics that concentrate the information, look for trigger information and send/broadcast it up to the framework (collectors and broadcasters).

3.1 Front End Data Flow

Figure 3.1 shows the D0 Central Fiber Tracker (CTT) structure organized in angular sectors and trigger sectors.

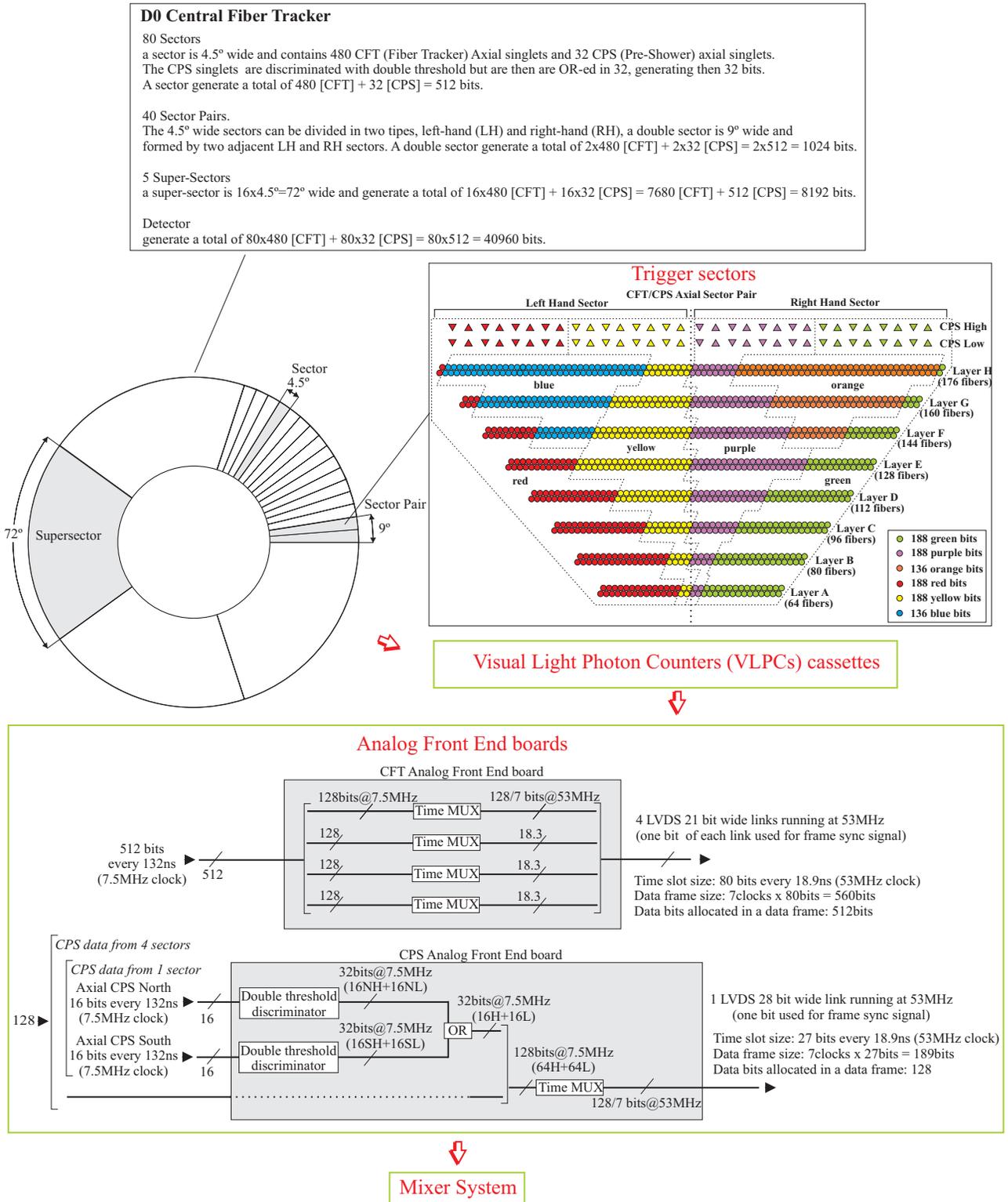


Figure 3.1, Front End data flow.

The fiber detector can be partitioned in five 72° wide "supersectors". Each supersector can be partitioned into forty 9° wide "sector pairs" or eighty 4.5° wide "sectors". Each sector pair is split in six "trigger sectors" identified by a color (blue ●, red ●, yellow ●, orange ●, green ●, purple ●).

The trigger sectors represent the data grouping done by the mixer system before the data is sent to the Digital Front-End boards system for trigger generation.

The Analog Front-End board block diagram in Figure 3.1 still shows the two types of AFE boards originally planned for the CTT system. In the current system only the type labeled "CFT Analog Front-End board" is used.

3.2 Supersector and Mixer Board Data Flow

From the mixer system point of view, the five supersectors look exactly the same. This is the reason for having the mixer system partitioned in five subsystems of four boards each. Every mixer subsystem handles the data from one supersector. Each of the five supersectors can be considered independent because no data exchange is needed between mixer subsystems.

This partitioning allowed concentrating the mixer system design effort on just a fifth of the detector and then replicating the subsystem for the other four supersectors.

Each Mixer board handles the data generated by two sector pairs. Because the data belonging to a particular set of two sector pairs is not necessarily received by the mixer board handling those sector pairs, there is the need of a board to board data exchange inside a mixer subsystem (four mixer boards). Thanks to the front-end system design, a mixer board needs to exchange data only with adjacent boards belonging to the same mixer subsystem.

The data from the Analog Front-End board system is received on Low Voltage Differential Signaling (LVDS) links. Two types of LVDS links are used, 21 bit wide to transmit CFT data and the 28 bit wide for CPS data. The data clock is, as it is for several systems at Fermilab, the Tevatron clock, which has a frequency of approximately 53 MHz. The LVDS transmitters on the AFEs serialize the data over balanced-pair conductors transmitting it with a clock seven times faster than the data clock (53MHz x 7= 371MHz). The LVDS receivers on the Mixer boards de-serialize the data received on the balanced pairs from 371 MHz LVDS back to 53 MHz Low Voltage TTL (LVTTTL).

In a mixer subsystem (4 mixer boards) the data is reorganized and serialized again by LVDS transmitters and sent to the Digital Front-End boards system that is responsible for trigger generation. Aside from LVDS components, the mixer board operates in LVTTTL. The board-to-board data exchange is also performed in LVTTTL.

Each Mixer board has sixteen LVDS receivers; fifteen of them are the 21 bit wide type (CFT data, input link# 1 to 15) and one is the 28 bit wide type (CPS data, input link#0). There are also sixteen LVDS transmitters, all of them are the 28 bit wide type, and are used to send the reorganized data to the DFEs. The output links are divided into two groups. This division is reflected in the numbering scheme, the first group has link numbers from 00 to 07, the second group link# 10 to 17. Throughout the mixer project documentation the two groups of output links are referred to as DFE0 and DFE1 links (because most of them go to two different DFE boards), plain color links and striped color links (to avoid confusion between links having the same trigger sector color and belonging to different groups).

The DFE boards need to share some of the data sent by the mixer system. This is achieved by duplicating some of the output links. In each of the two groups of 8 output links of a mixer board six links are unique and two of the links (green and red) are duplicates.

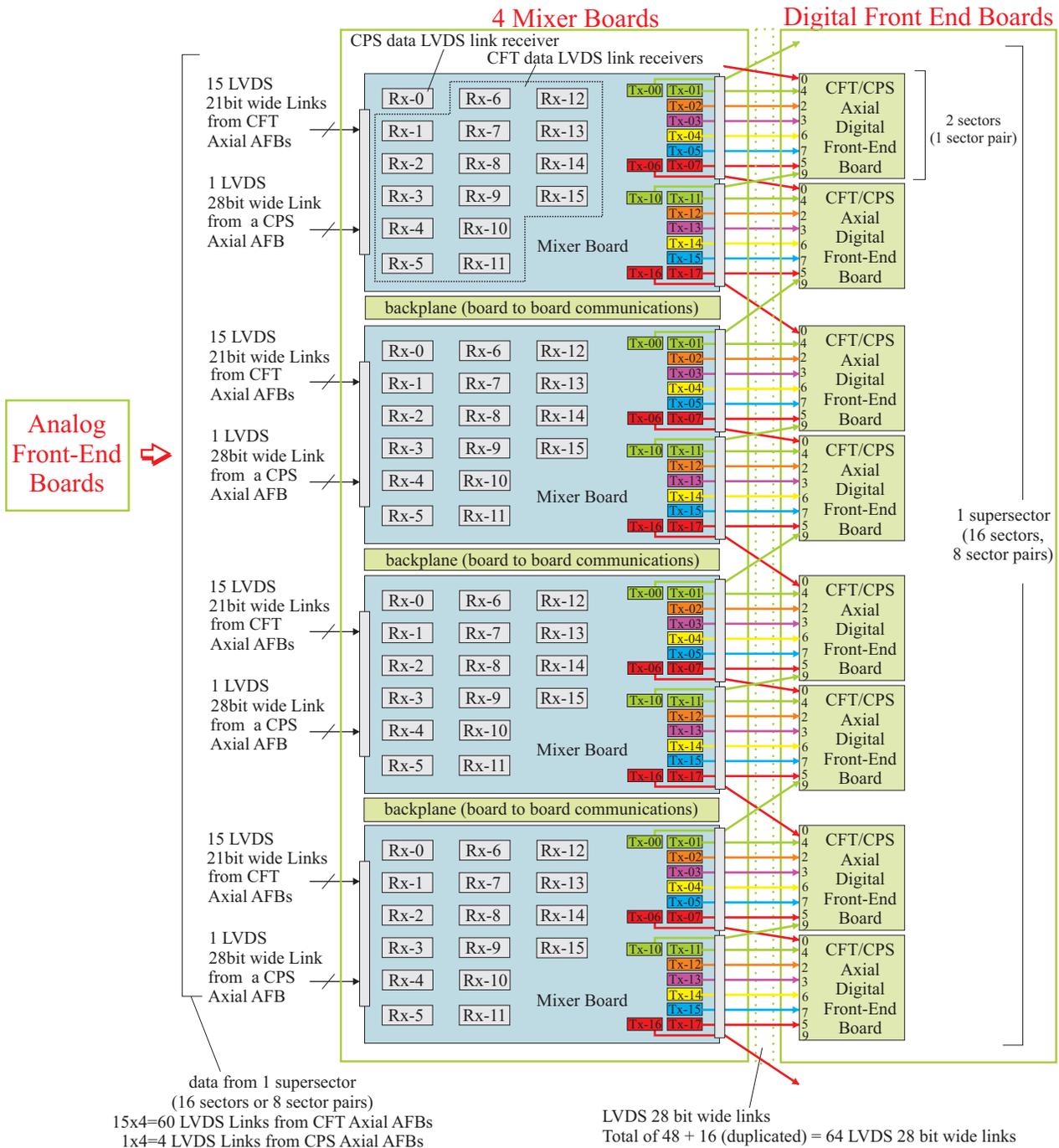
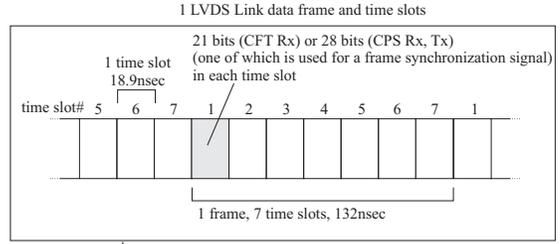
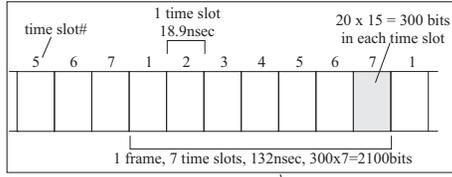


Figure 3.2, Supersector data flow.

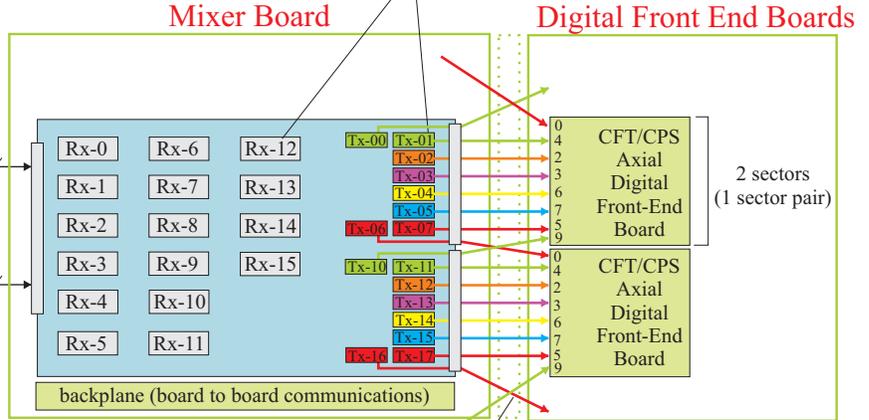
15 LVDS Links (21 bit wide) data frame and time slots from CFT AFBs
 one bit of each link is used for a frame synchronization signal.
 Total CFT data frame size to a mixer board: 20bits x 7 clocks x 15links = 2100bits
 Total # of CFT data bits allocated in a frame (data from 4 sectors CFT fibers) = 4 sectors x 480bits = 1920bits



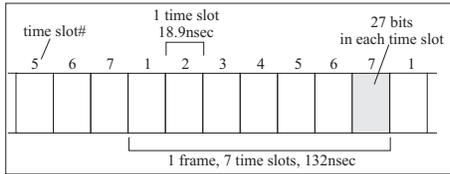
Analog Front-End Boards

data from 4 sectors (2 sector pairs)

15 LVDS 21bit wide Links from CFT Axial AFBs
 1 LVDS 28bit wide Link from a CPS Axial AFB



1 LVDS Link (28 bit wide) data frame and time slots from CPS AFBs
 one bit of the link is used for frame synchronization signal.
 CPS data frame size: 27bits x 7 clocks = 189bits
 CPS data bits allocated in a frame (data from 4 sectors CPS fibers): 4sectors x 32bits = 128bits



12 + 4 (duplicates) LVDS Links (28 bit wide)
 one bit in each link is used for a frame synchronization signal
 Data frame size: 27 bits x 7 clocks x 12 links = 2268bits
 Duplicates data frame size: 27 bits x 7 clocks x 4 links = 756 duplicated bits
 Data bits allocated in a data frame: (data from 4 sectors CFT&CPS fibers) = 4 sectors x 512 bits = 2048 bits

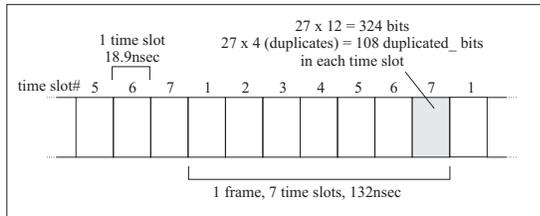


Figure 3.3, Mixer Board data flow.

3.3 Data frame structure and timing

The data of a specific particle interaction event (or bunch crossing) is received and sent by the Mixer System over seven 53MHz clock cycles or seven "time slots", this group of seven time slots defines a "data frame". In order to separate data from different bunch crossings a frame synchronization signal is needed.

The Analog Front-End board (AFE) has a signal derived from the 7.6 MHz bunch crossing clock called LD_SHFT. The equivalent signal on the Mixer System is called SYNC. The AFE sends this signal to the Mixer System on the **Least Significant bit (LSb)** of each LVDS link.

The Mixer System is expecting the SYNC signal to be high in the last time slot of each frame. Figure 3.4 shows the default frame structure at the output of the Mixer board LVDS receivers.

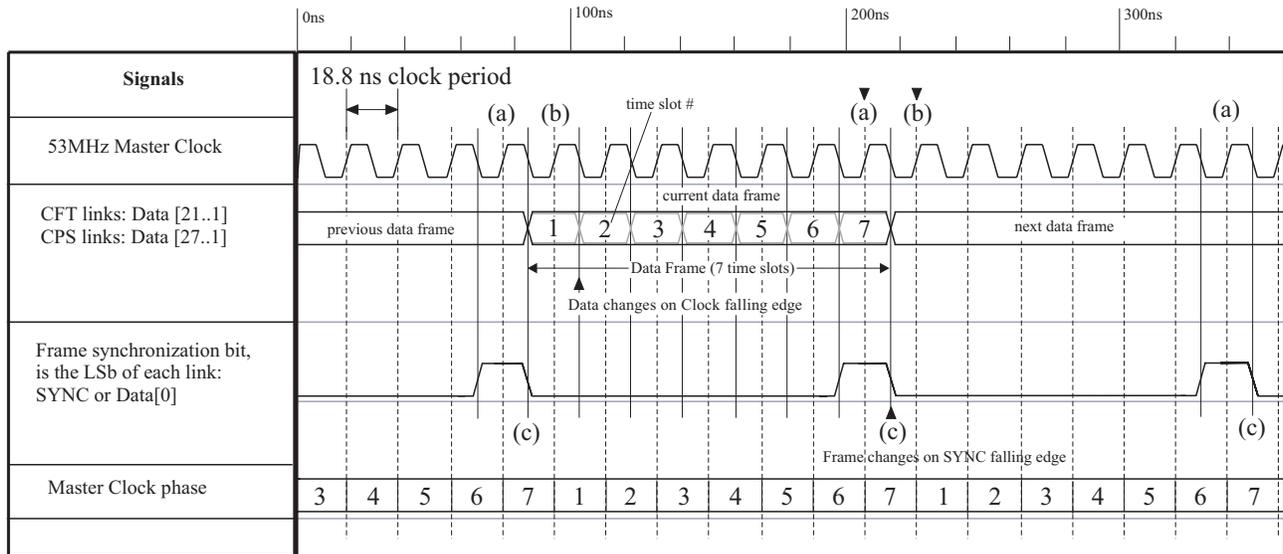


Figure 3.4, Master clock, data timing and frame structure at the output of the LVDS receivers

The correct SYNC timing is critical to the functioning of the mixer system. The position of the SYNC bit lets the mixer logic know at each clock tick (or time slot) which data bits are being received and how they should be reorganized to generate the output links data stream.

The SYNC bit is regenerated by each mixer board and used as a frame marker for the output data stream sent by the Mixer System to the Digital Front-End boards. The SYNC bit for the input LVDS links from the AFEs and the output LVDS links to the DFEs is located on the least significant bit and is high in the last time slot of a data frame.

3.4 Mixer Board Block Diagram

The mixer board can be logically partitioned in several logic blocks (see Figure 3.5):

a) LVDS receivers.

There are sixteen LVDS SERDES (serializer/deserializer) receivers on a mixer board. Fifteen receivers (link#1 to 15) are of the 21 bit wide type; they use the Texas Instrument SN65LVDS96 chip. One of the receiver (link#0) is of the 28 bit wide type and use the SN65LVDS94 chip. The output and the synthesized clock of the LVDS receivers is send to the Front-End FPGAs.

b) Front-End FPGAs.

There are six Xilinx Virtex 50 series FPGAs used to receive the data and clocks from the input links. Five FPGAs handle the data of three links each, one FPGA handle only the data of link#0. The FPGAs logic performs diagnostic functions like clock and frame synchronization (SYNC bit) detection, but its main purpose is the input links data synchronization to a "global clock". After the data is synchronized it is sent to the Back-End FPGAs and the Backplane FPGAs that perform the data reorganization in "trigger sectors". The Front-End FPGA handling the data from link#0 also perform the function of collecting the control bits from all input links and using them to generate the two "Embedded Command Bits" which are forwarded to four Back-End FPGA and inserted in some of the output links data streams.

b) Interconnection Matrix.

The interconnection matrix is made by all the connections used to forward the data from the Front-End FPGAs to the Back-End and Backplane FPGAs. The interconnection matrix is hardwired in the mixer printed circuit board and cannot be changed. The mixer board can be considered a custom digital data switch. The custom design allowed the designer to minimize the number of interconnections, fit the design in tight mechanical constraints, and to use quad flat packages for the FPGAs. One level of design complexity was added because of the requirement of having a unique mixer board design that fitted four different firmware versions, one for each of the four boards (mixer subsystem) handling the data from a supersector. The unpleasant side of a custom design is the very limited flexibility and this is particularly true for the mixer system. Minimal changes in the system specification may demand a different interconnection matrix that will require redesigning the printed circuit board.

c) Backplane FPGAs.

Four Xilinx Virtex 50 series FPGAs are used to handle the data exchange with the adjacent mixer boards inside a mixers subsystem. Two FPGAs are used as "backplane drivers", one to send data to the board to the right and one for the board to the left. The two other FPGAs are used as "backplane receivers". Both receive the same data and each of them handle the data for a different "sector pair". This mean that each of the backplane receivers forward the received data to only three of the six Back-End FPGAs.

d) Back-End FPGAs.

There are six Xilinx Spartan 40XL series FPGAs used to reorganize the data before sending it to the output link's LDVS transmitters. They can be divided in two subsets of three FPGAs, each of them handling the data belonging to a different sector pair. These two subsets of chips will be often referred as DFE0 and DFE1 FPGAs or plain color FPGAs and striped color FPGAs. The four backplane FPGAs receive two Embedded Command Bits from the link#0 Front-End FPGA. These bits are inserted in some of the output data streams.

e) LVDS transmitters.

There are sixteen LVDS SERDES (serializer/deserializer) transmitters on a mixer board. All of them are of the 28 bit wide type and are the Texas Instrument SN65LVDS93. The data inputs of the LVDS transmitters are driven by the Back-End FPGAs. As for the Front-End FPGAs the transmitters can be divided in two subsets referred to as DFE0 (or plain color) and DFE1 (or striped color). The DFE0 transmitters and links are numbered from 00 to 07, the DFE1 ones are numbered from 10 to 17. The color naming of the transmitters and links refer to the color assigned to the "trigger sector" in a "sector pair". Each transmitter/link handle the data belonging to one trigger sector. The DFE boards need to share some of the data sent by the mixer system. This is achieved with the duplication of some of the output links. In each of the two subsets of 8 output links of a mixer board six links are unique and two of the links (green and red) are duplicates.

f) Control logic. One of the seventeen FPGAs on a mixer board is used as "board controller" and is automatically configured at power-up by an on board EEPROM. The board controller performs several functions:

- 1) Handles backplane communication with the subrack controller (slot 1 of the subrack).
Read/Write operations are supported on a data space of several 8 bit-wide "registers". The board controller manages the configuration data download (from the subrack controller) to the other sixteen FPGAs.
- 2) Acts as central point of collection of information on board status and control of board behavior.
- 3) Relays FPGAs communications from/to the subrack controller.

An important block of the control logic is the "clock controller". Unlike the board controller it is not an individual FPGA. It is instead hosted by one of the backplane FPGAs, the backplane right driver. The clock controller supervises the distribution of the frame synchronization signal (SYNC) and clock on the mixer board. In particular it decides which clock the mixer board should use as "global clock" and which frame synchronization signal should be used as "global SYNC". The leftmost board in a mixer subsystem (four boards handling the data from a supersector) is used as clock/SYNC "master" board; it distributes the clock/SYNC signals to the other three ("slave") boards in the subsystem. This allows for clock and frame synchronized operations and data exchange inside a mixer subsystem. The clock controller has the capability to detect the presence of the link#0 clock and the backplane clock. The local clock (53MHz on-board oscillator) is always available. The clock controller on a slave board will use the backplane clock as first choice, the link#0 clock as second choice and the local clock as third. The clock controller on a master board has only the last two options.

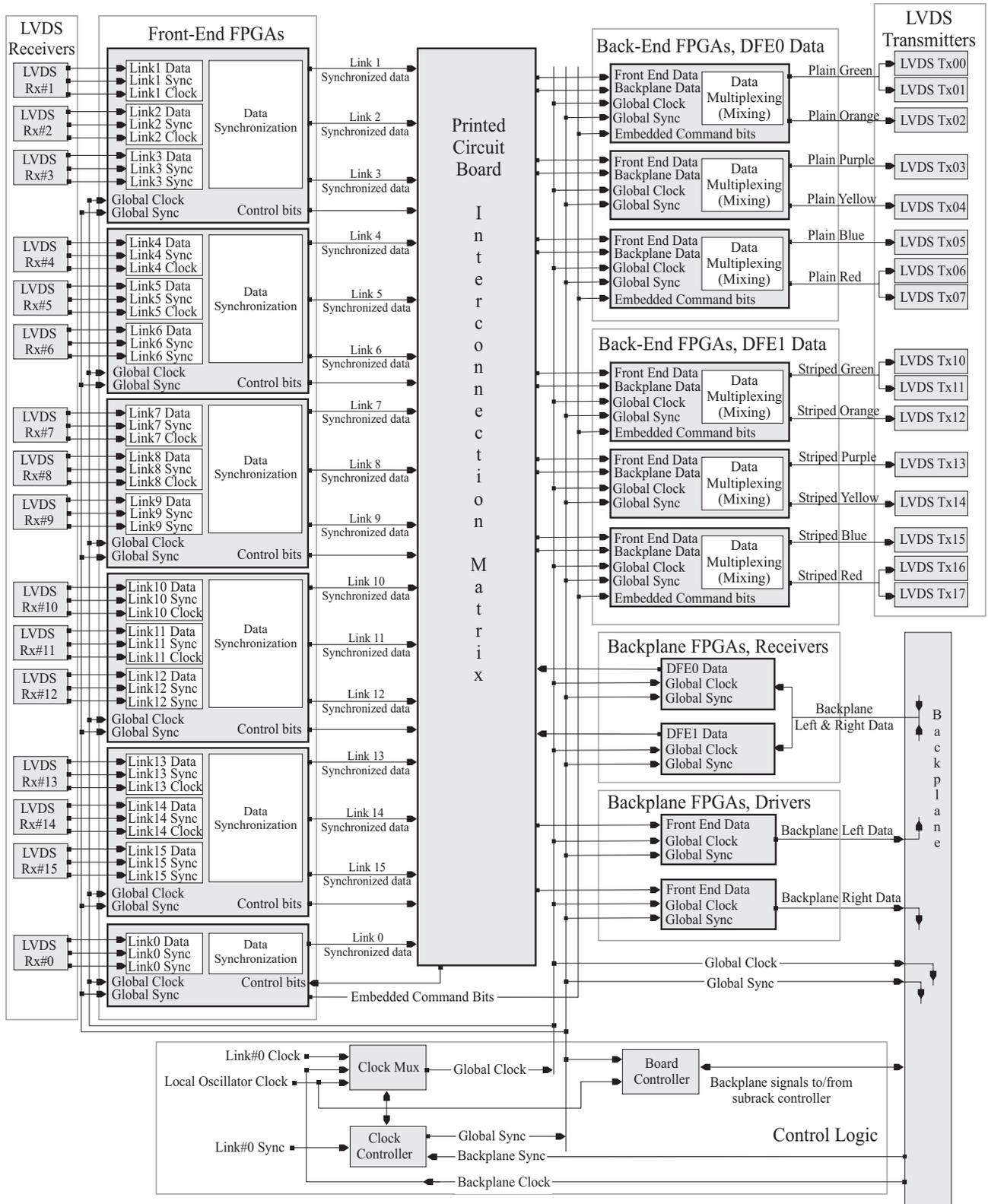


Figure 3.5, Mixer Board Block Diagram

4. Interfaces

4.1 LVDS Links Inputs from AFEs

The Mixer Board receives the data from the AFEs on two types of LVDS Links, 21 bits wide for the CFT fiber data and 28 bits wide for the CPS fiber data. On the 21 bit links the data is transmitted along four differential pair (three data and one clock), and on the 28 bit links the data is transmitted on five differential pair (four data and one clock). The Analog Front-End board uses the Texas Instrument serializers [Ref. 38] SN65LVDS95 and the SN65LVDS93 as transmitters and the Mixer Board uses the deserializers SN65LVDS96 and SN65LVDS94 as receivers which provide the 21 and 28 bits outputs of 3.3 V TTL data and clock.

The high-speed LVDS links interfacing the Analog Front End Boards with the Mixer System use 100 Ω controlled-impedance custom parallel cables. The front panel connectors are the AMP 1-1064-1 [Ref. 13] which have a 50 Ω single ended (signal to ground) and an 89 Ω differential (signal to signal) impedance.

Special care was taken on the Mixer Board design to ensure that the highest signal integrity was maintained. To achieve this, the board's impedance was controlled to 50 Ω single ended and 100 Ω differential for the high-speed LVDS serial connections. The board's impedance was controlled to 50 Ω for the slower parallel data. The quantity of vias was minimized and, when necessary, placed as close as possible to the device drivers. Since this is a combined serial and parallel interface, care was taken to control both impedance and trace length mismatch (board skew) [Ref. 38]. All traces from the connector to the receivers are as short as possible and matched in length. The 100 Ω LVDS interconnecting media is matched with a 100 Ω termination at the inputs of the receivers.

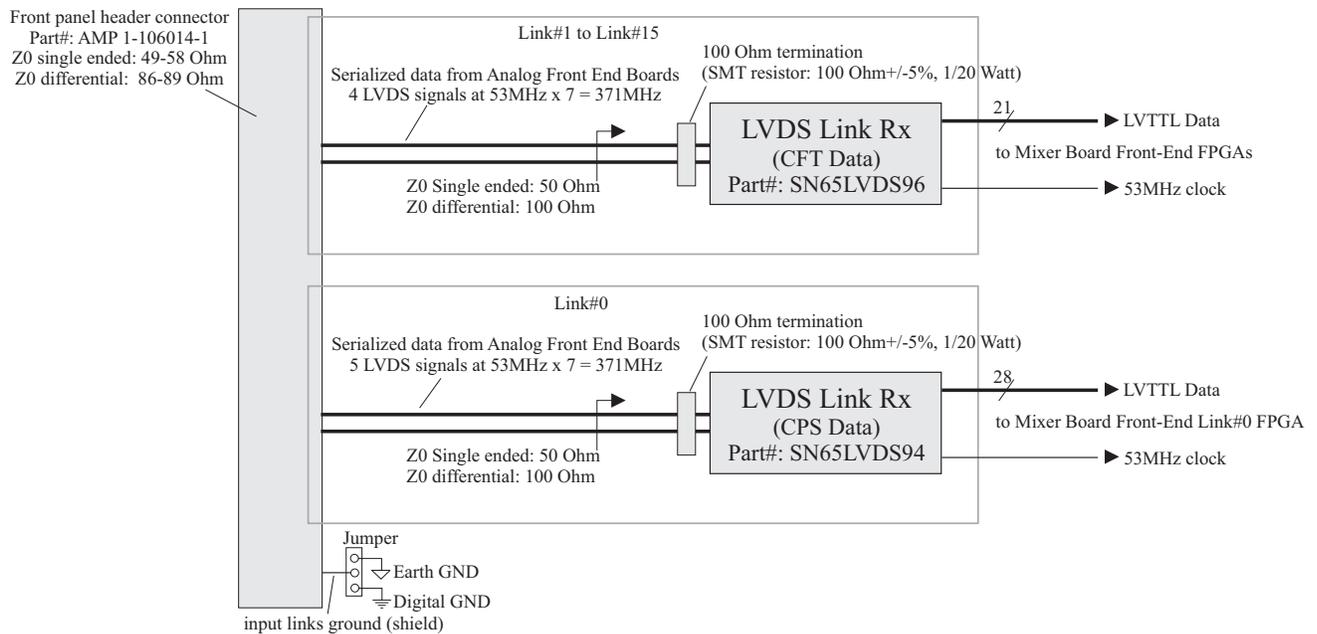


Figure 4.1, LVDS Input links logic block.

Table 4.1 shows the pinout of the input links front panel connector. Each input link has three differential signal pairs for data and one pair for the clock. Link #0 is an exception and has four differential pairs for data and one pair for the clock. On the LVDS cables the center column is connected to the cable shield. The center column of the board connector and all the pins labeled as "IS_GND" are connected to a copper pour that can be left floating, connected to the earth ground (front panel, chassis), or to the mixer board digital ground. The connection between the input links shield ground copper pour and the earth or digital ground can be done placing a solder bridge between two pads on the bottom front corner (solder side) of the mixer board (see Figure 12.1).

Link#	Pin #	Row 'a'	Row 'b'	Row 'c'	Row 'd'	Row 'e'
15	8	D1	/D1	IS_GND	D2	/D2
	7	/D0	D0	IS_GND	CLK	/CLK
14	6	D1	/D1	IS_GND	D2	/D2
	5	/D0	D0	IS_GND	CLK	/CLK
13	4	D1	/D1	IS_GND	D2	/D2
	3	/D0	D0	IS_GND	CLK	/CLK
12	2	D1	/D1	IS_GND	D2	/D2
	1	/D0	D0	IS_GND	CLK	/CLK
11	25	D1	/D1	IS_GND	D2	/D2
	24	/D0	D0	IS_GND	CLK	/CLK
10	23	D1	/D1	IS_GND	D2	/D2
	22	/D0	D0	IS_GND	CLK	/CLK
9	21	D1	/D1	IS_GND	D2	/D2
	20	/D0	D0	IS_GND	CLK	/CLK
8	19	D1	/D1	IS_GND	D2	/D2
	18	/D0	D0	IS_GND	CLK	/CLK
7	17	D1	/D1	IS_GND	D2	/D2
	16	/D0	D0	IS_GND	CLK	/CLK
6	15	D1	/D1	IS_GND	D2	/D2
	14	/D0	D0	IS_GND	CLK	/CLK
5	13	D1	/D1	IS_GND	D2	/D2
	12	/D0	D0	IS_GND	CLK	/CLK
4	11	D1	/D1	IS_GND	D2	/D2
	10	/D0	D0	IS_GND	CLK	/CLK
3	9	D1	/D1	IS_GND	D2	/D2
	8	/D0	D0	IS_GND	CLK	/CLK
2	7	D1	/D1	IS_GND	D2	/D2
	6	/D0	D0	IS_GND	CLK	/CLK
1	5	D1	/D1	IS_GND	D2	/D2
	4	/D0	D0	IS_GND	CLK	/CLK
0 (CPS)	3	D1	/D1	IS_GND	D2	/D2
	2	/D0	D0	IS_GND	CLK	/CLK
	1	IS_GND	IS_GND	IS_GND	D3	/D3

Table 4.1, Signal assignments for the LVDS inputs connector.

4.2 LVDS Links Outputs to DFEs

The Mixer Board sends the data to the DFE boards over sixteen 28 bit wide LVDS links. The data is transmitted along five differential pair (four data and one clock) on each link. The Mixer Board uses the Texas Instrument [Ref. 38] SN65LVDS93 serializers as transmitters which provide 28 bits of 3.3 V TTL data and clock outputs. The Digital Front-End Board uses the SN65LVDS94 deserializers as receivers.

As was done for the LVDS links' inputs, special care was taken on the Mixer Board design to ensure that the highest signal integrity is maintained on the LVDS outputs. All traces from the transmitters to the connector are as short as possible and matched in length.

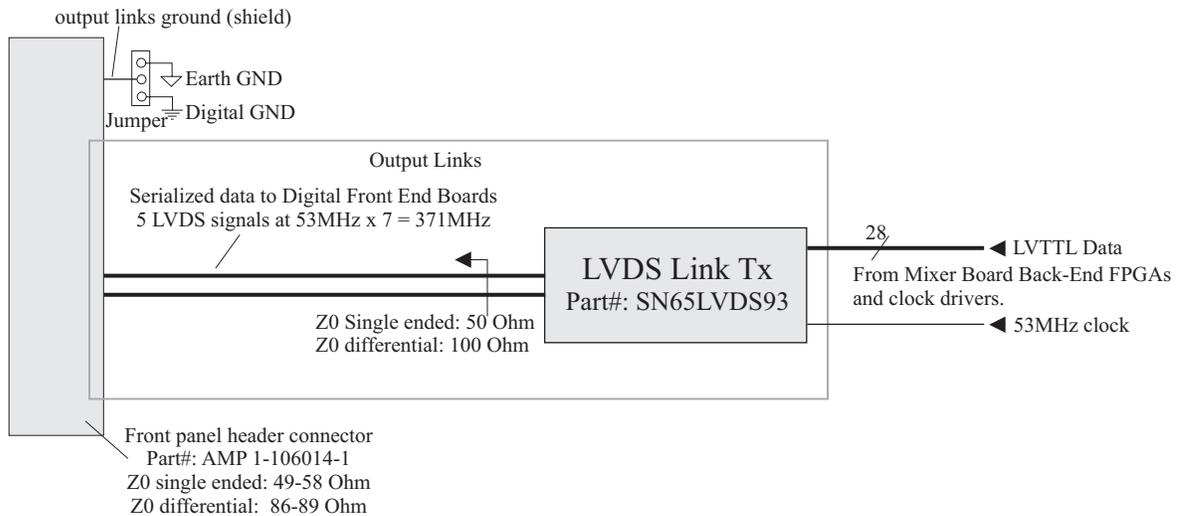


Figure 4.2, LVDS Output links logic block.

Table 4.2 shows the pinout of the output links' front panel connector. Each output link has four differential signal pairs for data and one differential signal pair for the clock. On the LVDS cables the center column of the connector is connected to the cable shield. The center column of the board connector and all the pins labeled as "OS_GND" are connected to a copper pour that can be left floating, connected to the earth ground (front panel, chassis), or can be connected to the mixer board digital ground. The connection between the output links shield ground copper pour and the earth or digital ground can be done by placing a solder bridge between two pads on the top front corner (solder side) of the mixer board (see Figure 12.1).

The top row of the connector was used in an "after manufacturing" hardware modification to allow front panel access to one of the two programmable logic JTAG chains. This modification allows reprogramming the board controller EEPROM without removing the board from the mixer subrack.

Link#	Color	Pin #	Row 'a'	Row 'b'	Row 'c'	Row 'd'	Row 'e'
Board Controller JTAG	N.A.	25	TMS	TCK	Board digital GND (JTAG cable shield)	TDI	TDO
17	Striped red (DFE1)	24	D1	/D1	OS_GND	D2	/D2
		23	/D0	D0	OS_GND	CLK	/CLK
		22	OS_GND	OS_GND	OS_GND	D3	/D3
16	Striped red (DFE1)	21	D1	/D1	OS_GND	D2	/D2
		20	/D0	D0	OS_GND	CLK	/CLK
		19	OS_GND	OS_GND	OS_GND	D3	/D3
15	Striped blue (DFE1)	18	D1	/D1	OS_GND	D2	/D2
		17	/D0	D0	OS_GND	CLK	/CLK
		16	OS_GND	OS_GND	OS_GND	D3	/D3
14	Striped yellow (DFE1)	15	D1	/D1	OS_GND	D2	/D2
		14	/D0	D0	OS_GND	CLK	/CLK
		13	OS_GND	OS_GND	OS_GND	D3	/D3
13	Striped purple (DFE1)	12	D1	/D1	OS_GND	D2	/D2
		11	/D0	D0	OS_GND	CLK	/CLK
		10	OS_GND	OS_GND	OS_GND	D3	/D3
12	Striped orange (DFE1)	9	D1	/D1	OS_GND	D2	/D2
		8	/D0	D0	OS_GND	CLK	/CLK
		7	OS_GND	OS_GND	OS_GND	D3	/D3
11	Striped green (DFE1)	6	D1	/D1	OS_GND	D2	/D2
		5	/D0	D0	OS_GND	CLK	/CLK
		4	OS_GND	OS_GND	OS_GND	D3	/D3
10	Striped green (DFE1)	3	D1	/D1	OS_GND	D2	/D2
		2	/D0	D0	OS_GND	CLK	/CLK
		1	OS_GND	OS_GND	OS_GND	D3	/D3
		25	OS_GND	OS_GND	OS_GND	OS_GND	OS_GND
07	Plain red (DFE0)	24	D1	/D1	OS_GND	D2	/D2
		23	/D0	D0	OS_GND	CLK	/CLK
		22	OS_GND	OS_GND	OS_GND	D3	/D3
06	Plain red (DFE0)	21	D1	/D1	OS_GND	D2	/D2
		20	/D0	D0	OS_GND	CLK	/CLK
		19	OS_GND	OS_GND	OS_GND	D3	/D3
05	Plain blue (DFE0)	18	D1	/D1	OS_GND	D2	/D2
		17	/D0	D0	OS_GND	CLK	/CLK
		16	OS_GND	OS_GND	OS_GND	D3	/D3
04	Plain yellow (DFE0)	15	D1	/D1	OS_GND	D2	/D2
		14	/D0	D0	OS_GND	CLK	/CLK
		13	OS_GND	OS_GND	OS_GND	D3	/D3
03	Plain purple (DFE0)	12	D1	/D1	OS_GND	D2	/D2
		11	/D0	D0	OS_GND	CLK	/CLK
		10	OS_GND	OS_GND	OS_GND	D3	/D3
02	Plain orange (DFE0)	9	D1	/D1	OS_GND	D2	/D2
		8	/D0	D0	OS_GND	CLK	/CLK
		7	OS_GND	OS_GND	OS_GND	D3	/D3
01	Plain green (DFE0)	6	D1	/D1	OS_GND	D2	/D2
		5	/D0	D0	OS_GND	CLK	/CLK
		4	OS_GND	OS_GND	OS_GND	D3	/D3
00	Plain green (DFE0)	3	D1	/D1	OS_GND	D2	/D2
		2	/D0	D0	OS_GND	CLK	/CLK
		1	OS_GND	OS_GND	OS_GND	D3	/D3

Table 4.2, Signal assignments for the LVDS outputs connector.

4.3 LVDS Cabling

The high-speed LVDS links interfacing the Analog Front End Boards with the Mixer System and the Mixer System with Digital Front End Boards use differential pairs parallel custom cables having 100 Ω differential impedance. These cables are terminated with lead assemblies to connect to the Mixer Board front panel connectors. The Mixer Board front panel connectors have a 50 Ω single ended (signal to ground) and an 89 Ω differential (signal to signal) impedance.

Cable characteristics:

Individually Shielded Twisted Pairs.

Signal and drain conductor size: 28 AWG

Propagation delay: 1.3 ns/ft [4.265 ns/m]

Propagation Velocity: 0.769 ft/ns [0.234 m/ns]

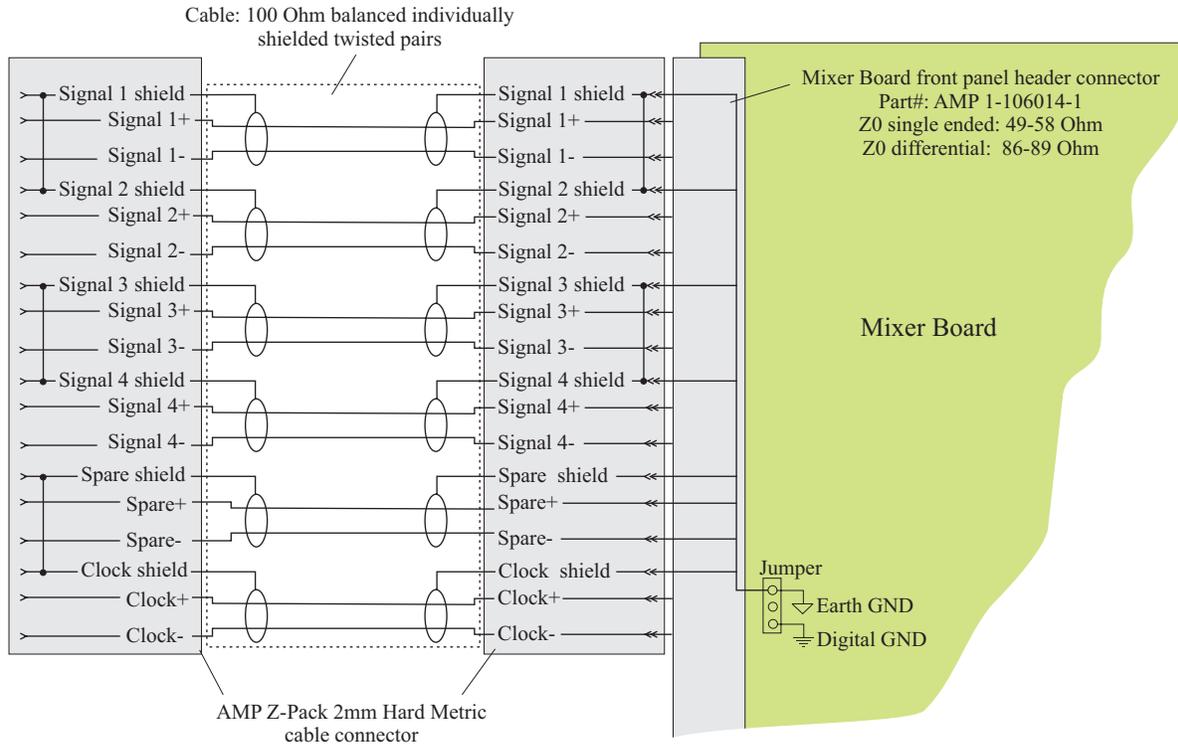


Figure 4.3, LVDS cabling for a 28 bit wide link.

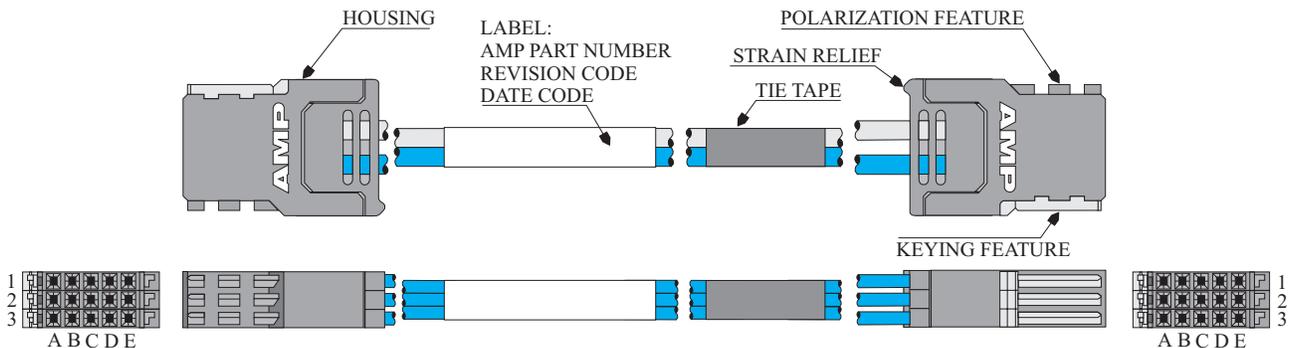


Figure 4.4, 28 bit link (3x5) LVDS cable.

4.4 Mixer System Backplane

The D0 Mixer System Backplane was developed as an interconnect and power distribution bus for the D0 Mixer Board set. It resembles the VME J1/J2 backplane form, but does not adhere to VME backplane specifications.

The mechanical and electrical specifications are available in separate documents [**Ref. 8**].

Figure 4.5 shows a sketch of the mixer system backplane.

The backplane supports the following interfaces:

Subrack controller general-purpose bus interface.

Used for configuration download and for remote access to the mixer boards. More details on the bus in paragraph 4.5 (page 29). More information about the Subrack Controller is provided in Paragraph 14.1 (page 139) and in a separate document [**Ref. 5e**].

Subrack controller slow monitoring serial bus interface.

During data acquisition, due to the proximity of the mixer system to detector components, noise considerations suggested avoiding accessing the mixer system over the "general purpose bus interface". The slow monitoring serial bus provides a way to readback status information from the mixer boards. More details in paragraph 4.6 (page 47).

Subrack controller 1553 interface.

The subrack controller is remotely accessible through a MIL-STD-1553 serial bus. The MIL-STD-1553 is a networking standard used for integration of military platforms [**Ref. 42**]. The backplane hosts the two 1553 triaxial connectors needed by the subrack controller to implement the 1553 interface.

Board to board buses.

Mixer boards need to exchange part of the data they receive over the LVDS input links with the adjacent boards belonging to the same mixer subsystem (four boards). This is accomplished with two LVTTTL parallel buses 41 bit wide, one to the next backplane slot to the left and one to the next backplane slot to the right.

Timing signals distribution

In a mixer subsystem (group of four boards), the leftmost board is used as "master" for distribution of global clock and global SYNC signals to the other three boards (slaves). The clock is distributed over three (one for each slave board) point-to-point LVDS connections. The SYNC is distributed over three point-to-point LVTTTL connections.

Power supply.

A mixer board is powered through a backplane connection to the 3.3Volts 240 Ampere subrack power supply. A small brick power supply is used to provide 5 Volts power needed by the subrack controller (slot 1). Two green LEDs, one for each supply voltage are on when the backplane is powered. Three polyfuses are used as over-current protection. Each mixer board has its own over-current/over-voltage protection.

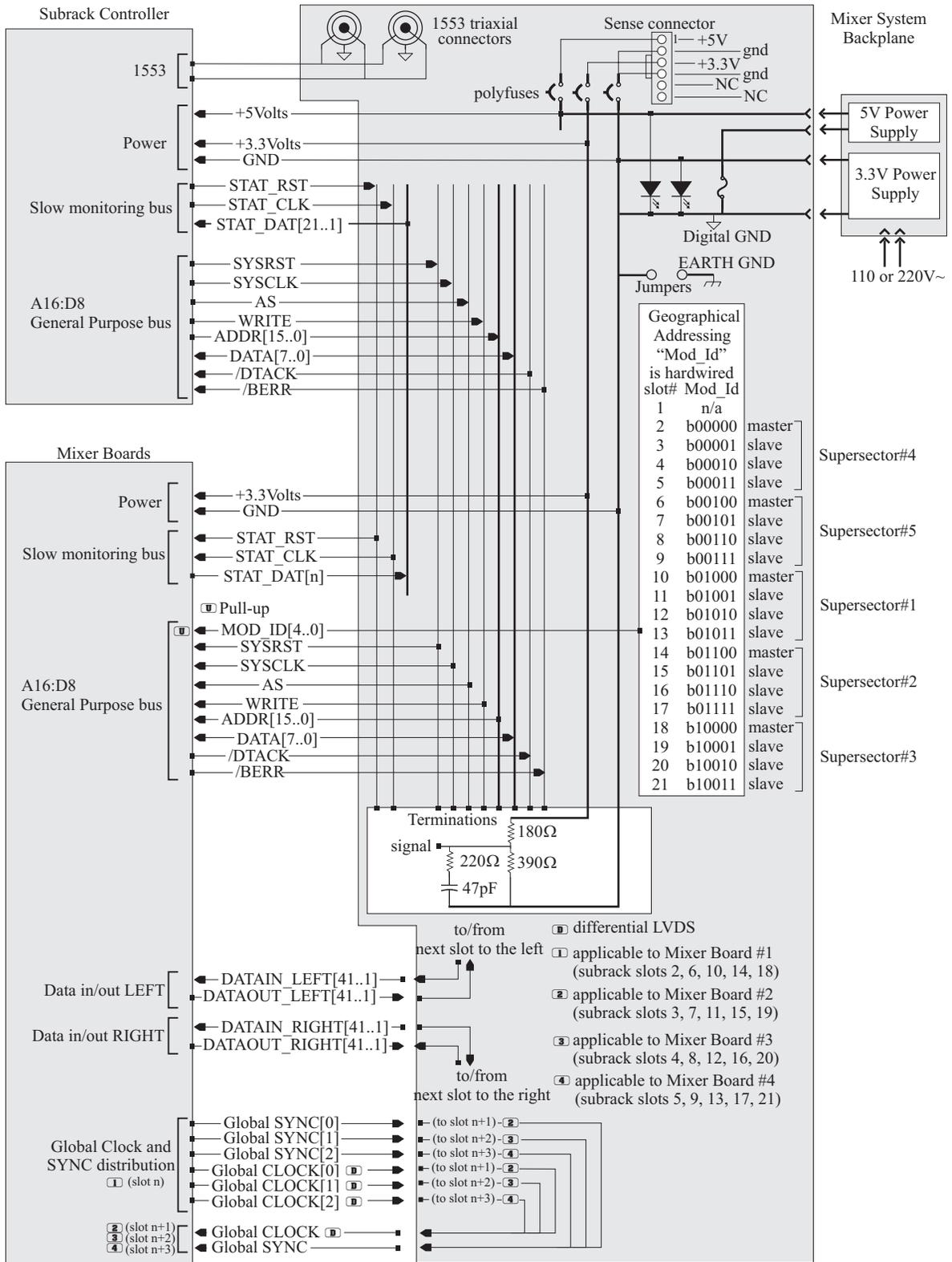


Figure 4.5, Mixer System backplane

4.5 Mixer Board - Subrack Controller General Purpose Bus interface

A general-purpose address/data bus connects the 20 Mixer Boards to the Subrack Controller. The bus has 16 address and 8 data bits. The Subrack Controller is the same used for Digital Front End Subrack [Ref. 5]. Each slot in the Mixer System Subrack is uniquely identified by the 5 bits address provided in Table 4.3. The address bits are hardwired into the backplane (Geographical Addressing) using 5 bits (MOD_ID) allowing each board to be addressed by its location in the subrack.

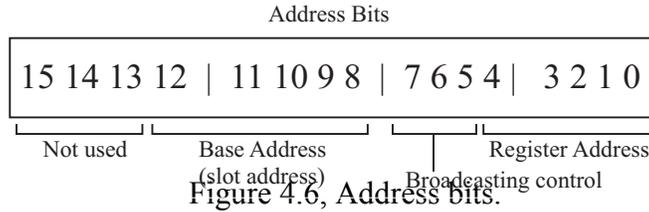


Figure 4.6, Address bits.

Slot #	Base Address	Slot MOD_ID	Mixer Board #	Supersector #	Notes [DFE subrack name and slot# on the D0 detector platform]
1	n/a	n/a	-	-	Subrack Controller slot.
2	0x02	b00000	1	4 (Sectors #1, 2)	Master slot. Feeds DFE #0 [PC03-3 Slot2], DFE#1 [PC03-3 Slot3].
3	0x03	b00001	2	4 (Sectors #3, 4)	Slave slot. Feeds DFE #2 [PC03-3 Slot4], DFE#3 [PC03-3 Slot5].
4	0x04	b00010	3	4 (Sectors #5, 6)	Slave slot. Feeds DFE #4 [PC03-3 Slot6], DFE#5 [PC03-3 Slot7].
5	0x05	b00011	4	4 (Sectors #7, 8)	Slave slot. Feeds DFE #6 [PC03-3 Slot8], DFE#7 [PC03-3 Slot9].
6	0x06	b00100	1	5 (Sectors #1, 2)	Master slot. Feeds DFE #8 [PC03-3 Slot10], DFE#9 [PC03-3 Slot11].
7	0x07	b00101	2	5 (Sectors #3, 4)	Slave slot. Feeds DFE #10 [PC03-3 Slot12], DFE#11 [PC03-3 Slot13].
8	0x08	b00110	3	5 (Sectors #5, 6)	Slave slot. Feeds DFE #12 [PC03-3 Slot14], DFE#13 [PC03-3 Slot15].
9	0x09	b00111	4	5 (Sectors #7, 8)	Slave slot. Feeds DFE #14 [PC03-3 Slot16], DFE#15 [PC03-3 Slot17].
10	0x0A	b01000	1	1 (Sectors #1, 2)	Master slot. Feeds DFE #16 [PC03-3 Slot18], DFE#17 [PC03-3 Slot19].
11	0x0B	b01001	2	1 (Sectors #3, 4)	Slave slot. Feeds DFE #18 [PC03-3 Slot20], DFE#19 [PC03-3 Slot21].
12	0x0C	b01010	3	1 (Sectors #5, 6)	Slave slot. Feeds DFE #20 [PC03-2 Slot2], DFE#21 [PC03-2 Slot3].
13	0x0D	b01011	4	1 (Sectors #7, 8)	Slave slot. Feeds DFE #22 [PC03-2 Slot4], DFE#23 [PC03-2 Slot5].
14	0x0E	b01100	1	2 (Sectors #1, 2)	Master slot. Feeds DFE #24 [PC03-2 Slot6], DFE#25 [PC03-2 Slot7].
15	0x0F	b01101	2	2 (Sectors #3, 4)	Slave slot. Feeds DFE #26 [PC03-2 Slot8], DFE#27 [PC03-2 Slot9].
16	0x10	b01110	3	2 (Sectors #5, 6)	Slave slot. Feeds DFE #28 [PC03-2 Slot10], DFE#29 [PC03-2 Slot11].
17	0x11	b01111	4	2 (Sectors #7, 8)	Slave slot. Feeds DFE #30 [PC03-2 Slot12], DFE#31 [PC03-2 Slot13].
18	0x12	b10000	1	3 (Sectors #1, 2)	Master slot. Feeds DFE #32 [PC03-2 Slot14], DFE#33 [PC03-2 Slot15].
19	0x13	b10001	2	3 (Sectors #3, 4)	Slave slot. Feeds DFE #34 [PC03-2 Slot16], DFE#35 [PC03-2 Slot17].
20	0x14	b10010	3	3 (Sectors #5, 6)	Slave slot. Feeds DFE #36 [PC03-2 Slot18], DFE#37 [PC03-2 Slot19].
21	0x15	b10011	4	3 (Sectors #7, 8)	Slave slot. Feeds DFE #38 [PC03-2 Slot20], DFE#39 [PC03-2 Slot21].

Table 4.3, Mixer System Subrack slot addressing

All signals used in the Subrack Controller General Purpose Bus interface are pulled to a logic high level on the backplane (see block "termination" in Figure 4.5).

The following description of the backplane General Purpose Bus protocol is partially derived and compliant with specifications in [Ref. 5c].

4.5.1 Bus Signals

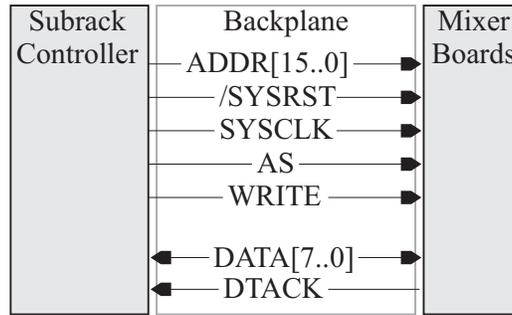


Figure 4.7, General Purpose Bus signals.

The Bus protocol is a simplification of a VME A16D8 bus [Ref. 3].

Signal	
ADDR[15..0]	16 bit Address bus. ADDR[15..13] unused ADDR[12..8] Base address (slot address) ADDR[7..5] Broadcasting control (write operations only) "000" normal addressing (one board at the time) "001" Subsystem/Super Sector Broadcasting (all board belonging to the Subsystem/Super Sector) "010" Mixer Board # Broadcasting (all boards having the same position in the five Subsystems/Super Sectors) "100" Subrack broadcasting (all boards) Any other set is not recognized (boards will not respond). ADDR[4..0] Register address
/SYSRST	Active low signal. Force all the Mixer boards in a power-up reset state if asserted for more then 2 seconds. NOT IMPLEMENTED.
SYSCLK	Free running clock with a maximum frequency of 12 MHz. Can be shut down by the subrack controller.
AS	Address Valid signal. Indicate that the address on the bus is valid on the next rising edge of SYSCLK.
WRITE	Active high (controller writing data to a Mixer Board).
DATA[7..0]	8 bit Data bus.
/DTACK	Data Transfer Acknowledge. Active low, open drain signal.
/BERR	Bus Error. Active low, open drain signal. NOT IMPLEMENTED.

Table 4.4, General Purpose Bus signals.

The Subrack Controller general purpose A16:D8 bus is synchronous, all the signals are registered using SYSCLK. To comply with timing specifications the logic on the mixer board uses both the rising and the falling edge of SYSCLK to register signals.

4.5.2 Write and Read Cycles

The mixer board latches the address and data lines on the rising edge of SYSCLK when the Address Strobe (AS) signal is high. The address is then compared with the geographical address of the board. For write operations, the address comparison will take into account the content of the value of the three bits (ADDR[7..5]) used for broadcasting operations (see Table 4.4). If the address is recognized as valid (i.e. as belonging to the board addressable space) the mixer board will respond on the next SYSCLK falling edge driving the Data Transfer Acknowledge (DTACK) signal low for one clock cycle. During broadcasting operations every board addressed by the broadcast will respond.

The mixer board addressable space is larger than the actual space used for data registers, and some of the data registers and register bits are read-only. The write operation will have an effect only if the data register addressed exists inside the addressable space, and only on the bits of this register which are writable.

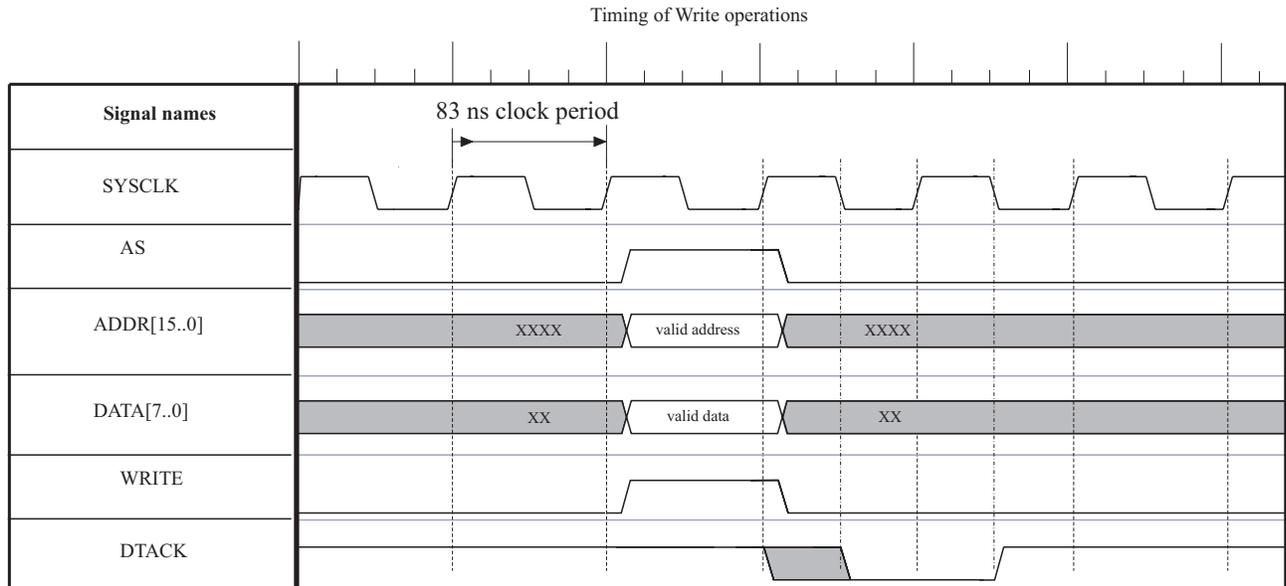


Figure 4.8, Write operation timing

For read operations the data is made available for the duration of one clock cycle on the first SYSCLK falling edge after a valid address has been received. At the same time, and still for one clock cycle the board will pull down the Data Transfer Acknowledge. Read operations to parts of the addressable space that is not implemented will return invalid data. Read operation addressing vacant subrack slots will return 0x00. Read operations do not support broadcasting.

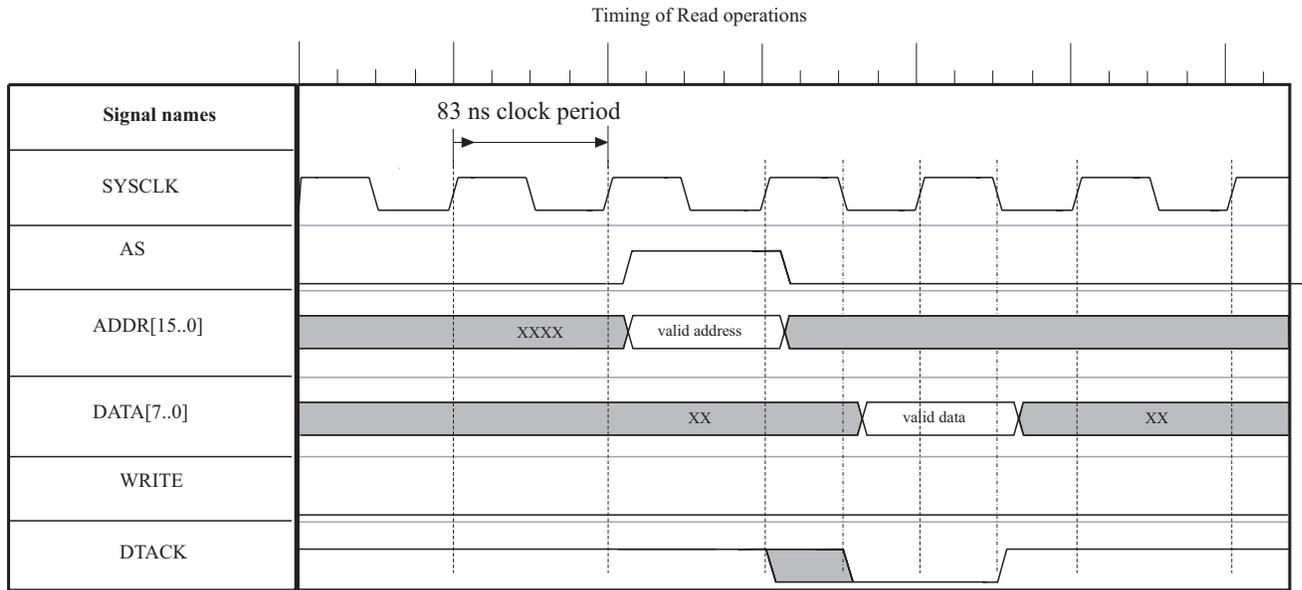


Figure 4.9, Read operation timing

4.5.3 Data Space Description

The Mixer Board provides 32 8-bit wide register locations in data space as described in the following subsections. Some register locations of the data space are not currently implemented. Table 4.5 shows the data space address map. The following description of the data space is in part derived from [Ref.5a].

Register	Access	Register Address (5 bits)
(0) Board Status/Control register	Read/Write	0x00
(1) Device Status Control register	Read/Write	0x01
(2) Device Configuration Data register ☼	Read/Write	0x02
(3) Device Firmware ID register	Read/Write	0x03
(4) Mode of Operation register	Read/Write	0x04
(5) Input Links Error Status Low register	Read	0x05
(6) Input Links Error Status High register	Read	0x06
(7) Device Access-Address register ☼	Read/Write	0x07
(8) Device Access-Data register ☼	Read/Write	0x08
(9) DFE0 Output Links (00, 01, 02, 03, 04, 05, 06, 07) Test Mode register	Read/Write	0x09
(10) DFE1 Output Links (10, 11, 12, 13, 14, 15, 16, 17) Test Mode register	Read/Write	0x0A
(11) Monitoring Mode register	Read/Write	0x0B
(12) Monitoring Status Low (Green LEDs 0..7) register	Read	0x0C
(13) Monitoring Status High (Green LEDs 8..15) register	Read	0x0D
(14) Monitoring Status Low History (Green LEDs 0..7) register	Read	0x0E
(15) Monitoring Status High History (Green LEDs 8..15) register	Read	0x0F
(16) Board Status/Control register B	Read/Write	0x10
(17) FIFO Trigger Control register	Read/Write	0x11
(18 to 21) -- not implemented --	--	0x20..0x15
(23) MMode Control	Read/Write	0x16
(23) MMode GL	Read/Write	0x17
(24) MMode GH	Read/Write	0x18
(25) MMode RL	Read/Write	0x19
(26) MMode RH	Read/Write	0x1A
(27) Read/Write Test register	Read/Write	0x1B
(28) Firmware revision date DAY register	Read	0x1C
(29) Firmware revision date MONTH register	Read	0x1D
(30) Firmware revision date YEAR register	Read	0x1E
(31) Board serial number register	Read	0x1F

☼ writing operations need to be enabled through setting the appropriate bit in the Mode of Operation register.

Table 4.5, Data space address map.

4.5.4 Board Status/Control register

Relative address 0x00 (5 bits) is the Board Status/Control register, a read/write register.

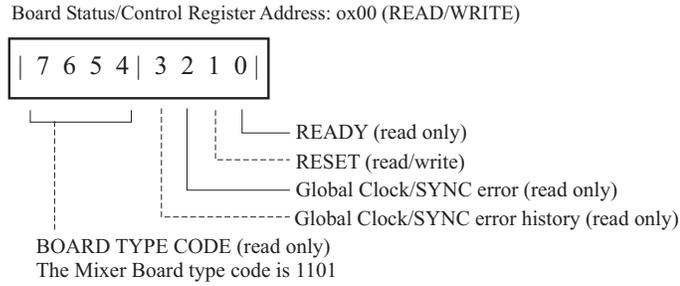


Figure 4.10, Board Status/Control Register.

Bit#	Name (Type)	Interpretation
7..4	BOARD TYPE CODE	(read only) Used by the DAQ system to recognize the type of board. The mixer board type is "b1101" or "0xD".
3	Global Clock/SYNC Error history	(read only) Latched version of Global Clock/SYNC Error. It is reset to '0' thorough the Board Status/Control register B (0x10). The bit is not cleared by a board reset because of the time taken by the clock controller logic to re-establish normal operations after a board reset. The bit is reset by writing to the appropriate bit in the "Board Status/Control register B" (0x10).
2	Global Clock/SYNC Error	(read only) The mixer board automatically chooses most appropriate clock to be used, but for correct operations the mixer subsystem master boards must use the link#0 clock and the mixer subsystem slave boards must use the backplane clock. Furthermore, the link#0 SYNC on the master boards and the backplane SYNC on the slave boards must respect the correct protocol (one and only one high pulse in a seven clock cycles wide window). If these conditions are not satisfied the Global Clock/SYNC Error bit is set.
1	RESET	(read/write) Writing a "1" will force the board to be reset and to stay in the reset status till the bit is deasserted. Reset will not cause devices to lose their configuration. Reset should be "0" while devices are configured.
0	READY	(read only) This bit is set if all devices are configured.

Table 4.6, Board Status/Control Register.

4.5.5 Device Status/Control register

Relative address 0x01 (5 bits) is the Device Status/Control register, a read/write register. This register allows setting a pointer to one of sixteen FPGAs on the mixer board (not including the board controller). This pointer is used during device configuration together with the Device Configuration Data register. The pointer is also used in the device access structure (see 4.5.12) to perform read/write operations on registers located inside the FPGAs. This register allow the user to erase/verify devices configuration.

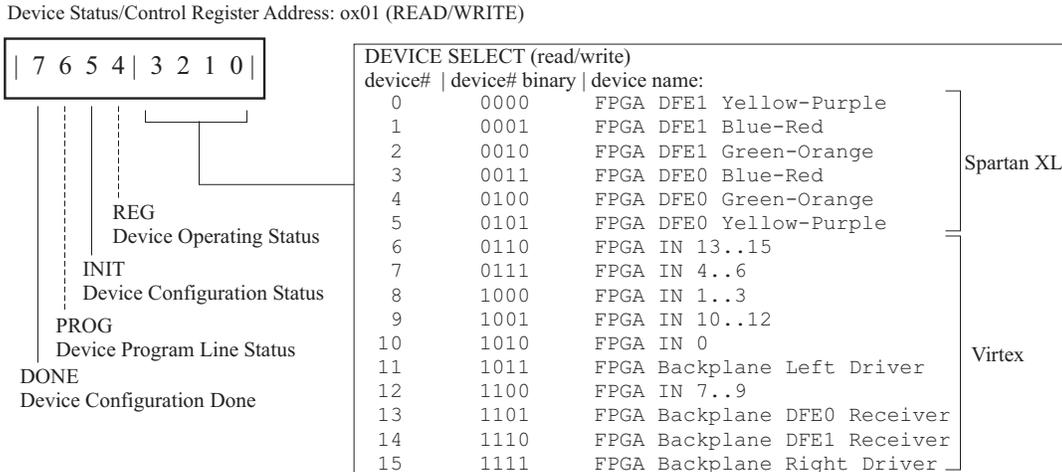


Figure 4.11, Device Status/Control Register.

Bit#	Name (Type)	Interpretation
7	DONE	(Read only) Goes high when the selected device (through DEVICE SELECT bits) has received all its configuration data.
6	PROG	(read/write) Used to assert the Mixer Board program bit. Each FPGA has its own program bit. The bit PROG on device #0 (the first device in the programming chain, is Back-End FPGA DFE1 Yellow-Purple) is used to force all the 16 devices of the Mixer Board to erase their configuration memories and preparing to accept new configuration data. This is achieved in two steps: <ul style="list-style-type: none"> a) Writing a '1' will erase the configuration memories of all 16 devices/FPGAs, b) Writing a '0' will make the devices/FPGAs available to receive configuration data. When all devices are configured this bit is no longer accessible for writing unless the appropriate bit is set in the Mode of Operation Register. This is a protection feature to prevent mistakenly erasing the devices configuration memories.
5	INIT	(Read only) NOT IMPLEMENTED. Read back always '1'.
4	REG	(read only) NOT IMPLEMENTED. Read back always '0'.

3..0	DEVICE SELECT	(Read/Write) Allow selection of one of the 16 Mixer Board's devices: b0000 (0x0) [Device#0] Back End FPGA DFE1 Yellow Purple b0001 (0x1) [Device#1] Back End FPGA DFE1 Blue Red b0010 (0x2) [Device#2] Back End FPGA DFE1 Green Orange b0011 (0x3) [Device#3] Back End FPGA DFE0 Blue Red b0100 (0x4) [Device#4] Back End FPGA DFE0 Green Orange b0101 (0x5) [Device#5] Back End FPGA DFE0 Yellow Purple b0110 (0x6) [Device#6] Front End FPGA Input Links #13..15 b0111 (0x7) [Device#7] Front End FPGA Input Links #4..6 b1000 (0x8) [Device#8] Front End FPGA Input Links #1..3 b1001 (0x9) [Device#9] Front End FPGA Input Links #10..12 b1010 (0xA) [Device#10] Front End FPGA Input Link #0 b1011 (0xB) [Device#11] Back End FPGA Backplane Left Driver b1100 (0xC) [Device#12] Front End FPGA Input Links #7..9 b1101 (0xD) [Device#13] Back End FPGA Backplane DFE0 Receiver b1110 (0xE) [Device#14] Back End FPGA Backplane DFE1 Receiver b1111 (0xF) [Device#15] Back End FPGA Backplane Right Driver
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Table 4.7, Device Status/Control Register.

4.5.6 Device Configuration Data register

Relative address 0x02 (5 bits) is the Device Configuration Data register, a read/write register.

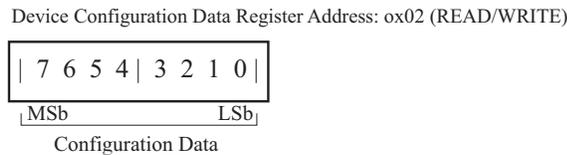


Figure 4.12, Device Configuration Data Register

Configuration data bytes are written to this register. Bit 7 is the most significant bit (MSb) and bit 0 is the Least Significant bit (LSb). The board controller will route the configuration data to the device selected as "current device" using the Device Status/Control register. Device configurations is lost if the board is powered down or the PROG bit of the Device Status/Control Register is set high for device#0 (Back-End FPGA DFE1 Yellow-Purple). When all devices are configured, the Device Configuration Register is no longer accessible for writing unless the appropriate bit is set in the Mode of Operation Register.

4.5.7 Device Firmware ID register

Relative address 0x03 (5 bits) is the Device Firmware ID register, a read/write register.

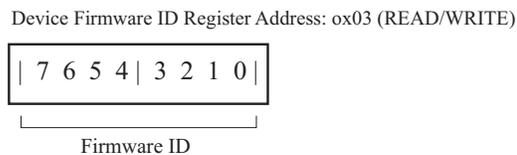


Figure 4.13, Firmware ID Register.

This register is used to store the firmware id assigned to each of the fifteen devices during the configuration process. This register provides the firmware id of the device pointed to by the Device

Status/Control Register. The firmware id is specified in the "Configure Device" DFE Controller command used to download the configuration file to each FPGA. The only time when this register is writable is when the device is not configured (DONE signal low).

The device firmware id information, as is devices configuration, is lost if the board is powered down or if the PROG bit of the Device Status/Control register is set high for device#0.

Bit#	Name (Type)	Interpretation
7..0	Device Firmware ID	ID byte assigned to the device when it was configured. It can only be written before the configuration process when the device is not yet configured. After device configuration the register is read only.

Table 4.8, Device Firmware ID Register.

4.5.8 Mode of Operation register

Relative address 0x04 (5 bits) is the Mode of Operation register, a read/write register.

The Mode of Operation register allows for activation/control of some of the board features.

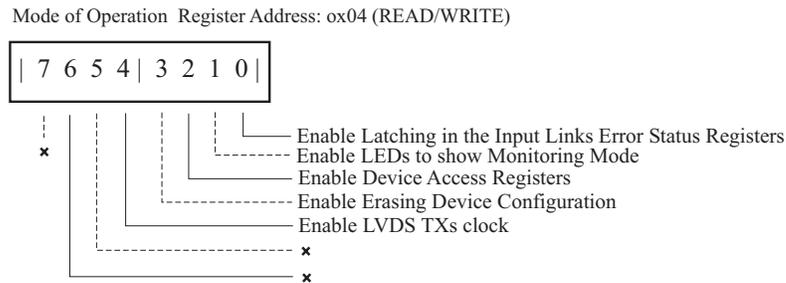


Figure 4.14, Mode of Operation register

Bit#	Name (Type)	Interpretation
7	--	Not used.
6	--	Not used.
5	--	Not used.
4	Enable LVDS TXs Clock	Turns ON the PLL driving the clock to the LVDS Transmitters. Default is enabled ('1').
3	Enable Erasing of Device Configuration	Default is disabled ('0'). Independently from the value of this bit devices configuration/erasing is always possible until all the devices have been configured. When all device are configured, the only way to reconfigure them is to set this bit to '1' and erase their configuration using the PROG bit in the Device Status/Control register.
2	Enable Device Access Registers	Enable the Device Access Registers. Default is disabled ('0').
1	LED Monitoring Mode	Enable LEDs to display the monitoring mode when the mode is changed. Default is enabled ('1').
0	Enable latching in the Input Links Error Status registers	Enable to latch the errors in the Input Links Error Status registers (0x05 and 0x06). Default is disabled ('0').

Table 4.9, Mode of Operation Register.

4.5.9 Input Links Error Status registers

Relative address 0x05 (5 bits) is the Input Links Error Status Low register, relative address 0x06 (5 bits) is the Input Links Error Status High register, both are read only registers. These two registers provide an easy way to monitor the status of the LVDS input links. The error information reported by these two registers can be latched setting the "Enable latching in the Input Links Error Status registers" bit to '1' in the Mode of Operation register (Paragraph 4.5.8).

The status of the input links can also be monitored selecting monitoring mode #14 in the Monitoring Mode register (Paragraph 4.5.14). Monitoring Mode #14 utilize the same signals used by the Input Links Status registers but is not affected by the "enable latching" feature.

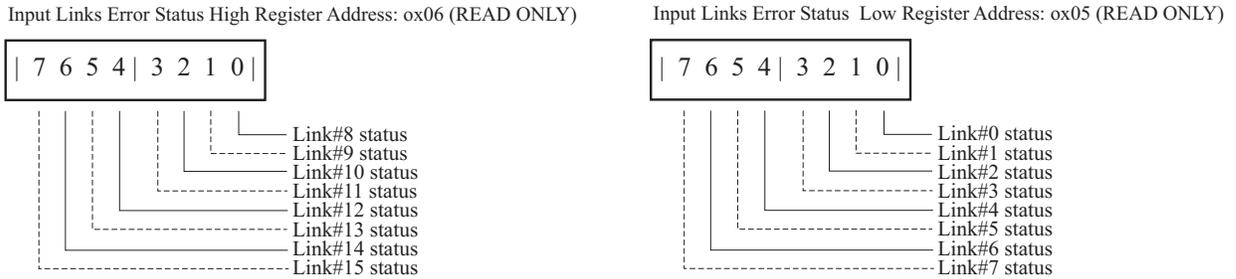


Figure 4.15, Input Links Error Status Registers

Bit#	Name (Type)	Interpretation
7..0	Link Status	<p>Status of the input links #7 (bit 7) to #0 (bit 0). A high value ('1') indicates that the corresponding input link has one of the following critical errors:</p> <ol style="list-style-type: none"> 1) Link clock: missing or out of frequency range (45MHZ to 55MHZ) or Delay Locked Loop not locked; 2) Link frame marker (SYNC) before synchronization: missing or not respecting the protocol (one and only one high bit every seven clock cycles); 3) Link frame marker (SYNC) after synchronization: missing or not respecting the protocol (one and only one high bit every seven clock cycles); 4) Link frame synchronization: the frames are not synchronized with those of the reference link (usually link#0 on the first board (master) in the mixer subsystem (group of four boards handling the data from one supersector)).

Table 4.10, Input Links Error Status Low Register

Bit#	Name (Type)	Interpretation
7..0	Link Status	<p>Status of the input links #15 (bit 7) to #8 (bit 0). A high value ('1') indicates that the corresponding input link has one of the critical errors mentioned in the input links status high register description.</p>

Table 4.11, Input Links Error Status High Register

4.5.10 Device Access-Address register

Relative address 0x07 (5 bits) is the Device Access-Address register, a read/write register. Operations on this register are disabled until all devices are configured ("READY" signal from Board Status/Control register is active). Furthermore, the Device Access feature needs to be enabled by setting the appropriate bit in the Mode of Operation register.

Device Access Address Register. Address: 0x07 (READ/WRITE)

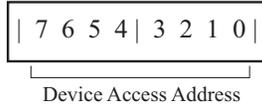


Figure 4.16, Device Access-Address register

The Device Access-Address register is part of the structure that allows access to advanced diagnostic features of the Mixer Board. This register contains the pointer to the device's registers (device's register address). Each time the Device Access-Address register is accessed in writing, the value is also written in each device internal register's pointer. The register pointed to by the Device Access-Address register is accessible through the Device Access Data register.

Bit#	Name (Type)	Interpretation
7..0	Device Access-Address	Pointer to device's registers.

Table 4.12, Device Access-Address register.

4.5.11 Device Access-Data register

Relative address 0x08 (5 bits) is the Device Access Data register, a read/write register. Operations on this register are disabled until all devices are configured ("READY" signal from Board Status/Control register is active). Furthermore, the Device Access feature needs to be enabled by setting the appropriate bit in the Mode of Operation register.

Device Access Data Address: 0x08 (READ/WRITE)



Figure 4.17, Device Access Data register

The Device Access-Data register is part of the structure that allows access to advanced diagnostic features of the Mixer Board. It contains the data of read/write operations performed on device's registers. To access a particular register, two pointers are needed; the device accessed is the one pointed by the Device Status/Control register, the register on the accessed device is the one pointed to by the Device Access Address register.

Bit#	Name (Type)	Interpretation
7..0	Device Access Data	Device's internal register data.

Table 4.13, Device Access register.

4.5.12 Device Access Structure

The Device Access-Address and Device Access-Data registers allow for access to advanced diagnostic features of the Mixer Board. In order to access these features a good understanding of the mixer board/system operation is required.

Each mixer board has 17 devices, one of them is the board controller which is the device hosting the backplane interface. There are two type of board registers, one is located on the board controller; the second type of registers are residing in all the other devices. The procedure to access the two types of registers is different. The board controller registers are accessible with a single (write or read) subrack controller command.

The way to operate on registers not residing on the board controller is different. The procedure includes the use of three support registers on the board controller itself. A register is used to point to the device to be accessed (Device Status/Control register), one to point to the location to be accessed inside the desired device (Device Access Address register) and one as data register (Device Access Data register). As safety precaution the device access features need to be enabled by setting the appropriate bit in the Mode of Operation register.

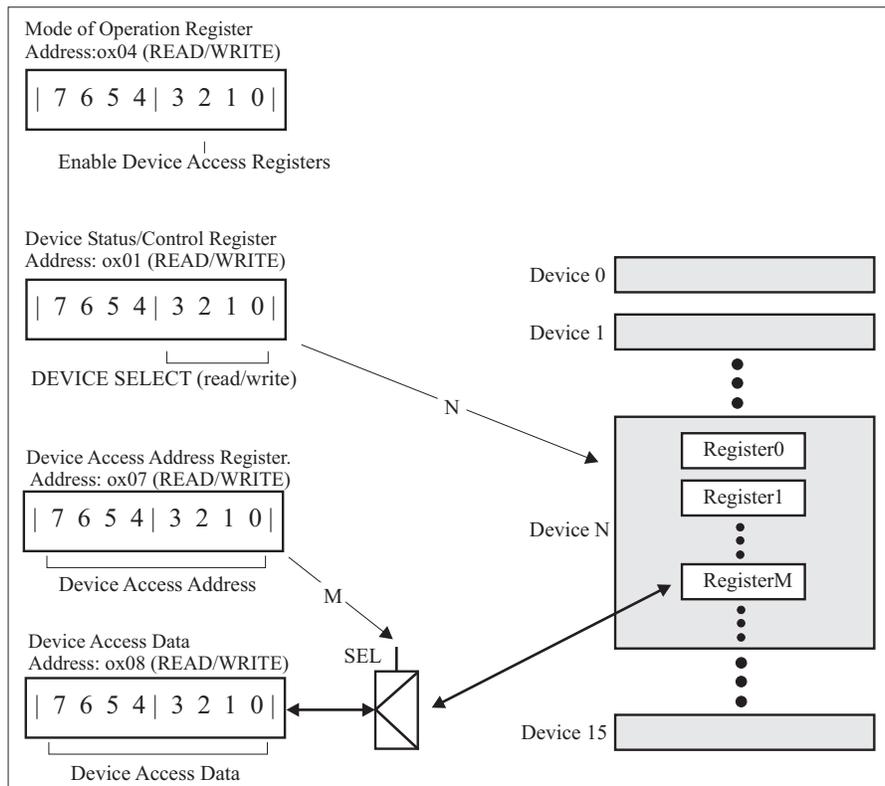


Figure 4.18, Device Access Structure

The multiplexer shown in Figure 4.18 is actually part of each device, so when writing to the Device Access Address register the device register pointer data is automatically written through the board’s local bus to a register in each of the sixteen devices and is used in each of them to control the multiplexer. This implies that when changing the Device Select (Device Status/Control register) to point to a different device there is no need to change the device register pointer (Device Access Address register) if the register pointed is the same in both devices. The devices internal registers are listed and described in Paragraph 7.

4.5.13 Output Links Test Mode registers

Relative address 0x09 (5 bits) is the DFE0 Output Links Test Mode register. Relative address 0x0A (5 bits) is the DFE1 Output Links Test Mode register. Both are read/write registers. These two registers allow the enabling of test pattern transmission on the output LVDS links. The test pattern consists of a walking one sequence followed by a coded word containing information that uniquely identifies the link in a mixer subsystem (4 mixer boards). The test pattern used is specified in Paragraph 11 (Page 112). The pattern is repeated continuously and its starting point is synchronized on the sixteen output links of a mixer board. The status of an output link (test pattern enabled or disabled) can be monitored selecting monitoring mode #13 in the Monitoring Mode register (Paragraph 4.5.14).

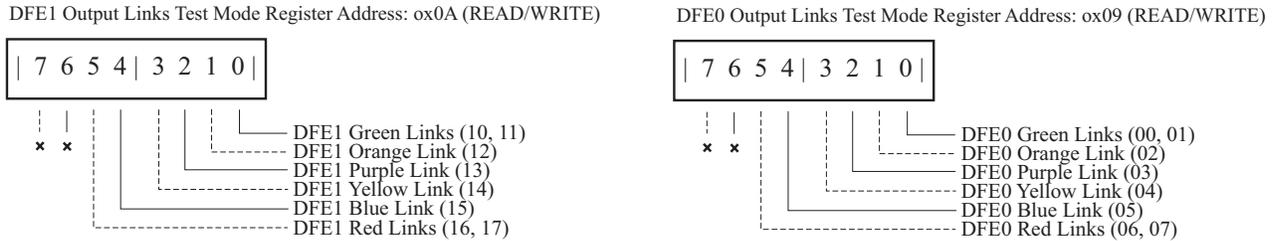


Figure 4.19, DFE0 and DFE1 Output Links Test Mode Registers

Bit#	Name (Type)	Interpretation
7..6	--	Not used.
5	Links 06, 07 TM Enable	Enable test pattern transmission on the DFE0 Red Links (06, 07)
4	Link 05 TM Enable	Enable test pattern transmission on the DFE0 Blue Link (05)
3	Link 04 TM Enable	Enable test pattern transmission on the DFE0 Yellow Link (04)
2	Link 03 TM Enable	Enable test pattern transmission on the DFE0 Purple Link (03)
1	Link 02 TM Enable	Enable test pattern transmission on the DFE0 Orange Link (02)
0	Links 00, 01 TM Enable	Enable test pattern transmission on the DFE0 Green Links (00, 01)

Table 4.14, DFE0 Output Links Test Mode Register

Bit#	Name (Type)	Interpretation
7..6	--	Not used.
5	Links 16, 17 TM Enable	Enable test pattern transmission on the DFE1 Red Links (16, 17)
4	Link 15 TM Enable	Enable test pattern transmission on the DFE1 Blue Link (15)
3	Link 14 TM Enable	Enable test pattern transmission on the DFE1 Yellow Link (14)
2	Link 13 TM Enable	Enable test pattern transmission on the DFE1 Purple Link (13)
1	Link 12 TM Enable	Enable test pattern transmission on the DFE1 Orange Link (12)
0	Links 10, 11 TM Enable	Enable test pattern transmission on the DFE1 Green Links (10, 11)

Table 4.15, DFE1 Output Links Test Mode Register

4.5.14 Monitoring Mode register

Relative address 0x0B (5 bits) is the Monitoring Mode register, a read/write register. This register allows changing of the monitoring mode, which allows the user to select the set of signals that are driving the front panel LEDs (see Paragraph 6.1 for a description of the monitoring modes). The status of these signals can also be remotely read by accessing the Monitoring Status register (Paragraph 4.5.15). Information about whether the monitored signals are changing or have changed are stored in the Monitoring Mode Status History registers (Paragraph 4.5.16). Accessing the Monitoring Mode register in writing will reset the two Monitoring Status History registers. It should be noted that the monitoring mode can also be changed using the front panel reset button. Each time the button is pressed for less than two seconds, the board switches to the next monitoring mode. This change is automatically reflected in the content of the Monitoring Mode register.

Each front panel LED consists of a green and a red LED in the same package. The LED latch mode feature allows latching the LED in the ON position when they get driven.

The LED monitor set feature is used to select between the green and the red sets of LED as trigger signals for the Monitoring Status and Monitoring Status History registers (Paragraphs 4.5.15 and 4.5.16).

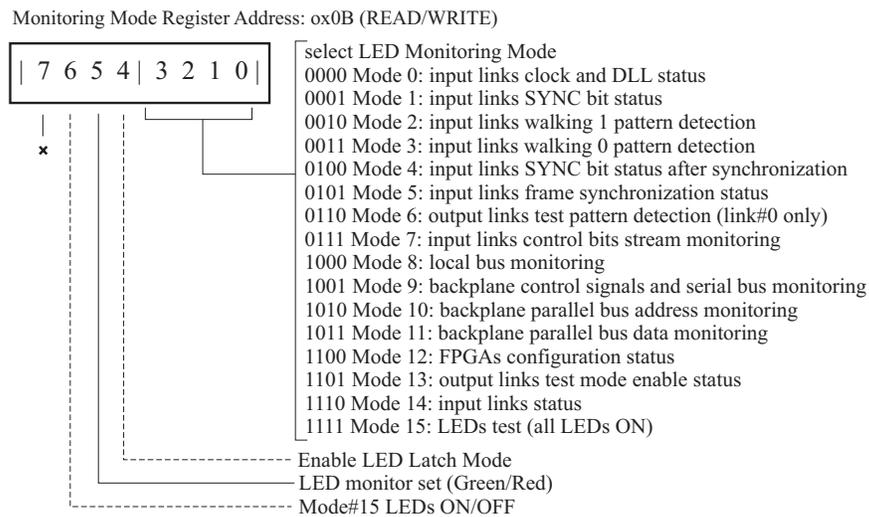


Figure 4.20, Monitoring Mode Register

Bit#	Name (Type)	Interpretation
7	--	Not used.
6	Mode 15 LEDs ON/OFF	In Monitoring Mode #15 all LEDs are on by default ('0'). When this bit is set high ('1') all the LEDs will be forced to be OFF in Monitoring Mode #15.
5	LED monitor set	Used to select the set of led to monitor through the monitoring status registers. '0': green LEDs set (default). '1' red LEDs set.
4	Enable LED Latch Mode	When enabled will force the LEDs (both red and green) to remain ON when they are turned ON even by a short transition. This "LED latching" is reset every time the Monitoring mode is changed (through the monitoring mode register or using the front panel reset button) or when the monitoring mode register is accessed in writing. Default is disabled ('0').
3..0	Monitoring Mode Select	Allows for selection of the monitoring mode

Table 4.16, Monitoring Mode Register

4.5.15 Monitoring Status registers

Relative address 0x0C (5 bits) is the Monitoring Status Low register, and relative address 0x0D (5 bits) is the Monitoring Status High register. Both are read only registers. These registers allow for reading the current status of the front panel LEDs. The default set of LEDs read is the green one. The Monitoring Mode register (Paragraph 4.5.14) allows switching to the red LED set. The front panel LEDs reflect the status of different groups of signals on the mixer board depending of which is the current monitoring mode. The monitoring mode can be changed using the front panel reset button (pressing it for less then 2 seconds) or remotely by accessing the Monitoring Mode register. The sixteen available monitoring modes are described in Paragraph 6.1.

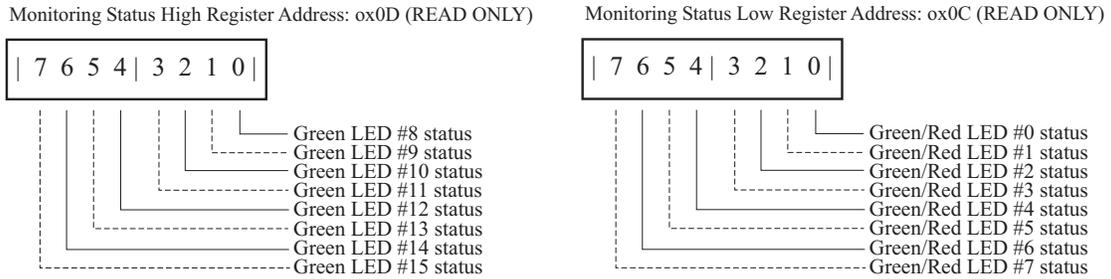


Figure 4.21, Monitoring Status Registers

Bit#	Name (Type)	Interpretation
7..0	Green/Red LEDs #7 to #0 status	Status of the Green/Red LEDs #7 to #0. LED ON is '1', LED OFF is '0'.

Table 4.17, Monitoring Status Low Register

Bit#	Name (Type)	Interpretation
7..0	Green/Red LEDs #15 to #8 status	Status of the Green/Red LEDs #15 to #8. LED ON is '1', LED OFF is '0'.

Table 4.18, Monitoring Status High Register

4.5.16 Monitoring Status History registers

Relative address 0x0E (5 bits) is the Monitoring Status Low History register, and relative address 0x0F (5 bits) is the Monitoring Status High History register. Both are read only registers. The bits in these registers are set if the signal driving the corresponding LED has changed status (high to low or low to high) since the last time the registers were reset. The registers are reset each time the Monitoring Mode register is accessed in writing.

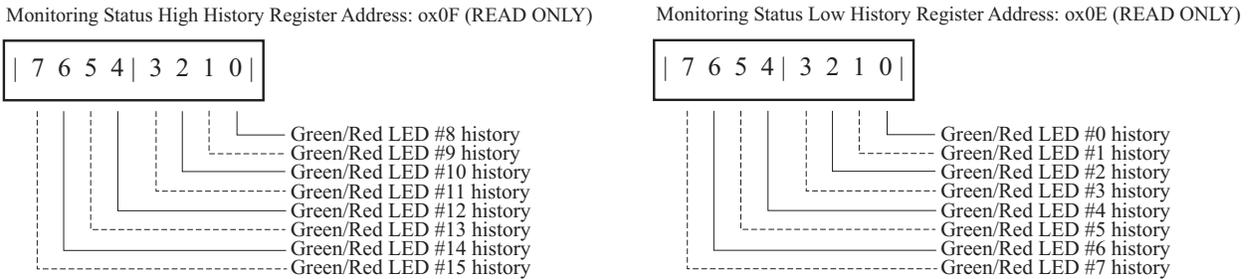


Figure 4.22, Monitoring Status History Registers

Bit#	Name (Type)	Interpretation
7..0	Green-Red LED #7 to #0 status history	Status history of the Green-Red LEDs #7 to #0. '1' mean that the signal driving the corresponding Green-Red LEDs changed status since last reset of the register, '0' otherwise.

Table 4.19, Monitoring Status Low History Register

Bit#	Name (Type)	Interpretation
7..0	Green-Red LED #15 to #8 status history	Status history of the Green-Red LEDs #15 to #8. '1' mean that the corresponding Green-Red LED changed status since last reset of the register, '0' otherwise.

Table 4.20, Monitoring Status High History Register

Bit#	Name (Type)	Interpretation
7..4	Trigger Length	The number of frames (one frame is seven 53MHz clock cycles long) the trigger should last.
3..2	--	Not used.
1	Continuous Trigger	Used to have a trigger that will last as long as the FIFO Trigger bit is active (high).
0	FIFO Trigger	A transition from '0' to '1' of this bit will internally latch the other bits in the register and generate a trigger signal for the output links FIFOs. If the "Continuous Trigger" bit is '1' the trigger will last until the "FIFO Trigger" bit is set back to '0'. If the "Continuous Trigger" bit is '0' the trigger will last the number of frames specified by the "Trigger Length" bits. For a new trigger to be produced the "FIFO Trigger" bit should be set back to '0' and then to '1' to generate a new '0' to '1' transition.

Table 4.22, FIFO Trigger Control Register.

4.5.19 Read/Write Test register

Relative address 0x1B is the read/write test register. This register doesn't affect/reflect the status of the board. Its only purpose is to allow test of read/write operations.

4.5.20 Firmware Revision Date registers

Relative addresses 0x1C, 0x1D, and 0x1E (5 bits) are the firmware revision date registers; all three are read only registers. These registers contain the Binary Coded Decimal of the day (0x1C), the month (0x1D) and the year (0x1E) of the board controller firmware revision.

4.5.21 Board Serial Number register

Relative address 0x1F (5 bits) is the board serial number register. It contains the Binary Coded Decimal serial number of the board. As of today, 25 boards have been manufactured. 0x00 is used for boards on which the serial number has not been encoded in the firmware. Board #01 and 02 are the two mixer board prototypes. Because their difference with the production boards are minimal there are no restriction for their use in the mixer system.

The serial number is also marked on the solder side of each board.

4.6 Mixer Board - Subrack Controller Slow Monitoring Serial Bus interface

The following description of the slow monitoring custom serial bus is partially derived from [Ref.5d].

The Mixer system uses several components and signal protocols designed/used by the Digital Front-End Board system. The slow monitoring custom serial bus is one of them.

To reduce noise injection in sensible detector parts located close to the Mixer System the custom general purpose A16:D8 bus is not used during data taking. Status information can be collected from the Mixer Board using a custom serial bus and the information is made accessible through a MIL-STD-1553 Remote Terminal in the Subrack Controller.

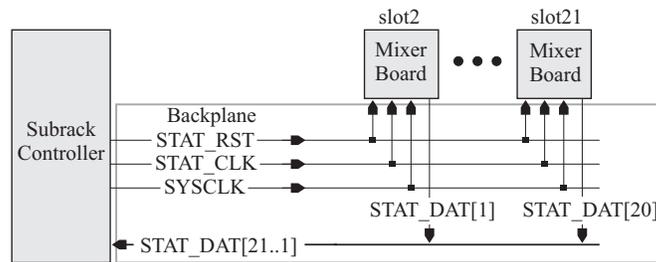


Figure 4.25, Slow Monitoring Bus signals

The subrack controller continuously collect sixteen bits of data from each Mixer Board slow monitoring register.

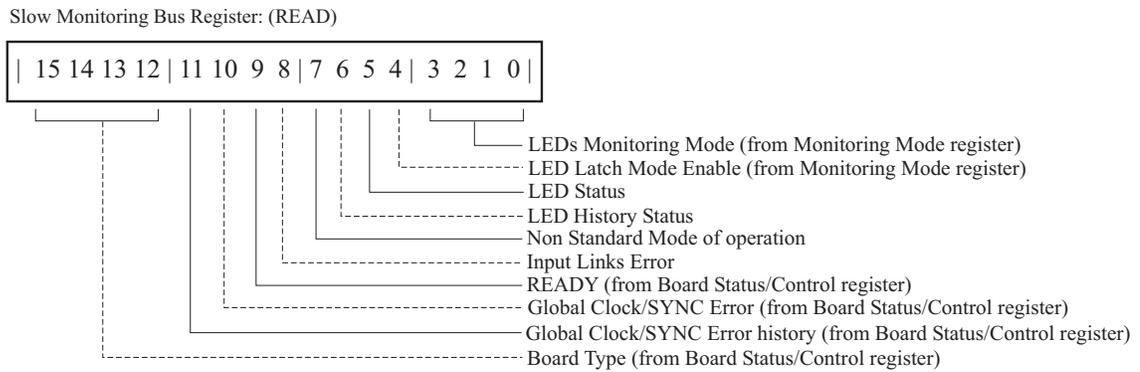


Figure 4.26, Slow Monitoring Bus register

Bit#	Name (Type)	Interpretation
15..12	Board Type	From Board Status/Control Register. Used by the DAQ system to recognize the type of board. The mixer board type is "b1101" or "0xD".
11	Global Clock./SYNC Error history	From Board Status/Control Register. Latched version of Global Clock./SYNC Error.
10	Global Clock./SYNC Error	From Board Status/Control Register. The mixer board automatically most appropriate clock to be used, but for correct operations the mixer subsystem master boards must use the link#0 clock and the mixer subsystem slave boards must use the backplane clock. Furthermore the link#0 SYNC on the master boards and the backplane SYNC on the slave boards must respect the correct protocol (one and only one high pulse in a seven clock cycles wide window). If these conditions are not satisfied the Global Clock/SYNC bit is set.
9	Ready	From Board Status/Control Register. This bit is set if all devices are configured.
8	Input Links Error	Logic OR of all the bits of the Input Links Error Status registers.
7	Not Standard Mode	Set when the board is not operating in the standard mode. Is the logic OR of the following signals: not <i>READY</i> (from Board Status/Control Register) not <i>Enable LVDS TXs Clock</i> (from Mode of Operation register) <i>Enable Erasing of Device Configuration</i> (from Mode of Operation register) <i>Enable Device Access Register</i> (from Mode of Operation register) bits 5..0 of the DFE0 Output Links Test Mode register bits 5..0 of the DFE1 Output Links Test Mode register
6	LED History Status	Logic OR of all the bits of the two LEDs Status History Registers.
5	LED Status	Logic AND of all the bits of the two LEDs Status Registers.
4	LED Latch Mode Enable	From Monitoring Mode Register. LED Latch Mode Enable.
3..0	LED Monitoring Mode	From Monitoring Mode Register. Shows the current LED monitoring mode.

Table 4.23, Slow Monitoring Bus Register

4.7 JTAG Interface

See a description of JTAG in Paragraph 16. Two four pin Test Access Ports (TAP) are provided on the Mixer Board, the first (Table 4.24) accesses the Board Controller FPGA and its configuration EEPROM, the second (Table 4.25) accesses the chain formed by the remaining sixteen FPGAs.

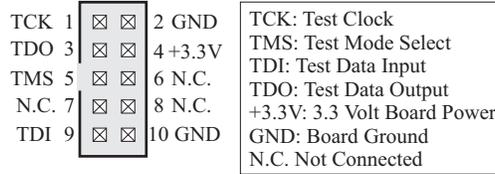


Figure 4.27, JTAG Connectors pinout

The JTAG Chain#1 TAP has been wired to the front panel top row of pins of the output links connector with a hardware modification. This change allows for board controller EEPROM reprogramming in-system without the need to disconnect the LVDS cabling and to remove the board from the mixer subrack. The front panel pinout is shown in Table 4.2. The JTAG ports have been extensively used during the initial board testing to program the board FPGAs without the need for using the backplane A16:D8 General Purpose bus.

JTAG Chain#1, connector CON3		
Device #	Device Type	Notes
1	XC18V01SO20C	In-System-Programmable Configuration PROM.
2	XCS40XL-5PQ240C	Spartan-XL FPGA used as Board Controller.

Table 4.24, JTAG Chain#1 Devices

JTAG Chain#2, connector CON1		
Device #	Device Type	Notes
1	XCS40XL-5PQ240C	U2, Spartan-XL FPGA used as DFE1 Yellow Purple (Outlink 5).
2	XCS40XL-5PQ240C	U1, Spartan-XL FPGA used as DFE1 Red Blue (Outlink 6).
3	XCS40XL-5PQ240C	U10, Spartan-XL FPGA used as DFE1 Orange Green (Outlink 4).
4	XCS40XL-5PQ240C	U11, Spartan-XL FPGA used as DFE0 Red Blue (Outlink 3).
5	XCS40XL-5PQ240C	U19, Spartan-XL FPGA used as DFE0 Orange Green (Outlink 1).
6	XCS40XL-5PQ240C	U18, Spartan-XL FPGA used as DFE0 Yellow Purple (Outlink 2).
7	XCV50-6PQ240C	U31, Virtex FPGA used as LINK_IN 13-15.
8	XCV50-6PQ240C	U45, Virtex FPGA used as LINK_IN 4-6.
9	XCV50-6PQ240C	U46, Virtex FPGA used as LINK_IN 1-3.
10	XCV50-6PQ240C	U32, Virtex FPGA used as LINK_IN 10-12.
11	XCV50-6PQ240C	U47, Virtex FPGA used as LINK_IN 0.
12	XCV50-6PQ240C	U48, Virtex FPGA used as Backplane Left Driver.
13	XCV50-6PQ240C	U33, Virtex FPGA used as LINK_IN 7-9.
14	XCV50-6PQ240C	U12, Virtex FPGA used as Backplane DFE0 receiver.
15	XCV50-6PQ240C	U5, Virtex FPGA used as Backplane DFE1 receiver.
16	XCV50-6PQ240C	U6, Virtex FPGA used as Backplane Right Driver.

Table 4.25, JTAG Chain#2 Devices

The JTAG ports also allow the performing of a boundary scan [Ref. 17] of the mixer board. The boundary scan testing has proven to be an invaluable resource in the detection of board defects or assembly problems [Ref. 8c]. Table 4.26 lists the Boundary Scan Description Language (BSDL) files for the devices used on the mixer board, which are compatible with JTAG/IEEE 1149.1. The files in Table 4.26 are available from Xilinx [Ref. 40].

Device	Description	BSDL File
XCS40XL	Spartan-XL FPGA	xcs40xl_pq240.bsd
XCV50	Virtex FPGA	xcv50_pq240.bsd
XC18V512	In-System-Programmable Configuration PROM.	xc18v512_so20.bsd

Table 4.26, Boundary Scan Description Language (BSDL) Files

4.8 Logic Analyzer Connectors

For debugging/diagnostic purposes the Mixer Board has three Amp "Mictor 38" connectors (AMP 2-767004-2) to fit the Agilent (formerly HP) [Ref. 11] High Density adapter cables (Agilent E5346A). Each adapter cable fits two test pods of an Agilent 16550A Logic Analyzer allowing monitoring of 32 signals. The following three tables list the signals connected to each mixer board's logic analyzer connector. There are several spare connections that can be assigned in the FPGA hardware description (VHDL code) to monitor specific signals. These spare connections are marked with **▲**.

Notes	Schematic name	Pin #	Pin name	Pin name	Pin #	Schematic name	Notes
	N.C.	1 —	+5VDC	SCL	— 2	N.C.	
	GND	3 —	GND	SDA	— 4	N.C.	
	N.C.	5 —	CLK1	CLK2	— 6	N.C.	
A16:D8 bus SYStem CLoCK	SYSCLK	7 —	P1.15	P2.15	— 8	BADDR15	A16:D8 bus Address bit
A16:D8 bus Address Strobe	AS	9 —	P1.14	P2.14	— 10	BADDR14	A16:D8 bus Address bit
A16:D8 bus /SYStem RESET	/SYSRESET	11 —	P1.13	P2.13	— 12	BADDR13	A16:D8 bus Address bit
A16:D8 bus WRITE	WRITE	13 —	P1.12	P2.12	— 14	BADDR12	A16:D8 bus Address bit
A16:D8 bus Data Transfer ACKnowledge	DTACK	15 —	P1.11	P2.11	— 16	BADDR11	A16:D8 bus Address bit
A16:D8 bus Bus Error	BERR	17 —	P1.10	P2.10	— 18	BADDR10	A16:D8 bus Address bit
Serial Bus Data In	STAT	19 —	P1.09	P2.09	— 20	BADDR9	A16:D8 bus Address bit
Serial Bus Clock	IN_STAT-CLK	21 —	P1.08	P2.08	— 22	BADDR8	A16:D8 bus Address bit
A16:D8 bus Data bit	BDAT7	23 —	P1.07	P2.07	— 24	BADDR7	A16:D8 bus Address bit
A16:D8 bus Data bit	BDAT6	25 —	P1.06	P2.06	— 26	BADDR6	A16:D8 bus Address bit
A16:D8 bus Data bit	BDAT5	27 —	P1.05	P2.05	— 28	BADDR5	A16:D8 bus Address bit
A16:D8 bus Data bit	BDAT4	29 —	P1.04	P2.04	— 30	BADDR4	A16:D8 bus Address bit
A16:D8 bus Data bit	BDAT3	31 —	P1.03	P2.03	— 32	BADDR3	A16:D8 bus Address bit
A16:D8 bus Data bit	BDAT2	33 —	P1.02	P2.02	— 34	BADDR2	A16:D8 bus Address bit
A16:D8 bus Data bit	BDAT1	35 —	P1.01	P2.01	— 36	BADDR1	A16:D8 bus Address bit
A16:D8 bus Data bit	BDAT0	37 —	P1.00	P2.00	— 38	BADDR0	A16:D8 bus Address bit

Table 4.27, HP Logic Analyzer connector J3 (suggested analyzer pods: 1 and 2)

Notes	Schematic name	Pin #	Pin name	Pin name	Pin #	Schematic name	Notes
	N.C.	1 —	+5VDC	SCL	— 2	N.C.	
	GND	3 —	GND	SDA	— 4	N.C.	
	N.C.	5 —	CLK1	CLK2	— 6	N.C.	
A16:D8 bus Data Buffer Direction	VDAT_DIR	7 —	P1.15	P2.15	— 8	FPGACLK10	Board Controller Global Clock
A16:D8 bus Data Buffer Enable	/VDAT_EN	9 —	P1.14	P2.14	— 10	53CLK0	Local Oscillator 53MHz Clock
Board Controller Master Reset to FPGAs	/MRESET	11 —	P1.13	P2.13	— 12	ASTRB	Local Bus Address Strobe
FE FPGA IN0	SPFE0_2	13 —	P1.12	P2.12	— 14	DSTRB	Local Bus Data Strobe
FE FPGA IN0	SPFE0_1	15 —	P1.11	P2.11	— 16	/WRITE	Local Bus /WRITE
FE FPGA IN0	SPFE0_0	17 —	P1.10	P2.10	— 18	/CONFIGDAT_EN	Local Bus Buffer enable
Backplane DFE1 Rx	SP1RX1	19 —	P1.09	P2.09	— 20	CONFIGDAT_DIR	Local Bus Buffer Direction
Backplane DFE1 Rx	SP1RX0	21 —	P1.08	P2.08	— 22	CONFIGCLK	FPGAs Configuration Clock
Backplane DFE0 Rx	SP0RX1	23 —	P1.07	P2.07	— 24	FDAT7	Local Bus Data bit
Backplane DFE0 Rx	SP0RX0▲	25 —	P1.06	P2.06	— 26	FDAT6	Local Bus Data bit
Backplane Left Driver	SPLDR1	27 —	P1.05	P2.05	— 28	FDAT5	Local Bus Data bit
Backplane Left Driver	SPLDR0	29 —	P1.04	P2.04	— 30	FDAT4	Local Bus Data bit
Backplane Right Driver	SPRDR3	31 —	P1.03	P2.03	— 32	FDAT3	Local Bus Data bit
Backplane Right Driver	SPRDR2	33 —	P1.02	P2.02	— 34	FDAT2	Local Bus Data bit
Backplane Right Driver	SPRDR1	35 —	P1.01	P2.01	— 36	FDAT1	Local Bus Data bit
Backplane Right Driver	SPRDR0▲	37 —	P1.00	P2.00	— 38	FDAT0	Local Bus Data bit

Table 4.28, HP Logic Analyzer connector J5 (suggested analyzer pods: 3 and 4)

Notes	Schematic name	Pin #	Pin name	Pin name	Pin #	Schematic name	Notes
	N.C.	1 —	+5VDC	SCL	— 2	N.C.	
	GND	3 —	GND	SDA	— 4	N.C.	
	N.C.	5 —	CLK1	CLK2	— 6	N.C.	
LinkIn0 FE FPGA & DFE0 Blue Red FGAs	Analyzer15▲	7 —	P1.15	P2.15	— 8	Analyzer31▲	LinkIn0 FE FPGA & DFE1 Blue Red FPGA
LinkIn0 FE FPGA & DFE0 Blue Red FPGA	Analyzer14▲	9 —	P1.14	P2.14	— 10	Analyzer30▲	LinkIn0 FE FPGA & DFE1 Blue Red FPGA
LinkIn0 FE FPGA & DFE0 Blue Red FPGA	Analyzer13▲	11 —	P1.13	P2.13	— 12	Analyzer29▲	LinkIn0 FE FPGA & DFE1 Blue Red FPGA
LinkIn0 FE FPGA & DFE0 Blue Red FPGA	Analyzer12▲	13 —	P1.12	P2.12	— 14	Analyzer28▲	LinkIn0 FE FPGA & DFE1 Blue Red FPGA
LinkIn0 FE FPGA & DFE0 Blue Red FPGA	Analyzer11▲	15 —	P1.11	P2.11	— 16	Analyzer27▲	LinkIn0 FE FPGA & DFE1 Blue Red FPGA
LinkIn0 FE FPGA & DFE0 Blue Red FPGA	Analyzer10▲	17 —	P1.10	P2.10	— 18	Analyzer26▲	LinkIn0 FE FPGA & DFE1 Blue Red FPGA
LinkIn0 FE FPGA & DFE0 Blue Red FPGA	Analyzer9▲	19 —	P1.09	P2.09	— 20	Analyzer25▲	LinkIn0 FE FPGA & DFE1 Blue Red FPGA
LinkIn0 FE FPGA & DFE0 Yellow Purple FPGA	Analyzer8▲	21 —	P1.08	P2.08	— 22	Analyzer24▲	LinkIn0 FE FPGA & DFE1 Blue Red FPGA
LinkIn0 FE FPGA & DFE0 Yellow Purple FPGA	Analyzer7▲	23 —	P1.07	P2.07	— 24	Analyzer23▲	LinkIn0 FE FPGA & DFE1 Green Orange FPGA
LinkIn0 FE FPGA & DFE0 Green Orange FPGA	Analyzer6▲	25 —	P1.06	P2.06	— 26	Analyzer22▲	LinkIn0 FE FPGA & DFE1 Green Orange FPGA
LinkIn0 FE FPGA & DFE0 Green Orange FPGA	Analyzer5▲	27 —	P1.05	P2.05	— 28	Analyzer21▲	LinkIn0 FE FPGA & DFE1 Green Orange FPGA
LinkIn0 FE FPGA & DFE0 Green Orange FPGA	Analyzer4▲	29 —	P1.04	P2.04	— 30	Analyzer20▲	LinkIn0 FE FPGA & DFE1 Green Orange FPGA
LinkIn0 FE FPGA & DFE0 Green Orange FPGA	Analyzer3▲	31 —	P1.03	P2.03	— 32	Analyzer19▲	LinkIn0 FE FPGA & DFE1 Green Orange FPGA
LinkIn0 FE FPGA & DFE0 Green Orange FPGA	Analyzer2▲	33 —	P1.02	P2.02	— 34	Analyzer18▲	LinkIn0 FE FPGA & DFE1 Green Orange FPGA
LinkIn0 FE FPGA & DFE0 Green Orange FPGA	Analyzer1▲	35 —	P1.01	P2.01	— 36	Analyzer17▲	LinkIn0 FE FPGA & DFE1 Green Orange FPGA
LinkIn0 FE FPGA & DFE0 Green Orange FPGA	Analyzer0▲	37 —	P1.00	P2.00	— 38	Analyzer16▲	LinkIn0 FE FPGA & DFE1 Green Orange FPGA

Table 4.29, HP Logic Analyzer connector J7 (suggested analyzer pods: 5 and 6)

The signals monitored through connector J7 can be remotely changed to two preset configurations without the need of changing the firmware. The active configuration is determined by a bit in the Input Link Control register (Paragraph 7.1.4).

The LVDS receiver used for the input link#0 is a 28-bit receiver. This type of receiver can also be used as a 21-bit receiver. The two preset configuration for analyzer connector J7 allows monitoring the outputs of the LVDS receiver in both cases, allowing analyzer access to both the 21-bit and the 28-bit LVDS transmissions.

Notes [schematic name of monitored signal]	Schematic name	Pin #	Pin name	Pin name	Pin #	Schematic name	Notes [schematic name of monitored signal]
	N.C.	1	+5VDC	SCL	2	N.C.	
	GND	3	GND	SDA	4	N.C.	
	N.C.	5	CLK1	CLK2	6	N.C.	
Link0 Data bit 15 [Link0_in(20)]	Analyzer15	7	P1.15	P2.15	8	Analyzer31	Link#0 clock [RXCLK0]
Link0 Data bit 14 [Link0_in(19)]	Analyzer14	9	P1.14	P2.14	10	Analyzer30	Global clock [CLK]
Link0 Data bit 13 [Link0_in(18)]	Analyzer13	11	P1.13	P2.13	12	Analyzer29	Global SYNC [GSYNC]
Link0 Data bit 12 [Link0_in(15)]	Analyzer12	13	P1.12	P2.12	14	Analyzer28	Link#0 Clock Fail [LK0CLK_FAIL]
Link0 Data bit 11 [Link0_in(14)]	Analyzer11	15	P1.11	P2.11	16	Analyzer27	Link#0 SYNC protocol OK [LK0_SYNC_OK] and SYNC protocol OK after synchronization.
Link0 Data bit 10 [Link0_in(13)]	Analyzer10	17	P1.10	P2.10	18	Analyzer26	Link#0 Frame Synchronization OK
Link0 Data bit 9 [Link0_in(12)]	Analyzer9	19	P1.09	P2.09	20	Analyzer25	Link#0 Clock Internal DLL Locked signal [LK0CLK_DLLI_LOCKED]
Link0 Data bit 8 [Link0_in(9)]	Analyzer8	21	P1.08	P2.08	22	Analyzer24	Link#0 Clock External DLL enable signal from Clock Controller [nDLL_EN]
Link0 Data bit 7 [Link0_in(8)]	Analyzer7	23	P1.07	P2.07	24	Analyzer23	Global Clock FAIL signal from Clock Controller [GCLK_FAIL]
Link0 Data bit 6 [Link0_in(7)]	Analyzer6	25	P1.06	P2.06	26	Analyzer22	Link#0 Walking 1 pattern OK [LK0_W1pattern_OK]
Link0 Data bit 5 [Link0_in(6)]	Analyzer5	27	P1.05	P2.05	28	Analyzer21	Link#0 Walking 0 pattern OK [LK0_W0pattern_OK]
Link0 Data bit 4 [Link0_in(4)]	Analyzer4	29	P1.04	P2.04	30	Analyzer20	Link0 Data bit 20 [Link0_in(26)]
Link0 Data bit 3 [Link0_in(3)]	Analyzer3	31	P1.03	P2.03	32	Analyzer19	Link0 Data bit 19 [Link0_in(25)]
Link0 Data bit 2 [Link0_in(2)]	Analyzer2	33	P1.02	P2.02	34	Analyzer18	Link0 Data bit 18 [Link0_in(24)]
Link0 Data bit 1 [Link0_in(1)]	Analyzer1	35	P1.01	P2.01	36	Analyzer17	Link0 Data bit 17 [Link0_in(22)]
Link0 Data bit 0 [Link0_in(0)]	Analyzer0	37	P1.00	P2.00	38	Analyzer16	Link0 Data bit 16 [Link0_in(21)]

Table 4.30, HP Logic Analyzer connector J7 preset configuration 0 (default, 21 bit link monitoring)

Notes [schematic name of monitored signal]	Schematic name	Pin #	Pin name	Pin name	Pin #	Schematic name	Notes [schematic name of monitored signal]
	N.C.	1	+5VDC	SCL	2	N.C.	
	GND	3	GND	SDA	4	N.C.	
	N.C.	5	CLK1	CLK2	6	N.C.	
Link0 Data bit 15 [Link0_in(15)]	Analyzer15	7	P1.15	P2.15	8	Analyzer31	Link#0 clock [RXCLK0]
Link0 Data bit 14 [Link0_in(14)]	Analyzer14	9	P1.14	P2.14	10	Analyzer30	Global clock [CLK]
Link0 Data bit 13 [Link0_in(13)]	Analyzer13	11	P1.13	P2.13	12	Analyzer29	Global SYNC [GSYNC]
Link0 Data bit 12 [Link0_in(12)]	Analyzer12	13	P1.12	P2.12	14	Analyzer28	Link#0 Clock Fail [LK0CLK_FAIL]
Link0 Data bit 11 [Link0_in(11)]	Analyzer11	15	P1.11	P2.11	16	Analyzer27	Link0 Data bit 27 [Link0_in(27)]
Link0 Data bit 10 [Link0_in(10)]	Analyzer10	17	P1.10	P2.10	18	Analyzer26	Link0 Data bit 26 [Link0_in(26)]
Link0 Data bit 9 [Link0_in(9)]	Analyzer9	19	P1.09	P2.09	20	Analyzer25	Link0 Data bit 25 [Link0_in(25)]
Link0 Data bit 8 [Link0_in(8)]	Analyzer8	21	P1.08	P2.08	22	Analyzer24	Link0 Data bit 24 [Link0_in(24)]
Link0 Data bit 7 [Link0_in(7)]	Analyzer7	23	P1.07	P2.07	24	Analyzer23	Link0 Data bit 23 [Link0_in(23)]
Link0 Data bit 6 [Link0_in(6)]	Analyzer6	25	P1.06	P2.06	26	Analyzer22	Link0 Data bit 22 [Link0_in(22)]
Link0 Data bit 5 [Link0_in(5)]	Analyzer5	27	P1.05	P2.05	28	Analyzer21	Link0 Data bit 21 [Link0_in(21)]
Link0 Data bit 4 [Link0_in(4)]	Analyzer4	29	P1.04	P2.04	30	Analyzer20	Link0 Data bit 20 [Link0_in(20)]
Link0 Data bit 3 [Link0_in(3)]	Analyzer3	31	P1.03	P2.03	32	Analyzer19	Link0 Data bit 19 [Link0_in(19)]
Link0 Data bit 2 [Link0_in(2)]	Analyzer2	33	P1.02	P2.02	34	Analyzer18	Link0 Data bit 18 [Link0_in(18)]
Link0 Data bit 1 [Link0_in(1)]	Analyzer1	35	P1.01	P2.01	36	Analyzer17	Link0 Data bit 17 [Link0_in(17)]
Link0 Data bit 0 [Link0_in(0)]	Analyzer0	37	P1.00	P2.00	38	Analyzer16	Link0 Data bit 16 [Link0_in(16)]

Table 4.31, HP Logic Analyzer connector J7 preset configuration 1 (28 bit link monitoring)

4.9 Power Supply and safety features

The Mixer Boards are powered through the backplane connectors (see Paragraph 10, page 110 for connectors pinout). The backplane is powered by a Vicor **[Ref. 39]** Mini PFC power supply using three 80 Amperes modules in parallel for a total of 240 Amperes @ +3.3Volt. The backplane is also connected to a +5V “brick” style supply to provide power to the subrack controller. A sketch of the mixer backplane is provided in Figure 4.5, detailed backplane description is available in separate documents **[Ref. 8]**. The two mixer board backplane connectors provide a total of 25 3.3Volt pins and 175 ground pins. The Mixer board 3.3Volt input is protected from both over-current and over-voltage with a 10 Amperes fuse and a 1N5908 zener transient voltage suppressor **[Ref. 35]**.

Xilinx Virtex FPGAs need to be powered with two voltages, 3.3Volt (I/Os) and 2.5Volt (core). The 2.5Volt is generated from the 3.3Volt with a Micrel 39500 low dropout 5 Amperes regulator **[Ref. 32]**. The input of the Micrel regulator is protected from over-current with a 4 Amperes fuse.

5. Mixer Board Configuration

The Mixer Board uses a total of 17 FPGAs, 7 Xilinx Spartan XCS40XL and 10 Xilinx Virtex XCV50. The XCS40XL has 330,647 configuration bits (PROM size: 330,696), the XCV50 has 559,232 configuration bits. One of the Spartan devices is used as the Board Controller and a Xilinx XC18V01 In-System-Programmable PROM automatically configures it at power-up. This PROM has a capacity of 1,048,576 bits and can be reprogrammed using JTAG. [Ref.40].

The top row of the LVDS input connector (see Table 4.2) allows access from the front panel to the board controller JTAG chain. This permits the reprogramming of the board controller EEPROM without removing the board from the mixer subrack

After being configured (at power up) the board controller is ready to handle the configuration data for the remaining 16 FPGAs. This data is fed to the board controller through the A16:D8 general-purpose backplane bus [Paragraph 4.5] by the subrack controller located in slot 1 or alternatively by mean of one of the board JTAG ports.

♦ *A note of caution: The download of a wrong configuration file to a device can cause not only a system malfunction but also irreversible hardware damage.*

5.1 Configuration through JTAG

As was already mentioned the board controller FPGA firmware can be changed by reprogramming its configuration EEPROM through one of the two JTAG chains (see paragraph 4.7). The remaining sixteen FPGAs can be programmed through the second JTAG chain. But contrary to the board controller, which is reprogrammed at power-up with the configuration data stored in the EEPROM, the other FPGAs will need to be reconfigure after each power-up.

The JTAG configuration method has been extensively used during the initial mixer board testing and debugging and has proved itself to be a very valuable feature.

The software used to configure/program devices through the JTAG ports is the "Xilinx JTAG Programmer" [Ref. 40]. The software Help Menu provides thorough instructions for configuration and program operations. In order to perform configuration correctly the devices part of a JTAG chain needs to be specified in the right order (refer to paragraph 4.7) and each device definition should point to its "bit" file. The JTAG chain information is usually stored in a Chain Description File (extension "cdf").

The hardware needed for this procedure, beside a PC is one of the Xilinx JTAG cables:

Parallel cable, connects to any PC using the standard IEEE-1284 compliant parallel port.

MultiLINX cable, takes advantage of the USB port found on newer PCs and the serial port (RS232) on most PCs & work stations.

It should be noted that the files for JTAG configuration are different than those used for configuration through the A16:D8 backplane bus using the Subrack Controller. The files need to be generated with the configuration option set to JTAG in the "Xilinx Design Manager tool".

5.2 Configuration through the subrack general purpose bus.

The Subrack Controller [Paragraph 14.1] has the FPGAs configuration information stored in a removable CompactFlash™ memory card [Paragraph 14.2]. The CompactFlash™ can be easily inserted/removed from the subrack controller front panel. This memory card allows the storage of multiple configuration sets for the FPGAs of the 20 Mixer Boards inside the Mixer System Subrack. Having more than one set of FPGAs configurations available allow for more reliable/efficient FPGAs firmware updates with the ability to return almost immediately to the previously used firmware version if the new one doesn't perform as expected.

Device #	Device Type	Schematic device#, device name	Mixer#1 files	Mixer#2 files	Mixer#3 files	Mixer#4 files
0	Spartan XL	U2, DFE1 YP (Outlink 5).	0200_PC.bin	0300_PC.bin	0400_PC.bin	0500_PC.bin
1	Spartan XL	U1, DFE1 RB (Outlink 6).	0201_PC.bin	0301_PC.bin	0401_PC.bin	0501_PC.bin
2	Spartan XL	U10, DFE1 OG (Outlink 4).	0202_PC.bin	0302_PC.bin	0402_PC.bin	0502_PC.bin
3	Spartan XL	U11, DFE0 RB (Outlink 3).	0203_PC.bin	0303_PC.bin	0403_PC.bin	0503_PC.bin
4	Spartan XL	U19, DFE0 OG (Outlink 1).	0204_PC.bin	0304_PC.bin	0404_PC.bin	0504_PC.bin
5	Spartan XL	U18, DFE0 YP (Outlink 2).	0205_PC.bin	0305_PC.bin	0405_PC.bin	0505_PC.bin
6	Virtex	U31, LINK_IN 13-15.	0206_PC.bin	0306_PC.bin	0406_PC.bin	0506_PC.bin
7	Virtex	U45, LINK_IN 4-6.	0207_PC.bin	0307_PC.bin	0407_PC.bin	0507_PC.bin
8	Virtex	U46, LINK_IN 1-3.	0208_PC.bin	0308_PC.bin	0408_PC.bin	0508_PC.bin
9	Virtex	U32, LINK_IN 10-12.	0209_PC.bin	0309_PC.bin	0409_PC.bin	0509_PC.bin
10	Virtex	U47, LINK_IN 0.	020A_PC.bin	030A_PC.bin	040A_PC.bin	050A_PC.bin
11	Virtex	U48, Backplane Left Driver.	020B_PC.bin	030B_PC.bin	040B_PC.bin	050B_PC.bin
12	Virtex	U33, LINK_IN 7-9.	020C_PC.bin	030C_PC.bin	040C_PC.bin	050C_PC.bin
13	Virtex	U12, Backplane DFE0 receiver.	020D_PC.bin	030D_PC.bin	040D_PC.bin	050D_PC.bin
14	Virtex	U5, Backplane DFE1 receiver.	020E_PC.bin	030E_PC.bin	040E_PC.bin	050E_PC.bin
15	Virtex	U6, Backplane Right Driver.	020F_PC.bin	030F_PC.bin	040F_PC.bin	050F_PC.bin

Table 5.1, Configuration Files denomination.

Mixer#	Subrack slots
1	02, 06, 10, 14, 18
2	03, 07, 11, 15, 19
3	04, 08, 12, 16, 20
4	05, 09, 13, 17, 21

Table 5.2, Mixer# and Subrack slot#.

Table 5.1 lists the sixteen FPGA devices with the names of their configuration files. Each device is configured with one of the four sets of files corresponding to the four boards in a mixer subsystem (Mixer 1, Mixer 2, Mixer 3, Mixer 4). The file naming convention is

<FSslot#><Device#>_PC.bin, where "FSslot#" is the slot# in the first mixer subsystem (marked in bold in Table 5.2) and "Device#" is the one reported in Table 5.1. Note that the device numbering scheme in Table 5.1 is different from the one used in the JTAG chain (Table 4.25).

Since the configuration file for a particular device is used in five boards the subrack controller command sequence take advantage of the "Mixer Board # Broadcasting" feature (paragraph 4.5 and Table 4.4). This feature allows for writing configuration data contemporaneously to five boards.

A few steps need to be followed in order to correctly generate the configuration files:

- a) *Bit file generation.*
Virtex devices use the default configuration options, with CCLK as startup-clock. Spartan devices need some more attention. The parallel configuration used for them is called "Express Mode" and a user configuration template must be defined for it using the "Template Manager" utility. The template can be named "Express_Mode" and should contain the following options for the bitgen executable: "-g ExpressMode:Enable -g CRC:Disable". The newly defined "Express_Mode" configuration template should then be selected in the design>option>configuration menu before generating the bit file.
- b) *Bit files conversion to HEX files.*
Bit files need to be converted in HEX files using the Xilinx PROM File Formatter utility. The following options must be used.
PROM File Format: HEX;
Value used to calculate checksum: 00;
Swap bits: ON.
- c) *HEX ASCII files conversion to HEX binary.*
Xilinx HEX files are ASCII representation of binary data. They must be converted to binary format. This can be done using the HEX2BIN utility [Ref. 5].
- d) *File naming and copying to CompactFlash.*
The last step is to organize the files with the naming convention of Table 5.1 and copy them to the CompactFlash card (see Paragraph 14.2).

In order for the device to be configured, the subrack controller should be provided with files containing the sequence of configuration commands. The content of the two standard command files is reported in Paragraph 14.2.2. A list of available commands is available in Paragraph 14.3.

6. Monitoring and Debugging features

6.1 Front Panel LEDs

The front panel accommodates sixteen bicolor LEDs numbered from 0 to 15 and two red LEDs (see

Figure 6.1). The red LEDs are powered by the 3.3 Volt supply and 2.5 Volt on-board regulator. The bicolor LEDs are controlled by the FPGAs and allow monitoring of the state of several signals. The reset push button is used to select the set of signal to be displayed by the LEDs. At power up, the default set is set number twelve. Pushing the reset button (for less then two seconds) allows the user to select the next set. Immediately after the reset button is pushed the LEDs will indicate for about two seconds the selected set of signal that will be displayed. Pressing the reset button for more then two seconds forces the mixer board to reset.

If not specified otherwise, the LED use is as follows: green LED ON if signal is in a logic low state, red LED ON if signal is in a logic high state. Each LED is controlled by it's own state machine which stretches the signal driving the LED to a minimum of 150msec in order to make it visible to the human eye. If a signal is continuously changing both the green and red LEDs will be ON resulting in a yellow color.

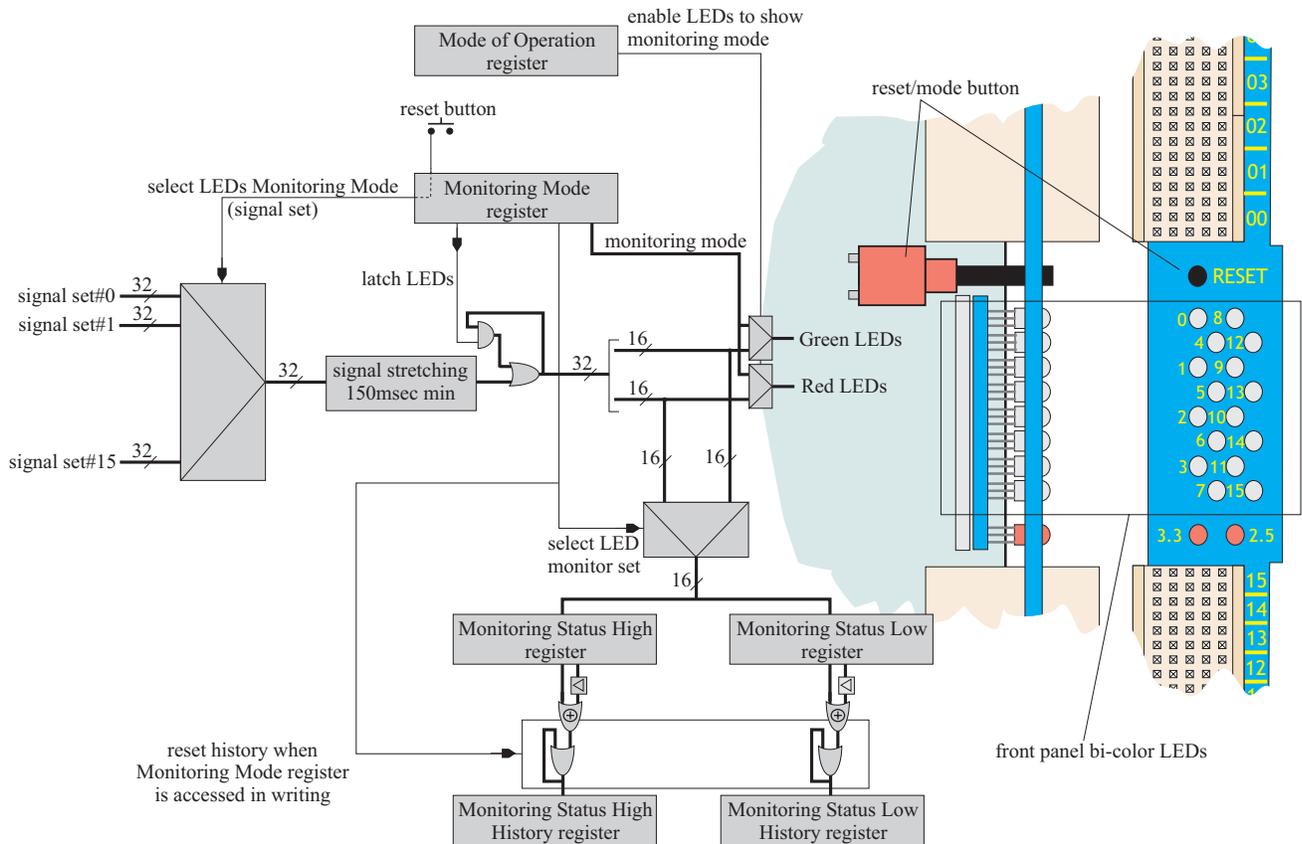


Figure 6.1, Front panel LEDs and LEDs monitoring mode

The following tables describe the sixteen available sets of signals (or monitoring modes).

LED#	Led Use. This set is used to monitor the input links clocks and DLLs. Link clock: Green LED ON if clock present, clock frequency is $45\text{MHz} < f < 55\text{MHz}$ and clock DLL is locked. Red LED-ON otherwise.
15..0	Link #15 to Link#0 clock status.

Table 6.1, LED's set #0 (input links clock and DLLs status).

LED#	Led Use. This set is used to monitor the SYNC bit (data frame synchronization bit located on the LSb of each LVDS link). The link's own clock is used as timing reference. Green LED ON only if the SYNC bit is present and is respecting the protocol (one and only one high bit every seven clock cycles). Red LED ON otherwise.
15..0	Link #15 to Link#0 sync bit status.

Table 6.2, LED's set #1 (input links SYNC bit status).

LED#	Led Use. This set is used to check the presence on the input links of a walking one test pattern. The pattern is specified in Paragraph 11. The link's own clock is used as timing reference. Green LED ON if the walking one pattern is detected, Red LED ON otherwise.
15..0	Link #15 to Link#0 walking one test pattern presence.

Table 6.2, LED's set #2 (input links Walking 1 test pattern detection).

LED#	Led Use. This set is used to check the presence on the input links of a walking zero test pattern. The pattern is specified in Paragraph 11. The link's own clock is used as timing reference. Green LED ON if the walking zero pattern is detected, Red LED ON otherwise.
15..0	Link #15 to Link#0 walking zero test pattern presence.

Table 6.3, LED's set #3 (input links Walking 0 test pattern detection).

LED#	Led Use. This set is used to monitor the SYNC bit (data frame synchronization bit located on the LSb of each LVDS link) after the synchronization process. The Global Clock is used as timing reference. Green LED ON only if the SYNC bit is present and is respecting the protocol (one and only one high bit every seven clock cycles). Red LED ON otherwise.
15..0	Link #15 to Link#0 sync bit status after synchronization.

Table 6.2, LED's set #4 (input links SYNC bit status after synchronization).

LED#	Led Use. This set is used to monitor the synchronization of the input links frames with the global sync. A link data frame is considered synchronized when the SYNC bit is in received in the same frame time slot as the SYNC bit used as timing reference (usually the SYNC received on link#0 of Mixer board #1). Green LED ON if link data frames are synchronized, Red LED ON otherwise.
15..0	Link #15 to Link#0 synchronization status.

Table 6.4, LED's set #5 (input links frame synchronization status).

LED#	Link #0 Output links Test Pattern detection. It is used to test the mixer output link when they are sending the test pattern. The test pattern transmission can be enabled through the Output Links Test Mode registers. The output links test pattern is specified in Paragraph 11. A 28 bit type LVDS cable should be used to loop-back one of the output links to the link#0 input link. Green LED ON if the pattern is detected, Red LED ON otherwise.
0	pattern detection.
1..15	not used, always OFF.

Table 6.5, LED's set #6 (Output links test pattern detection).

LED#	Input links control bits stream monitoring. Each LED is driven by the sequence of seven data bits received on a particular link. If a LED is red it means that the control bits on that link are always high ('1'), if the LED is green the control bits are always low ('0'). If the LED is orange it means that on that link some control bits are high and some are low or that at least one control bit is changing status. By default all the control bits are monitored, but a mask can be set in the "Monitoring Mode 7 Mask registers" (See 7.1.12) to monitor only a subset of control bits.
15..0	Link #15 to Link #0 control bits stream.

Table 6.6, LED's set #7 (Input links control bits stream monitoring).

LED#	Mixer Board local bus monitoring. This set is used to monitor the local bus data, address and control signals. When FPGAs device access operations are enabled (see Paragraph for an example) this monitoring mode can be used to view the content of FPGA's internal registers directly on the front panel LEDs. This is because when device access is enabled the local bus is driven with the content of FPGAs internal registers.
0	Local Data Bus bit 0 (FDAT0).
1	Local Data Bus bit 1 (FDAT1).
2	Local Data Bus bit 2 (FDAT2).
3	Local Data Bus bit 3 (FDAT3).
4	Local Data Bus bit 4 (FDAT4).
5	Local Data Bus bit 5 (FDAT5).
6	Local Data Bus bit 6 (FDAT6).
7	Local Data Bus bit 7 (FDAT7).
8	Local Data Bus read/write (/WRITE).
9	Local Bus Address Strobe (ASTRB) and FPGAs /INIT.
10	Local Bus Data Strobe (DSTRB).
11	FPGAs /PROGRAM (/PROGRAM).
12	FPGAs Configuration Clock (CONFIGCLK), green LED ON if clock is present, red LED ON if is absent.
13	Local Bus Transceiver enable (/CONFIGDAT EN).
14	Local Bus Transceiver direction (/CONFIGDAT DIR). '1' FPGAs to Board Controller, '0' Board Controller to FPGAs.
15	FPGA Global Clock (FPGACK10), green LED ON if clock is present, red LED ON if is absent.

Table 6.7, LED's set #8 (Mixer Board local bus monitoring).

LED#	Backplane serial bus and A16:D8 control signals monitoring. This set is used to monitor the A16:D8 general purpose bus control signals and the slow monitoring serial bus part of the backplane interfaces between the Mixer Board and the subrack controller.
0	SYSCLOCK (green LED ON if clock is present, red LED if clock is absent).
1	Address STRoBe (AS).
2	WRITE (WRITE).
3	Data Transfer ACKnowledge (/DTACK).
4	Bus ERRor (/BERR).
5	SYSRESET (SYSRST).
6	Transceivers enable (/VDAT_EN).
7	Transceiver direction (VDAT_DIR).
8	Serial Link Reset (STAT_RST).
9	Serial Link Clock (STAT_CLK), green LED ON if clock is present, red LED if clock absent.
10	Serial Link Data (STAT_DAT[n]).
11	Broadcast addressing.
12	Not Standard Mode (from Slow Monitoring register).
13	Input Links Error (from Slow Monitoring register)
14	Global Clock/SYNC Error (from Board Status/Control register)
15	Global Clock/SYNC Error history (from Board Status/Control register)

Table 6.8, LED's set #9 (Backplane serial bus and A16:D8 bus control signals monitoring).

LED#	Led Use. This set is used to monitor the backplane address bus part of the A16:D8 general purpose bus interface between the Mixer Board and the subrack controller.
0..15	Address bit 0 (BADDR0) to Address bit 15 (BADDR15).

Table 6.5, LED's set #10 (Backplane A16:D8 general purpose bus address signals monitoring).

LED#	This set is used to monitor the backplane data and geographical address signals part of the A16:D8 general purpose bus interface between the Mixer Board and the subrack controller.
0	Data bit 0 (BDAT0).
1	Data bit 1 (BDAT1).
2	Data bit 2 (BDAT2).
3	Data bit 3 (BDAT3).
4	Data bit 4 (BDAT4).
5	Data bit 5 (BDAT5).
6	Data bit 6 (BDAT6).
7	Data bit 7 (BDAT7).
8	Slot Address bit 0 (MOD_ID0).
9	Slot Address bit 1 (MOD_ID1).
10	Slot Address bit 2 (MOD_ID2).
11	Slot Address bit 3 (MOD_ID3).
12	Slot Address bit 4 (MOD_ID4).
13	Not used, always OFF.
14	Not used, always OFF.
15	Not used, always OFF.

Table 6.5, LED's set #11 (A16:D8 general purpose bus data and slot address signals monitoring).

LED#	This set is used to verify the configuration of 16 of the 17 FPGAs of a Mixer Board. The only FPGA not considered is the Board Controller which is automatically configured at power-up by an EPROM. Green: FPGA configured correctly. Red: FPGA not configured. The name in parenthesis is the one used on the board electrical schematic.
0	Configuration Done BE DFE1 Yellow-Purple FPGA (DONE11).
1	Configuration Done BE DFE1 Red-Blue FPGA (DONE12).
2	Configuration Done BE DFE1 Orange-Green FPGA (DONE13).
3	Configuration Done BE DFE0 Red-Blue FPGA (DONE14).
4	Configuration Done BE DFE0 Orange-Green FPGA (DONE15).
5	Configuration Done BE DFE0 Yellow-Purple FPGA (DONE16).
6	Configuration Done FE LinkIn13..15 FPGA (DONE1).
7	Configuration Done FE LinkIn4..6 FPGA (DONE2).
8	Configuration Done FE LinkIn1..3 FPGA (DONE3).
9	Configuration Done FE LinkIn10..12 FPGA (DONE4).
10	Configuration Done FE LinkIn0 FPGA (DONE5).
11	Configuration Done Backplane Left Driver FPGA (DONE6).
12	Configuration Done FE LinkIn7..9 FPGA (DONE7).
13	Configuration Done Backplane DFE0 Receiver FPGA (DONE8).
14	Configuration Done Backplane DFE1 Receiver FPGA (DONE9).
15	Configuration Done Backplane Right Driver FPGA (DONE10).

Table 6.6, LED's set #12 (Default mode, FPGA configuration status).

LED#	Output Links Test Mode Enable status.
0	DFE 0 Green Link (00) status.
1	DFE 0 Green Link (01) status.
2	DFE 0 Orange Link (02) status.
3	DFE 0 Purple Link (03) status.
4	DFE 0 Yellow Link (04) status.
5	DFE 0 Blue Link (05) status.
6	DFE 0 Red Link (06) status.
7	DFE 0 Red Link (07) status.
8	DFE 1 Green Link (10) status.
9	DFE 1 Green Link (11) status.
10	DFE 1 Orange Link (12) status.
11	DFE 1 Purple Link (13) status.
12	DFE 1 Yellow Link (14) status.
13	DFE 1 Blue Link (15) status.
14	DFE 1 Red Link (16) status.
15	DFE 1 Red Link (17) status.

Table 6.7, LED's set #13 (Output Links Test Mode Enable status).

LED#	Input Links Error Status. This set is used to monitor the input links status using the same signals driving Input Links Error Status registers (0x05, 0x06).
15..0	<p>Status of the input links #15 (bit 15) to #0 (bit 0). A high value ('1', red LED ON) indicates that the corresponding input link has one of the following critical errors:</p> <ol style="list-style-type: none"> 1) Link clock: missing or out of frequency range (45MHZ to 55MHZ) or Delay Locked Loop not locked; 2) Link frame marker (SYNC) before synchronization: missing or not respecting the protocol (one and only one high bit every seven clock cycles); 5) Link frame marker (SYNC) after synchronization: missing or not respecting the protocol (one and only one high bit every seven clock cycles); 6) Link frame synchronization: the frames are not synchronized with those of the reference link (usually link#0 on the first board (master) in the mixer subsystem (group of four boards handling the data from one supersector)).

Table 6.7, LED's set #14 .(Input Links Error Status).

LED#	Led Test. This set is used to check that all the LEDs are functioning.
15..0	Both Green and Red LEDs are always ON (Orange light).

Table 6.7, LED's set #15 (LED Test).

7. Appendix A – Devices registers

The board controller internal registers allow for most of the user controls needed during normal system operations. Beside the board controller there are sixteen FPGAs on a mixer board and each one has internal registers. These registers allow access to advanced features generally used for diagnostic purposes during system debugging, testing and commissioning. These features can also be utilized periodically to test system operations or in the event of a malfunction.

7.1 FrontEnd Devices

Table 7.1 lists the internal registers of the six front-end FPGAs. The address specified in the first column refers to the FPGA internal address and is the one to be used in the Device Access Address register. Please refer to Paragraph 4.5.12 for more information on the Device Access Structure. The table is followed by a description of each of the registers.

Register address	Register name and use.	IN0 [Dev# 1010b]	IN1..3 [Dev# 1000b]	IN4..6 [Dev# 0111b]	IN7..9 [Dev# 1100b]	IN10..12 [Dev# 1001b]	IN13..15 [Dev# 0110b]
0x00	Device Firmware	X	X	X	X	X	X
0x01	Link pointer	X	--	--	--	--	--
0x02..0x0F	--	--	--	--	--	--	--
0x10	Link Status A (Read-Only)	Link#0	Link#1	Link#4	Link#7	Link#10	Link#13
0x11	Link Status B (Read-Only)	Link#0	Link#1	Link#4	Link#7	Link#10	Link#13
0x12	Link Control (Read/Write)	Link#0	Link#1	Link#4	Link#7	Link#10	Link#13
0x13	Frame Sync Status (Read-Only)	Link#0	Link#1	Link#4	Link#7	Link#10	Link#13
0x14	Frame Sync Status History (Read-Only)	Link#0	Link#1	Link#4	Link#7	Link#10	Link#13
0x15	Monitoring Mode 7 Mask	Link#0	Link#1	Link#4	Link#7	Link#10	Link#13
0x16	Link Control Bits Status	Link#0	Link#1	Link#4	Link#7	Link#10	Link#13
0x17..0x1F	--	--	--	--	--	--	--
0x20	Link Status A (ReadOnly)	--	Link#2	Link#5	Link#8	Link#11	Link#14
0x21	Link Status B (ReadOnly)	--	Link#2	Link#5	Link#8	Link#11	Link#14
0x22	Link Control (Read/Write)	--	Link#2	Link#5	Link#8	Link#11	Link#14
0x23	Frame Sync Status (Read-Only)	--	Link#2	Link#5	Link#8	Link#11	Link#14
0x24	Frame Sync Status History (Read-Only)	--	Link#2	Link#5	Link#8	Link#11	Link#14
0x25	Monitoring Mode 7 Mask	--	Link#2	Link#5	Link#8	Link#11	Link#14
0x26	Link Control Bits Status	--	Link#2	Link#5	Link#8	Link#11	Link#14
0x27..0x2F	--	--	--	--	--	--	--
0x30	Link Status A (Read-Only)	--	Link#3	Link#6	Link#9	Link#12	Link#15
0x31	Link Status B (Read-Only)	--	Link#3	Link#6	Link#9	Link#12	Link#15
0x32	Link Control (Read/Write)	--	Link#3	Link#6	Link#9	Link#12	Link#15

0x33	Frame Sync Status (Read-Only)	--	Link#3	Link#6	Link#9	Link#12	Link#15
0x34	Frame Sync Status History (Read-Only)	--	Link#3	Link#6	Link#9	Link#12	Link#15
0x35	Monitoring Mode 7 Mask	--	Link#3	Link#6	Link#9	Link#12	Link#15
0x36	Link Control Bits Status	--	Link#3	Link#6	Link#9	Link#12	Link#15
0x37..0x3F	--	--	--	--	--	--	--
0x40	Control bits masking	Link#0	--	--	--	--	--
0x41	Control bits masking	Link#1	--	--	--	--	--
0x42	Control bits masking	Link#2	--	--	--	--	--
0x43	Control bits masking	Link#3	--	--	--	--	--
0x44	Control bits masking	Link#4	--	--	--	--	--
0x45	Control bits masking	Link#5	--	--	--	--	--
0x46	Control bits masking	Link#6	--	--	--	--	--
0x47	Control bits masking	Link#7	--	--	--	--	--
0x48	Control bits masking	Link#8	--	--	--	--	--
0x49	Control bits masking	Link#9	--	--	--	--	--
0x4A	Control bits masking	Link#10	--	--	--	--	--
0x4B	Control bits masking	Link#11	--	--	--	--	--
0x4C	Control bits masking	Link#12	--	--	--	--	--
0x4D	Control bits masking	Link#13	--	--	--	--	--
0x4E	Control bits masking	Link#14	--	--	--	--	--
0x4F	Control bits masking	Link#15	--	--	--	--	--
0x50	Input Links Control bits status at Link0 FPGA	Link#15..0	--	--	--	--	--
0x51	EC bits status	X	--	--	--	--	--
0x52	ECS bits status	X	--	--	--	--	--
0x53..0xFF	--	--	--	--	--	--	--

Table 7.1, Front-End devices registers.

7.1.1 Device Firmware Register

This register contains information about the FPGA/device accessed. It allows verifying which device is being accessed.

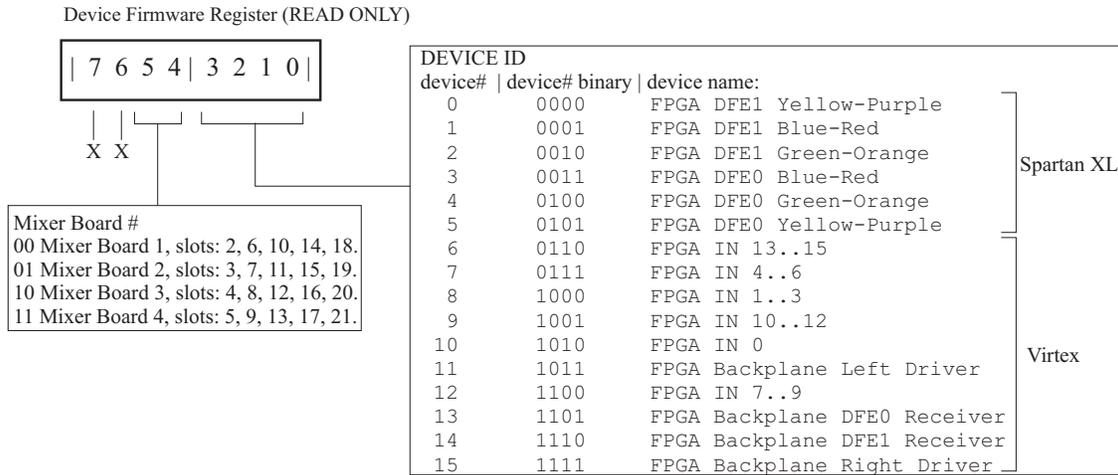


Figure 7.1, Device Firmware register.

7.1.2 Link pointer register

Allows selecting which link is to be monitored by some of the diagnostic. The diagnostic information can be read back through FPGA's internal registers. The content of these registers depends on the link pointed to by the "Link Pointer register". The four bits used as link pointer represent the link# in hexadecimal.

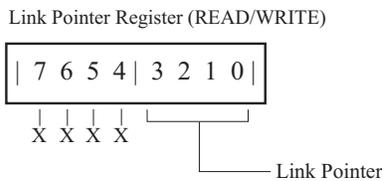


Figure 7.2, Link Pointer register

Currently only the "Input Links Control bits status at IN0 FPGA" register needs the Link pointer register.

7.1.3 Input Link Status registers

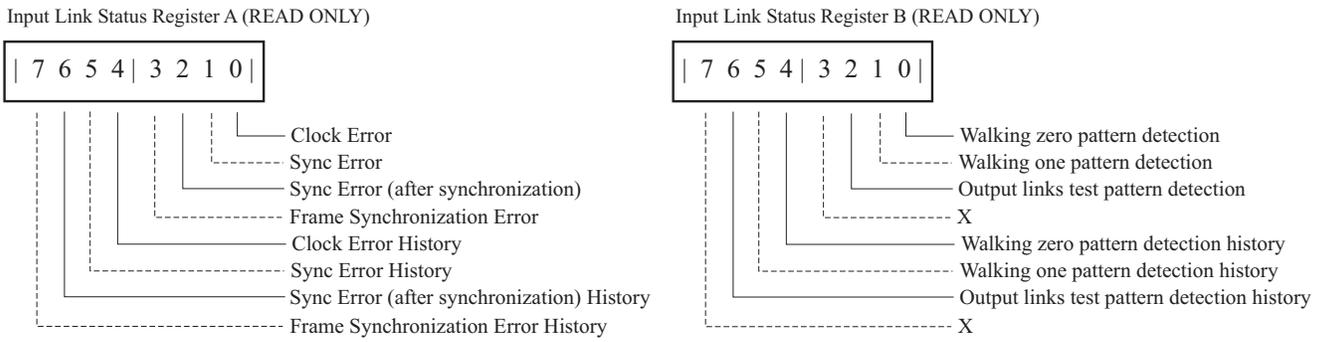


Figure 7.3, Input Link Status register.

7.1.4 Input Link Control register

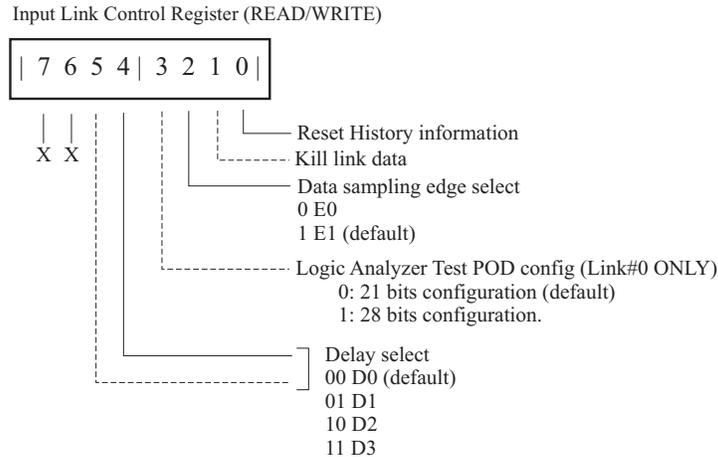


Figure 7.4, Input Link Control register

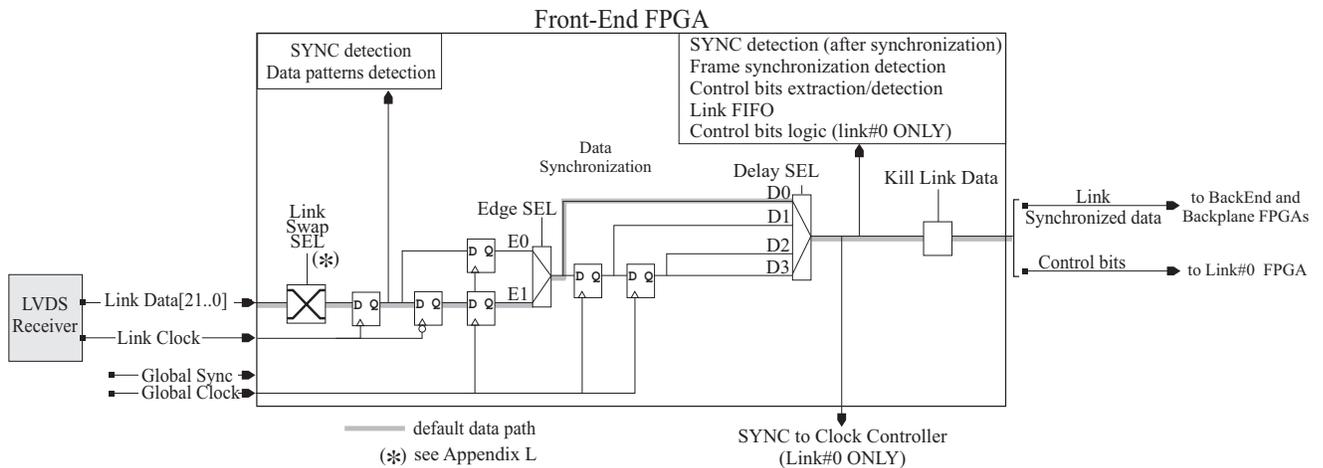


Figure 7.5, Data synchronization and link controls.

7.1.5 Frame Sync Status register

The frame synchronization register data is used to determine the link SYNC (link frame marker) position relative to the global SYNC. Its content is generated by sampling with the global SYNC signal the content of an 8bit long shift register fed by the link SYNC. When the data frames on a link are synchronized to the global SYNC all of the bits but the least and most significant will readback “0” (see Figure 7.7).

Frame Synchronization Status Register (READ ONLY)



Figure 7.6, Frame Synchronization Status register.

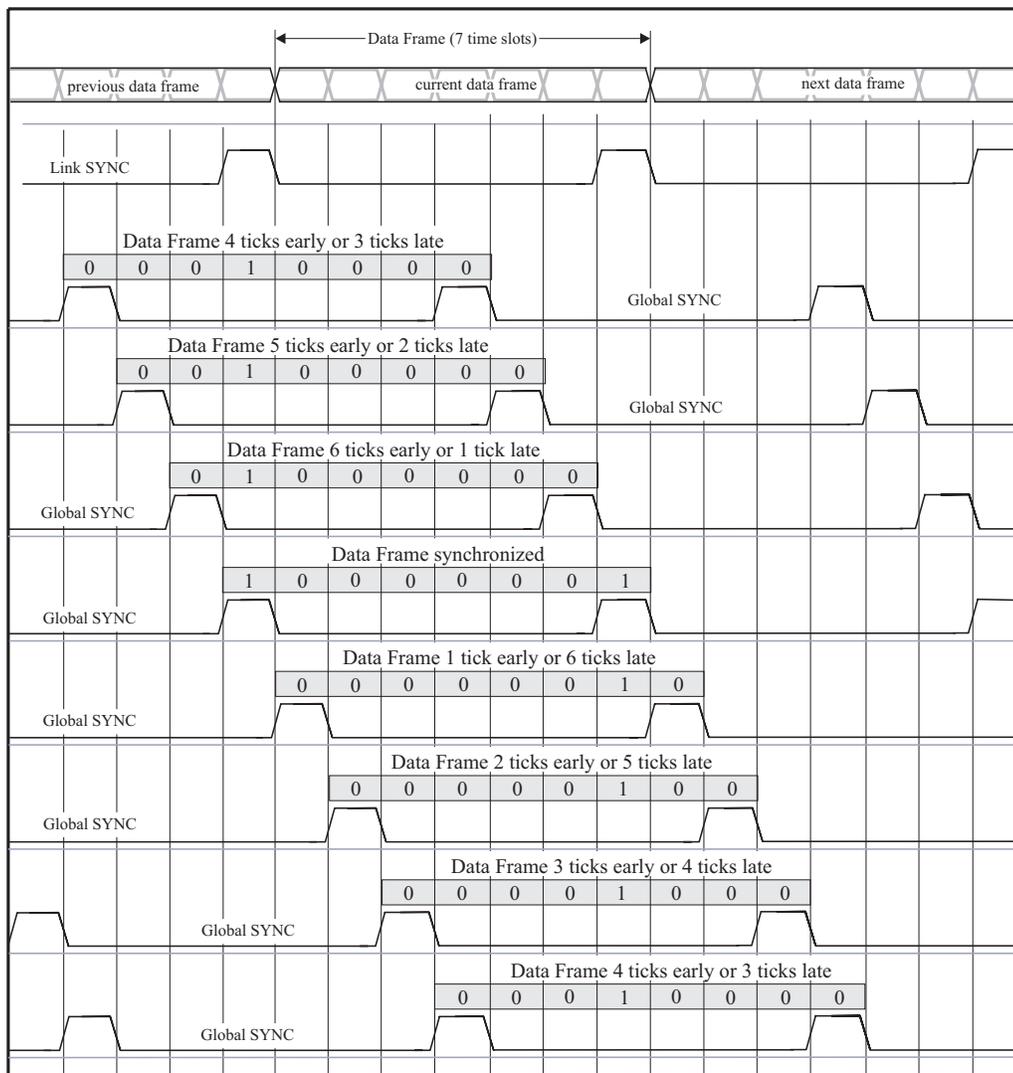


Figure 7.7, Frame Synchronization Status register content.

7.1.6 Frame Sync Status History register

The Frame Sync Status History register is used to keep track of the changes in the Frame Sync Status register. The register content is zero at power up or reset (or with the "reset history information" from Input Link Control register) and each of its bit is set and remain set to '1' if the corresponding bit in the Frame Sync Status register is '1'.

Frame Synchronization Status History Register (READ ONLY)

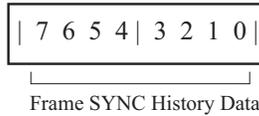


Figure 7.8, Frame Synchronization Status History register.

7.1.7 Input Link Control Bits Mask register

Each input link is preset to receive one control bit at each time slot embedded in the 7-time slot data stream, for a total of 7 control bits per link. The control bits from every link are sent to one FPGA (the Link#0 FPGA) where, at each time slot, they are all ORed and XORED to generate the Embedded Command (EC) and the Embedded Command Status (ECS) bit. The EC and ECS bits are then sent to the backend FPGAs to be embedded in some of the output data streams.

If any of the control bits are not sent by the front end electronics (AFEs) to the mixer, the missing control bits need to be masked on the Mixer boards in order to perform the OR and XOR operation only on the valid control bits. This masking is done in the Link#0 FPGA before the OR and XOR operation are performed. To allow this, there are 16 "input link control bits mask registers" for each input link on a mixer board. If any control bit needs to be masked, the corresponding bit in the masking register should be set to '0'. The default content of each of these registers is 0x01 for link#0 and 0xFF for all the other links. The reason for having all the control bits masked on input link#0 is that the data mapping done by the AFEs driving link#0 doesn't comply with the mixer design specification so the control bits aren't where the mixer would expect them.

Input Link Control Bits Mask Register (READ/WRITE)

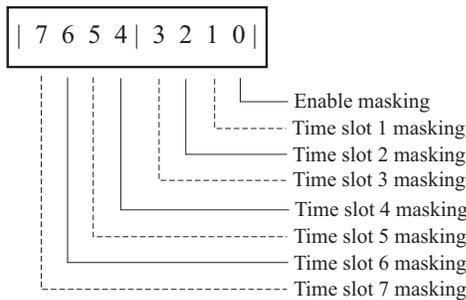
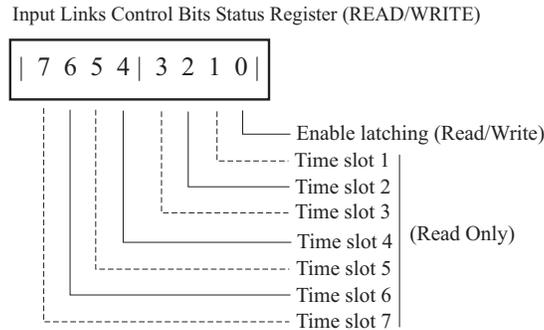


Figure 7.9, Input Link Control Bits Mask register.

7.1.8 Input Link Control Bits Status registers

Allows verifying of the presence of control bits on each of the sixteen input links. There is one of these registers for each input link.

The registers content reflects the control bits received on each link and is not affected by any control bits mask selection made in the "Input Link Control Bits Mask register".

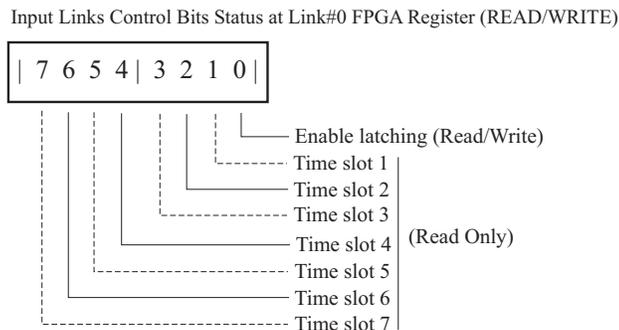


7.1.9 Input Link Control Bits Status at Link#0 FPGA register

Allows verifying of the presence of control bits from each of the sixteen input links at the Link#0 FPGA, which is the place where the control bits are combined to generate the Embedded Command and Embedded Command Status bits for the output data stream.

Only one link at a time can be monitored. The link to be monitored is selected in the "Link Pointer register" inside the IN0 FPGA (device# 0x0A). The register content reflects the control bits received on each link and is not affected by any control bits mask selection made in the "Input Link Control Bits Mask register". The register is NOT reset when the monitored link is changed. Because of this, after a link change and when the latching option (bit#0) is used there is the need to disable and re-enable it in order for the register to show the correct information.

This register will be probably removed in future firmware upgrades.



7.1.10 Embedded Command Bits status register

Allows verifying of the presence of the Embedded Command bits generated ORing the control bits received from the 16 input links.

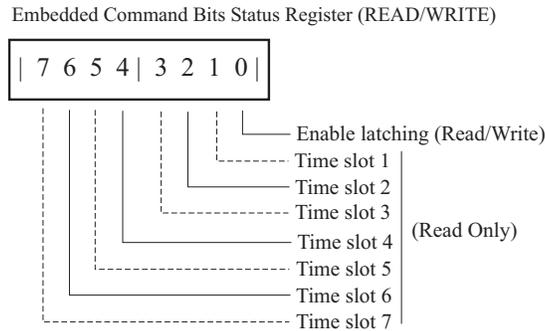


Figure 7.12, Embedded Command Bits Status Register.

7.1.11 Embedded Command Status Bits status register

Allows verifying of the presence of the Embedded Command Status bits generated XORing the control bits received from the 16 input links.

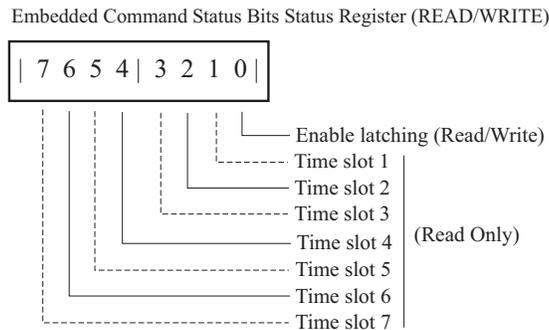


Figure 7.13, Embedded Command Status Bits Status Register.

7.1.12 Monitoring Mode 7 Mask register

Each input link is preset to receive one control bit at each time slot embedded in the 7-time slot data stream, for a total of 7 control bits per link. LED monitoring mode 7 (see Paragraph 6.1) allows seeing on the front panel LEDs the presence of the control bits data stream. The Monitoring Mode 7 Mask register allows individual masking on any input link for any set of control bits in order to have monitoring mode 7 shows the presence of a desired control bits subset. There are 16 "input link control bits mask registers", one for each input link on a mixer board. The default content of each of these registers is 0xFF. If any control bit needs to be masked, the corresponding bit in the masking register should be set to '0'.

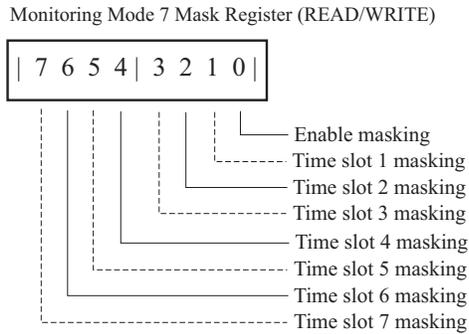


Figure 7.14, Monitoring Mode 7 Mask register.

7.2 Backplane Devices

Partially Implemented

Grayed blocks are not implemented.

Register address	Register name and use.	DFE0_RX [Dev# 1101b]	DFE1_RX [Dev# 1110b]	LEFT_DRV [Dev# 1011b]	RIGHT_DRV [Dev# 1111b]
0x00	Device Firmware	X	X	X	X
0x01	--	--	--	--	--
0x02	Device Control	X	X	X	X
0x03..0x6F	--	--	--	--	--
0x70	Clock DLL Error (Read-Only)	--	--	--	X
0x71	Clock Frequency Error (Read-Only)	--	--	--	X
0x72	SYNC Error (Read Only)	--	--	--	X
0x73	Clock/SYNC Select Status (Read Only)	--	--	--	X
0x74..0x7F	--	--	--	--	--
0x80	Backplane Driver Status (Read-Only)	--	--	X	X
0x81	Backplane Driver Control (Read/Write)	--	--	X	X
0x82..0x8F	--	--	--	--	--
0x90	Backplane Receiver Status (Read-Only)	X	X	--	--
0x91	Backplane Receiver Control (Read/Write)	X	X	--	--
0x92..0xFF	--	--	--	--	--

Table 7.2, Backplane Devices registers.

7.2.1 Device Firmware Register

See paragraph 7.1.1.

7.2.2 Device Control register

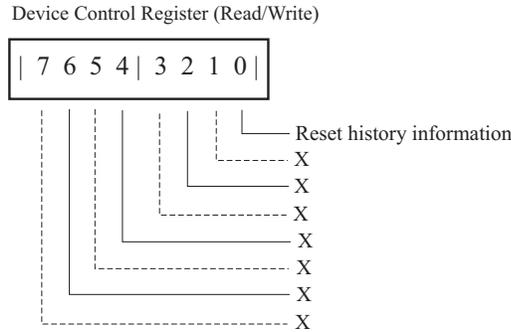


Figure 7.15, Device Control register

7.2.3 Clock DLL Error register

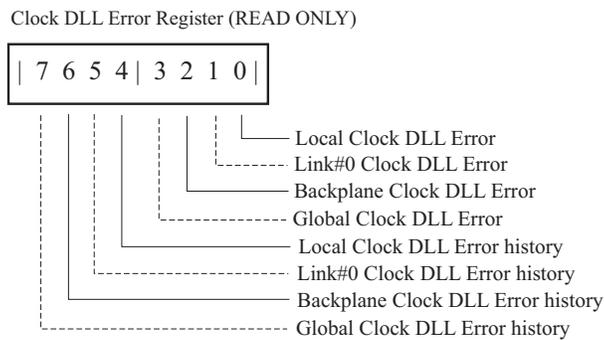


Figure 7.16, Clock DLL Error register.

7.2.4 Clock Frequency Error register

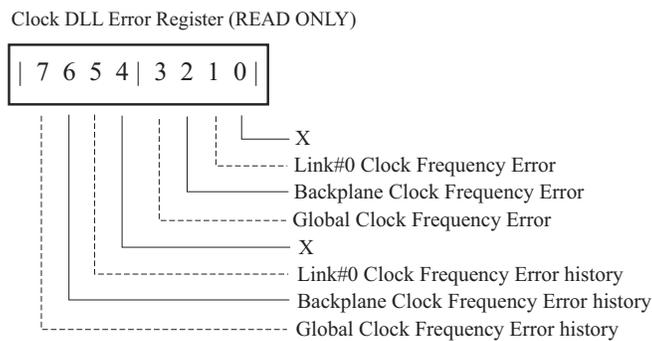


Figure 7.17, Clock Frequency Error register.

7.2.5 SYNC Error register

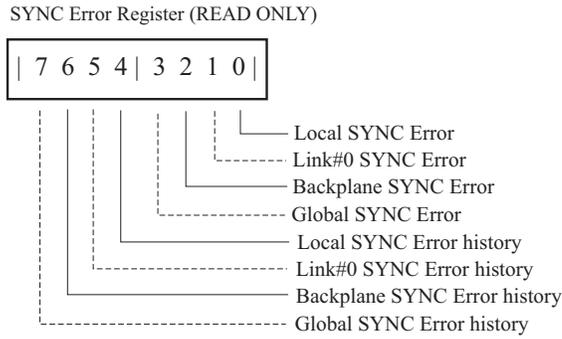


Figure 7.18, SYNC Error register

7.2.6 Clock/SYNC Select Status register

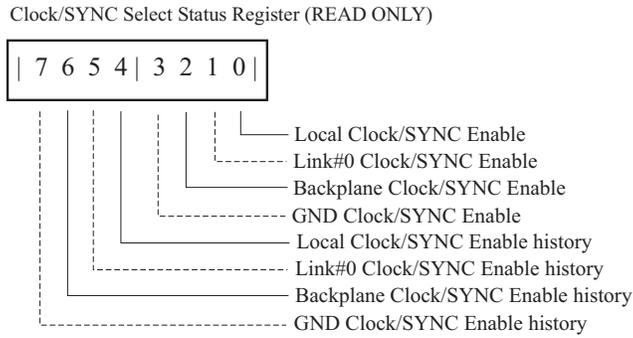


Figure 7.19, Clock/SYNC Select Status register

7.2.7 Backplane Driver Status register

NOT IMPLEMENTED

7.2.8 Backplane Driver Control register

NOT IMPLEMENTED

7.2.9 Backplane Receiver Status register

NOT IMPLEMENTED

7.2.10 Backplane Receiver Control register

NOT IMPLEMENTED

7.3 BackEnd Devices

Partially implemented, grayed blocks are not implemented.

Register address	Register name and use.	DFE0_GO [Dev# 0100b]	DFE0_YP [Dev# 0101b]	DFE0_BR [Dev# 0011b]	DFE1_GO [Dev# 0010b]	DFE1_YP [Dev# 0000b]	DFE1_BR [Dev# 0001b]
0x00	Device Firmware	X	X	X	X	X	X
0x01	--	--	--	--	--	--	--
0x02	Device Control	X	X	X	X	X	X
0x03..0x0F	--	--	--	--	--	--	--
0x10..0x9F	--	--	--	--	--	--	--
0xA0	Link Status	Green (00, 01)	Yellow (04)	Blue (05)	Green (10, 11)	Yellow (14)	Blue (15)
0xA1	Link Control	Green (00, 01)	Yellow (04)	Blue (05)	Green (10, 11)	Yellow (14)	Blue (15)
0xA2	Embedded Command Bits mask	--	--	X	--	--	X
0xA3..0xAC	--	--	--	--	--	--	--
0xAD	Link FIFO Memory Pointer	Green (00, 01)	Yellow (04)	Blue (05)	Green (10, 11)	Yellow (14)	Blue (15)
0xAE	Link FIFO Control	Green (00, 01)	Yellow (04)	Blue (05)	Green (10, 11)	Yellow (14)	Blue (15)
0xAF	Link FIFO Access	Green (00, 01)	Yellow (04)	Blue (05)	Green (10, 11)	Yellow (14)	Blue (15)
0xB0	Link Status	Orange (02)	Purple (03)	Red (06, 07)	Orange (12)	Purple (13)	Red (16, 17)
0xB1	Link Control	Orange (02)	Purple (03)	Red (06, 07)	Orange (12)	Purple (13)	Red (16, 17)
0xB2	Embedded Command Bits mask	X	--	--	X	--	--
0xB3..0xBC	--	--	--	--	--	--	--
0xBD	Link FIFO Memory Pointer	Orange (02)	Purple (03)	Red (06, 07)	Orange (12)	Purple (13)	Red (16, 17)
0xBE	Link FIFO Control	Orange (02)	Purple (03)	Red (06, 07)	Orange (12)	Purple (13)	Red (16, 17)
0xBF	Link FIFO Data	Orange (02)	Purple (03)	Red (06, 07)	Orange (12)	Purple (13)	Red (16, 17)
0xC0..0xFF	--	--	--	--	--	--	--

Table 7.3, BackEnd Devices registers.

7.3.1 Device Firmware Register

See paragraph 7.1.1.

7.3.2 Device Control Register

See paragraph 7.2.2.

7.3.3 Output Link Status register

NOT IMPLEMENTED

7.3.4 Output Link Control register

This register allows to shutdown the output link data stream and the output link SYNC bit. Some of the output links are used to transmit the Embedded Command and the Embedded Command Status bits (or control bits). These bits are not affected by the data stream shutdown, if desired they can be masked using the Embedded Command Bits Mask register.

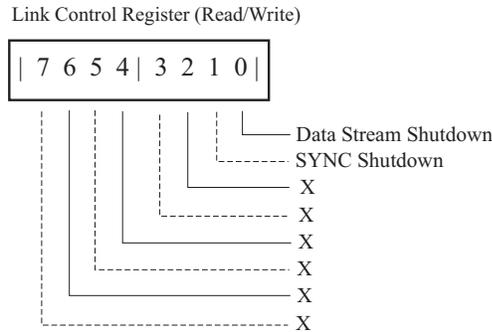


Figure 7.20, Link Control register

7.3.5 Output Link Embedded Command Bits Mask register

This register allows masking the control bits on the output links. Only 4 output links are carrying control bits, these are the orange (02, 12) and the blue (05, 15) links. The control bits can be masked independently on each of these links. The masking affects both the Embedded Command Bits (ECB) and the Embedded Command Status Bits (ECSB).

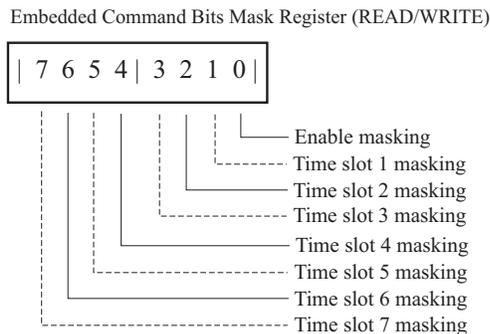


Figure 7.21, Embedded Command Bits Mask register.

7.3.6 Output Link FIFO

Each output link has a 32 bit wide FIFO that can be used to sample the data stream sent to the output link transmitters or to feed the output link transmitters with fake events to test the system downstream.

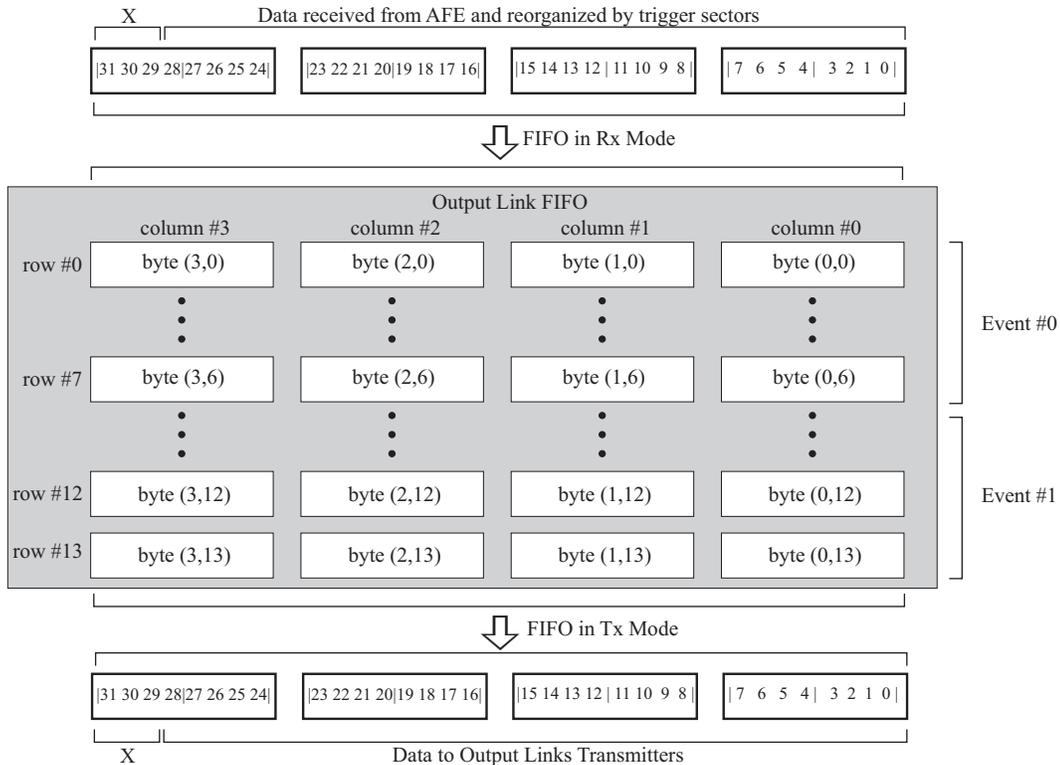


Figure 7.22, Output Link FIFO

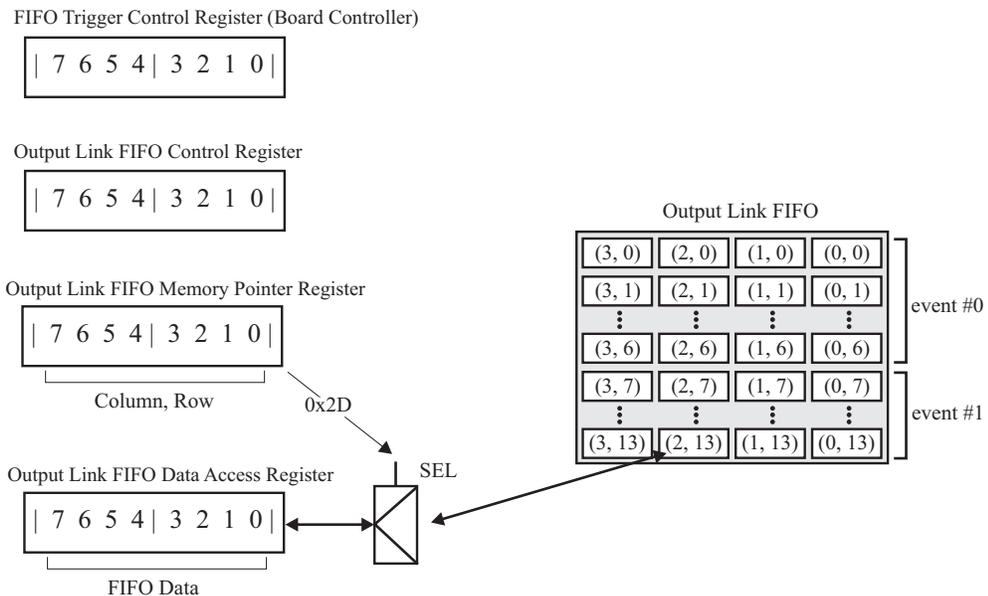


Figure 7.23, Output Link FIFO Access/Control Structure

7.3.8 Output Link FIFO Control register

This register is used to control the FIFO behavior.

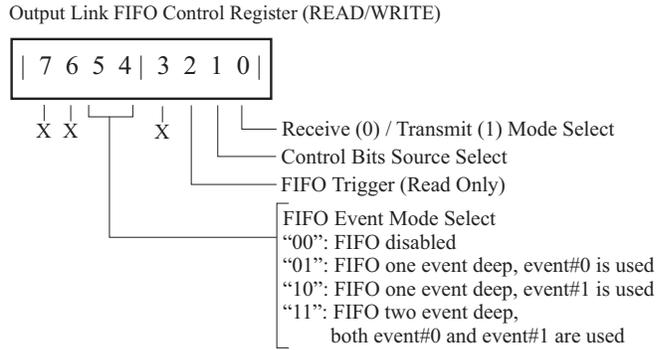


Figure 7.25, Output Link FIFO Control register

Bit#	Name (Type)	Interpretation
7..6	--	Not used.
5..4	FIFO Event Mode Select	The FIFO can operate in four event modes: "00": FIFO disabled, the trigger is ignored. "01": FIFO one event deep. Event #0 is used. "10": FIFO one event deep. Event#1 is used. "11": FIFO two event deep, both event #0 and #1 are used. The event mode affect both the receive and transmit mode of operation.
3	--	Not used
2	FIFO Trigger	Read Only. Is high when the FIFO is receiving a trigger signal from the board controller (FIFO Trigger Control register).
1	Control Bits Source Select	Some of the output links are used to transmit control bits together with the data stream. When the FIFO is operating in transmit mode and a trigger is received the content of the FIFO is used on the output link data stream and replace the data bits, the SYNC (frame marker) bit and the control bits. To avoid disrupting the control bit flow the Control Bits Source Select bit can be set high '1'.
0	Receive/Transmit Mode Select	Allow to select if the FIFO has to operate in Transmit ('0', default) or in Receive ('1') mode. The transmit mode allow to send the FIFO content on the output data stream. The receive mode is used to store portion of the data stream in the FIFO.

Table 7.4, Output Link FIFO Control Register.

7.3.9 Output Link FIFO Data Access register

This register allows to access in read/write the 56 byte-wide locations of the Output Link FIFO. When a trigger is active the write access is disabled and the value read is 0xFF.



Figure 7.26, Output Link FIFO Data Access register

8. Appendix B – Mixer Board detailed block diagrams

8.1 Mixer Board data flow from LVDS receivers to LVDS transmitters

Figure 8.1 shows a graphical sketch of the interconnections used by the bits of data flowing from the input links LVDS receivers to the output links LVDS transmitters. The PCB Interconnection Matrix block shows the number of connections between the output of the front-end FPGAs and the back-end FPGAs. Details of the interconnection matrix with the indication of which mixer firmware (Mixer 1 to Mixer 4) is used for a particular connection are reported in Chapter 9.

The link#0 Front-End FPGA performs more functions than the other front-end FPGAs. It receives and forwards to the clock controller (hosted by the backplane right driver FPGA) the link#0 clock. This is the clock used by the clock controller as first choice for the global clock (GCLK). The link#0 FPGA also receive the input links control bits, extracted from the data stream inside the front-end FPGAs, and generate two control bits used in some of the output links data streams. These output control bits are the Embedded Command bit (ECb) and the Embedded Command Status bit (ECSb).

Each of the back-end FPGAs has two sets of data inputs, one coming from the front-end FPGAs and one coming from the backplane FPGAs. The DFE0 (or plain color) back-end FPGAs receive backplane data only from the DFE0 backplane receiver, the DFE1 (or striped color) back-end FPGAs only from the DFE1 backplane receiver.

Each back-end FPGA produces and sends two unique data streams to the output links LVDS transmitters, but the green and red data streams are duplicated (they feed two LVDS transmitters).

Each of the backplane drivers feed a bus 41 bits wide that connects to the adjacent board to the right or to the left through the backplane. Each of the backplane receivers receives data from both right and left sides over an 82 bits wide bus.

All the FPGAs on the board receive the global clock (GCLK) and global SYNC (GSYNC) from the clock controller. The clock controller has the capability to choose between the backplane clock, the link#0 clock and the local clock.

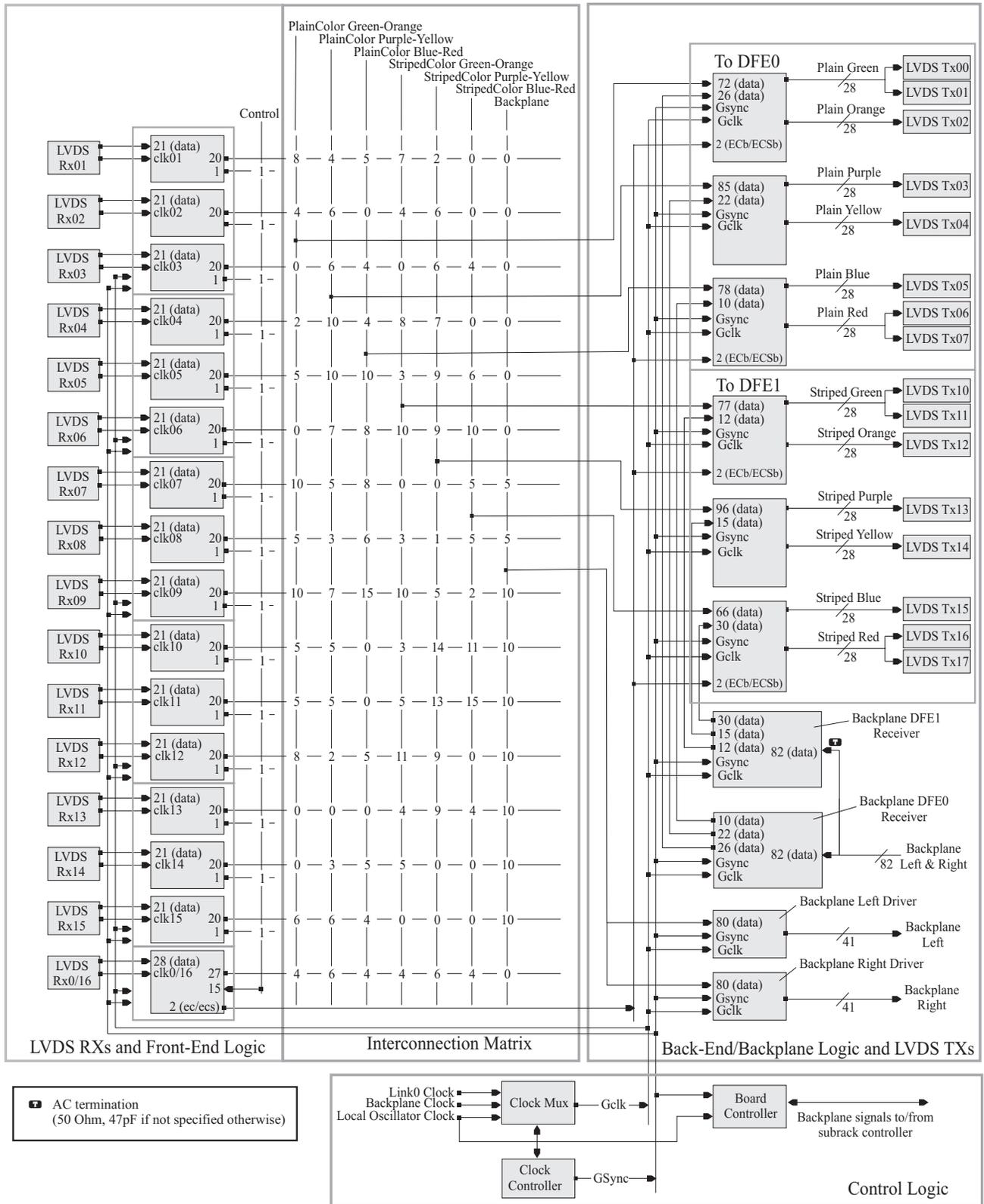


Figure 8.1, Mixer Board simplified data flow

8.2 Mixer Board Front-End FPGAs

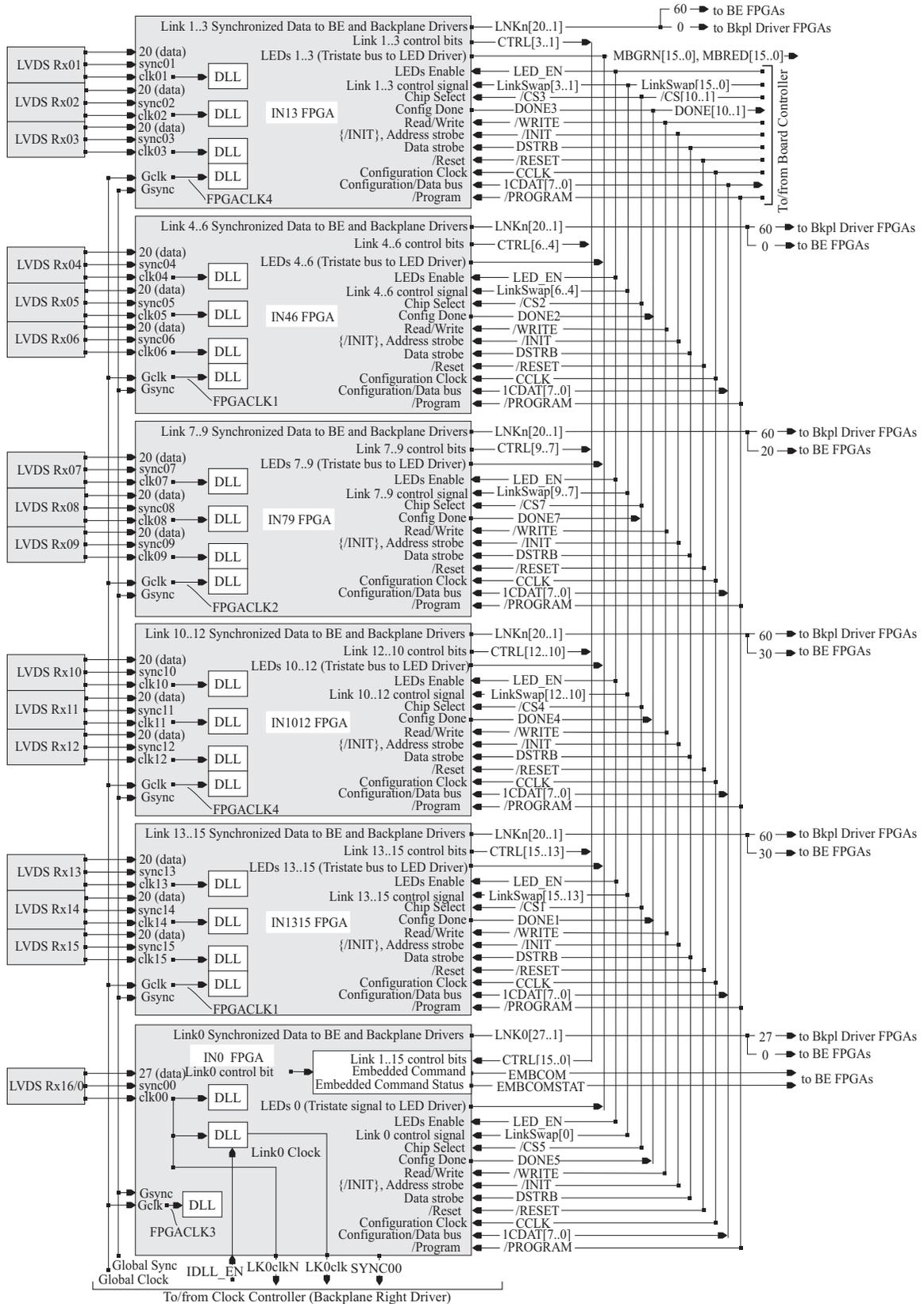


Figure 8.2, Mixer Board Front-End FPGAs

8.3 Mixer Board Back End FPGAs

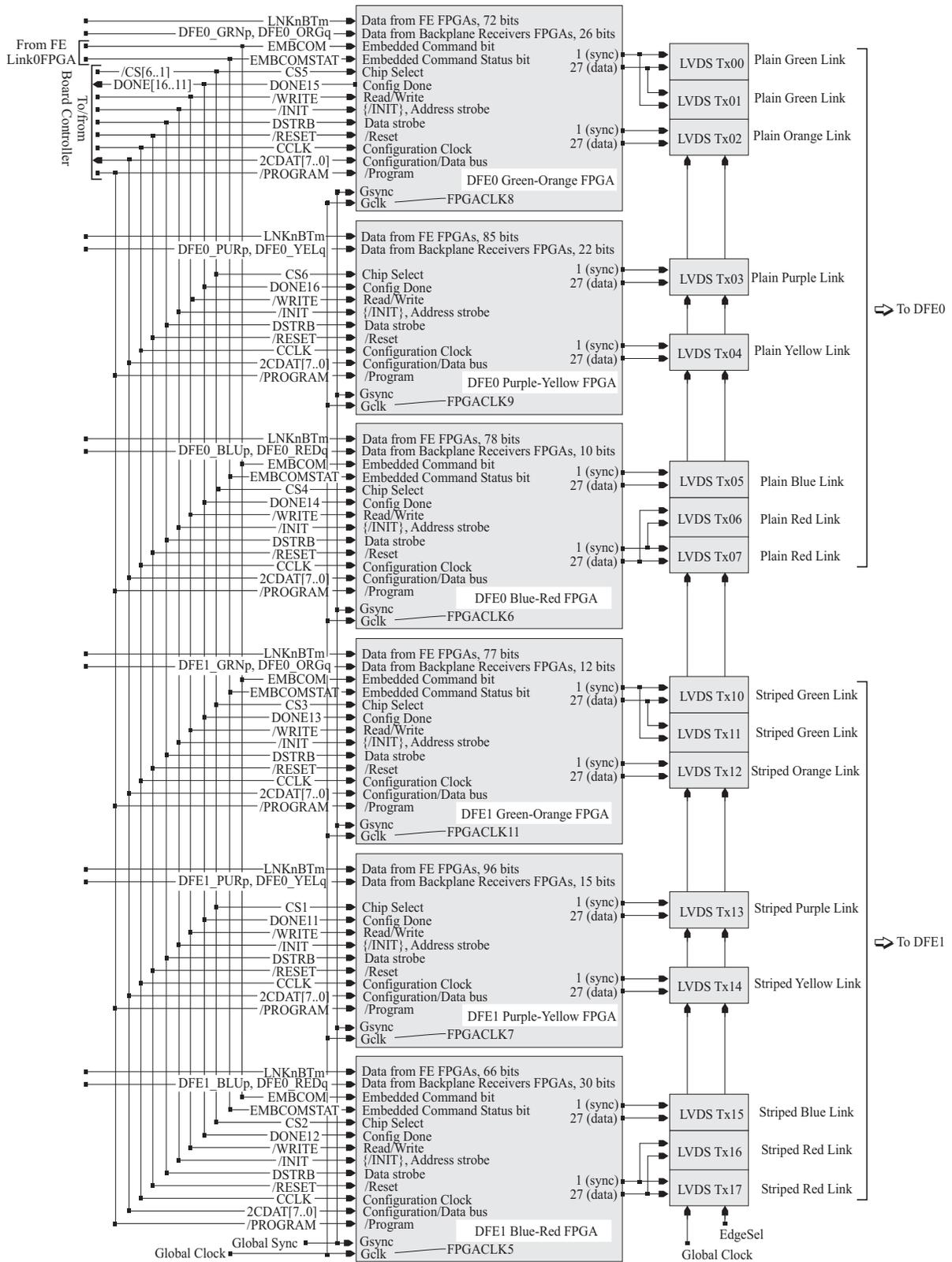


Figure 8.3, Mixer Board Back-End FPGAs

8.4 Mixer Board Backplane FPGAs

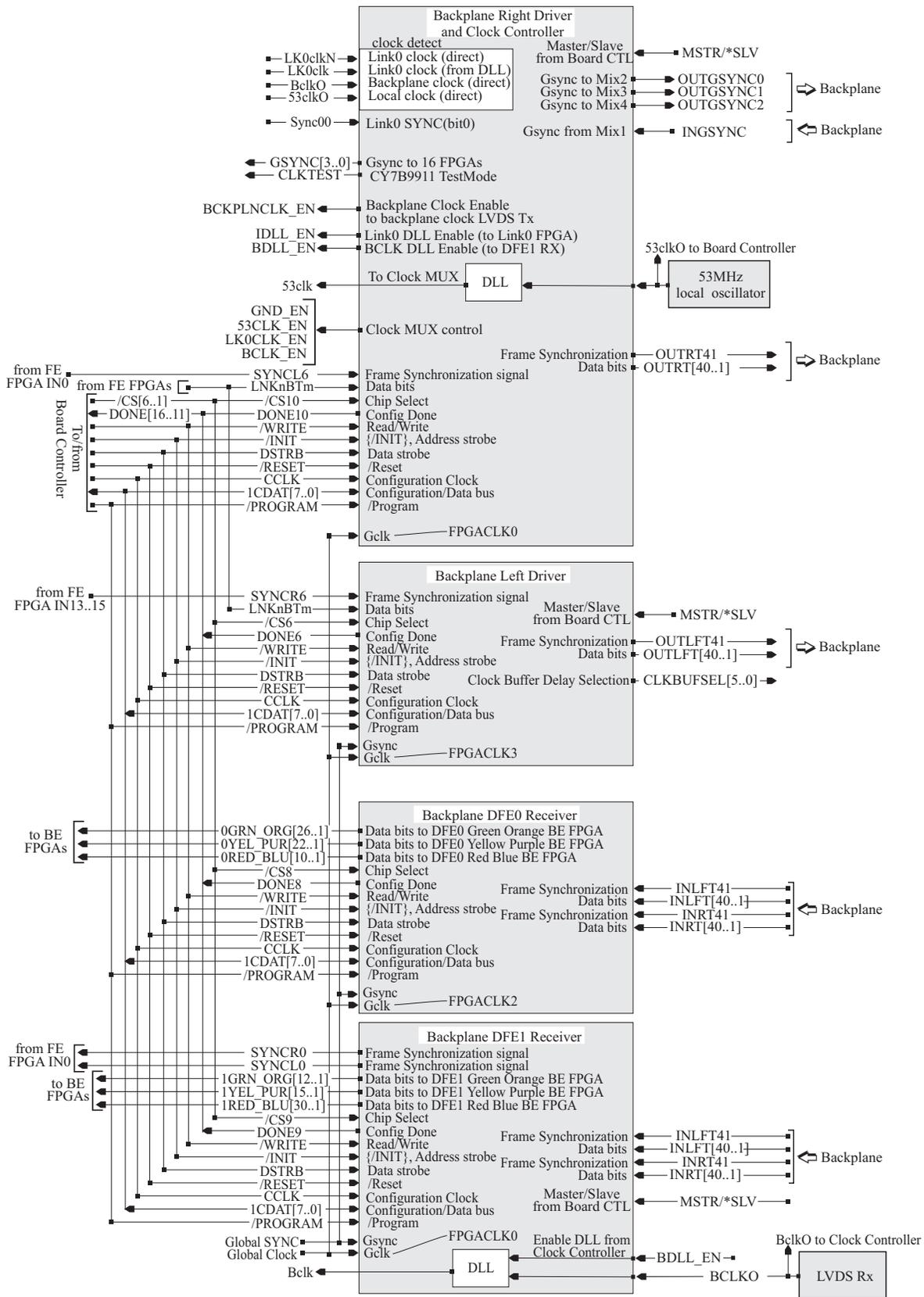


Figure 8.4, Mixer Board Backplane FPGAs

8.5 Control bits (inputs) and command bits (outputs)

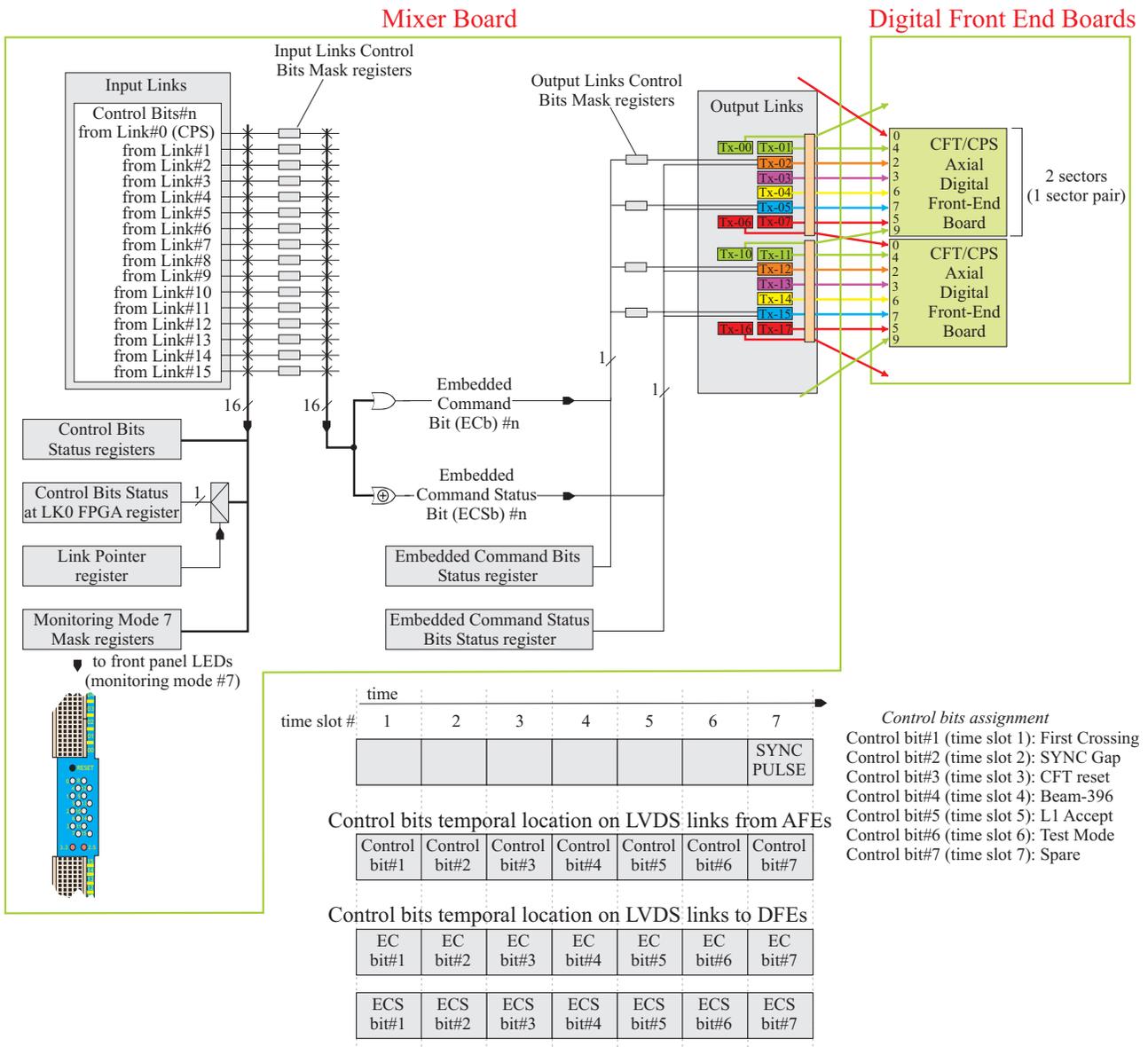


Figure 8.5, Command bits generation, timing and denomination.

8.6 Mixer Board Board-Controller

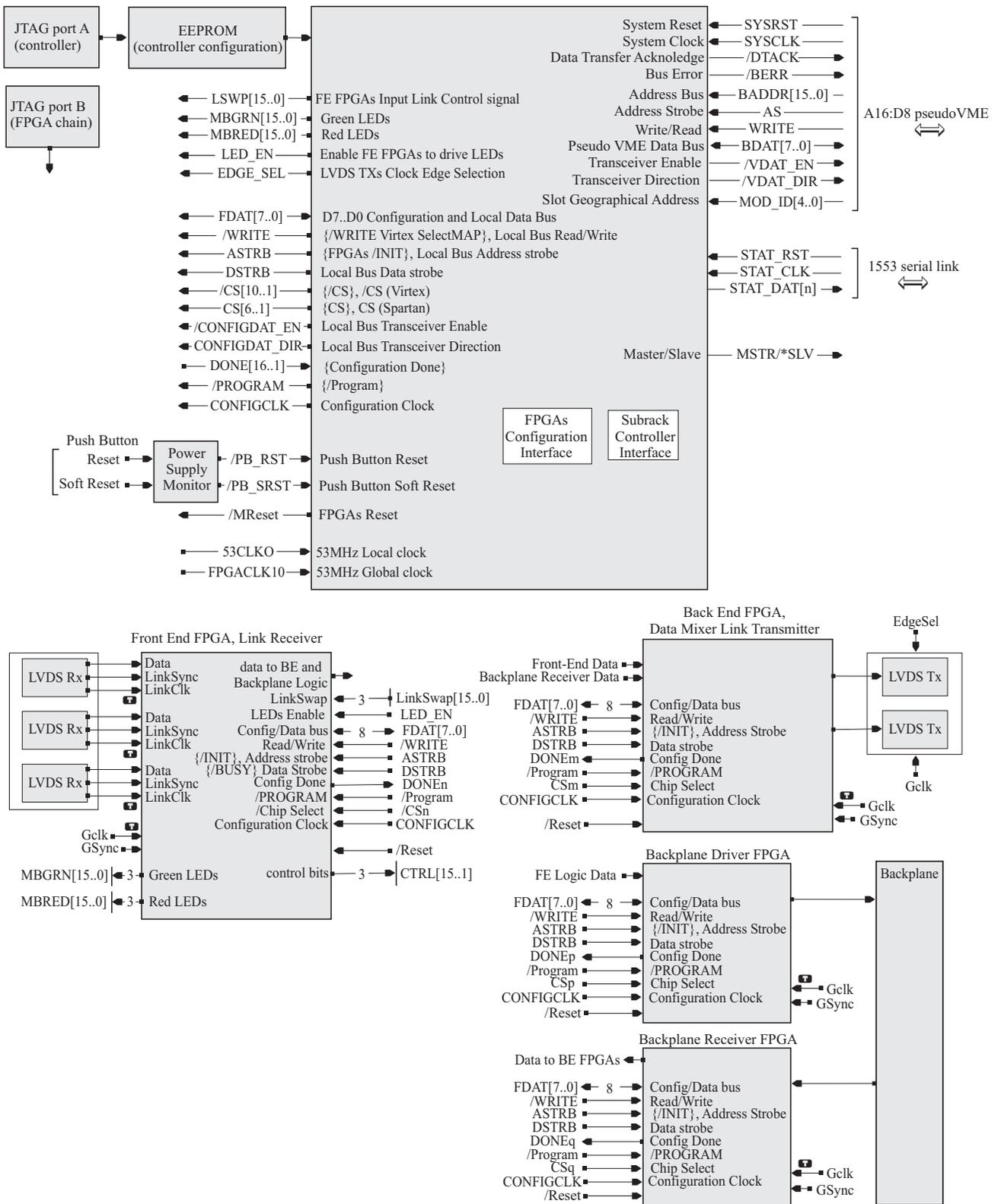


Figure 8.6, Mixer Board Controller

8.7 Mixer System Timing Signals Distribution

Clock and SYNC distribution is critical for the mixer system.

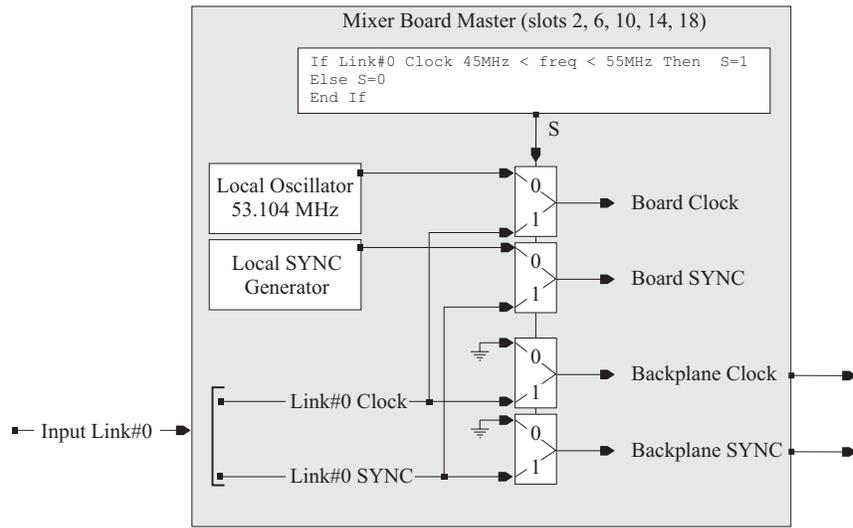


Figure 8.7, Mixer Master clock selection

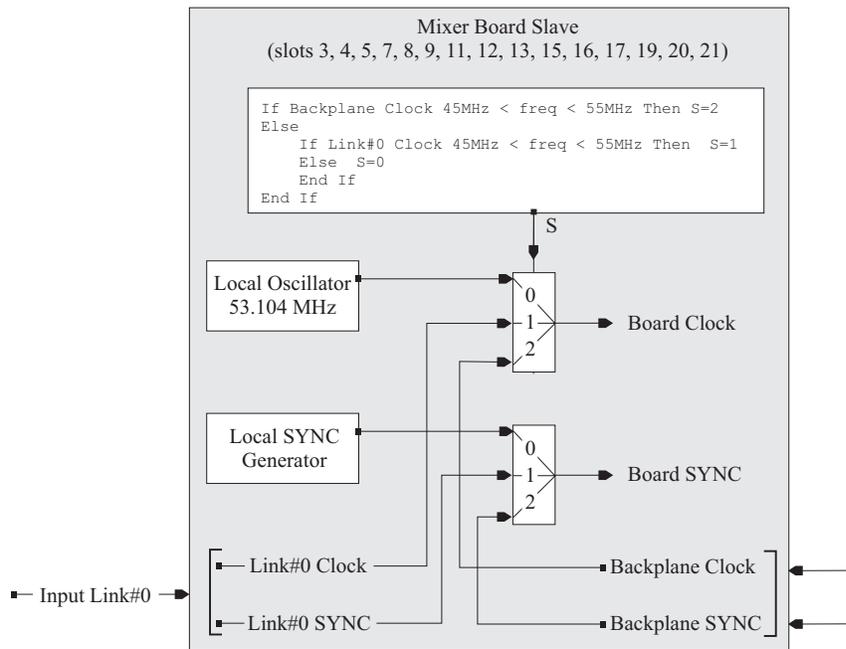


Figure 8.8, Mixer Slave clock selection

In an ideal situation, each mixer subsystem (group of four boards handling the data belonging to a supersector) will use the same clock/SYNC pair after the input links data synchronization. In order to do this, one of the input links clocks is used as global clock. The link used as clock reference is link#0 of the leftmost board (master) of each mixer subsystem. The master board propagates clock and SYNC to the other three boards (slaves) in the subsystem. The clock controller on a slave board has the choice of three clocks: the backplane clock, the link#0 clock or the local oscillator clock. The

clock controller on a master board has only the last two options. The "global sync" is always chosen from the same source of the global clock.

When the mixer system is operating correctly the master boards will be using the link#0 clock and the slave boards will use the backplane clock. In the event a master board doesn't receive a link#0 clock it will switch to the local clock (on-board 53MHz oscillator) for the board "global clock" and switch off the clock backplane distribution to the slave boards.

If a slave board doesn't receive a backplane clock it will switch to the link#0 clock as its first option, and to the local clock (on-board 53MHz oscillator) as its second option.

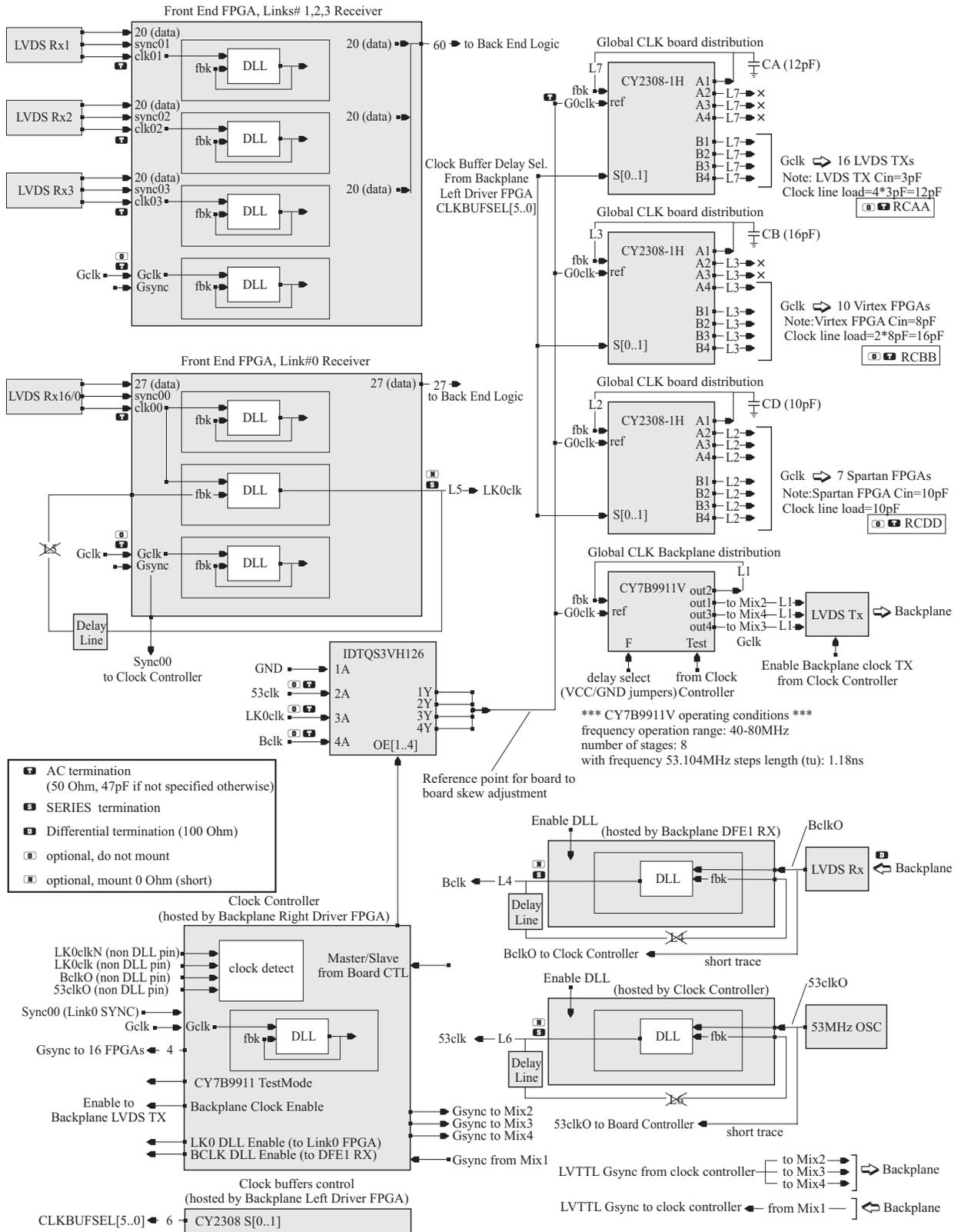


Figure 8.9, Mixer System Clock Distribution

8.8 Mixer System Data Synchronization

A major issue in the mixer system is synchronizing the input data. Two type of synchronization processes are actually needed:

- a) Clock synchronization. It consists of correctly transferring the input data from the input link clock domain to the subsystem clock domain (GCLK).
- b) Frame synchronization. It consists of aligning the input data frames to the subsystem frame reference marker (GSYNC).

The mixer firmware doesn't perform any automatic operation to synchronize input data; it provides instead a means to detect synchronization errors and to correct them.

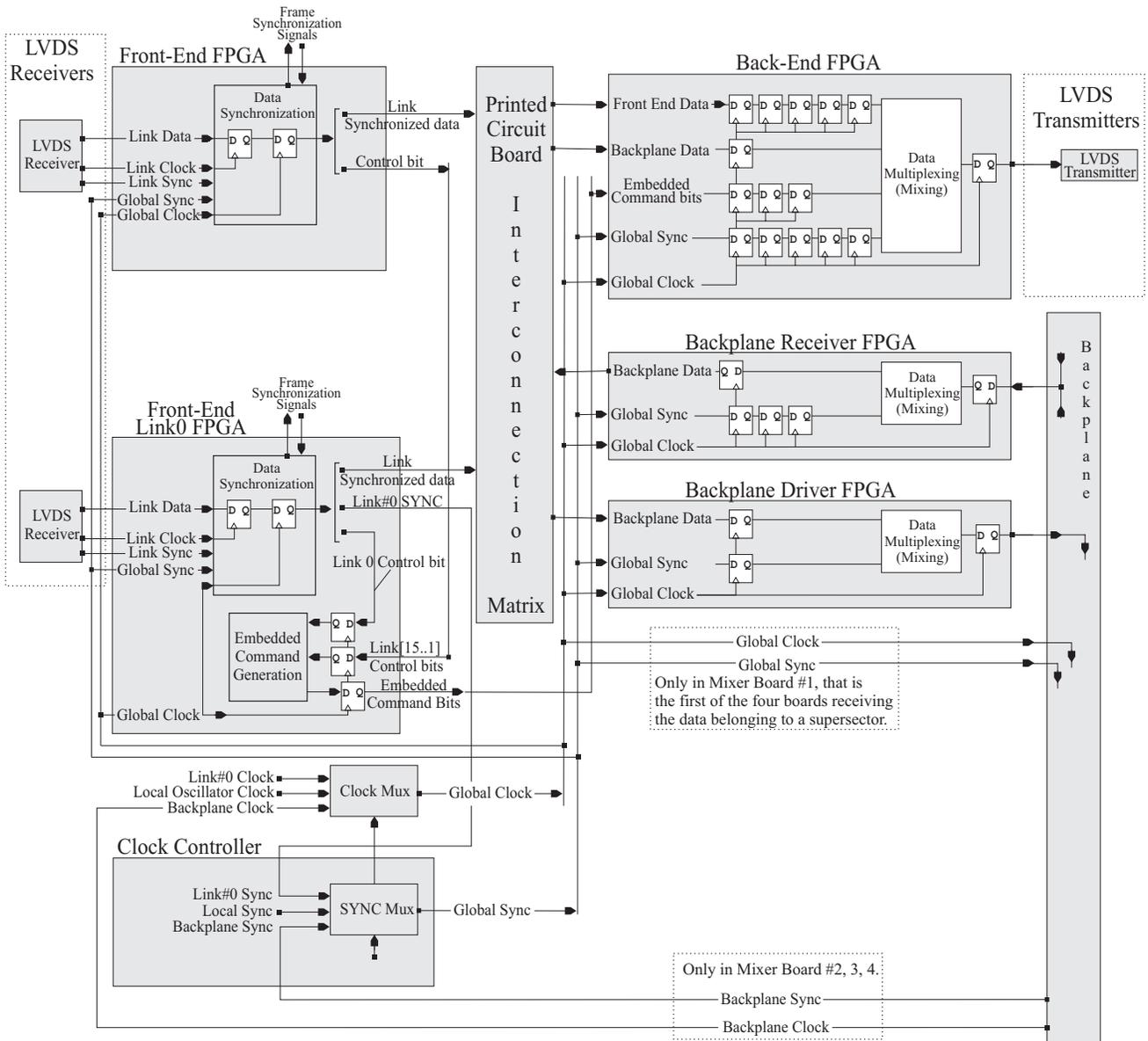
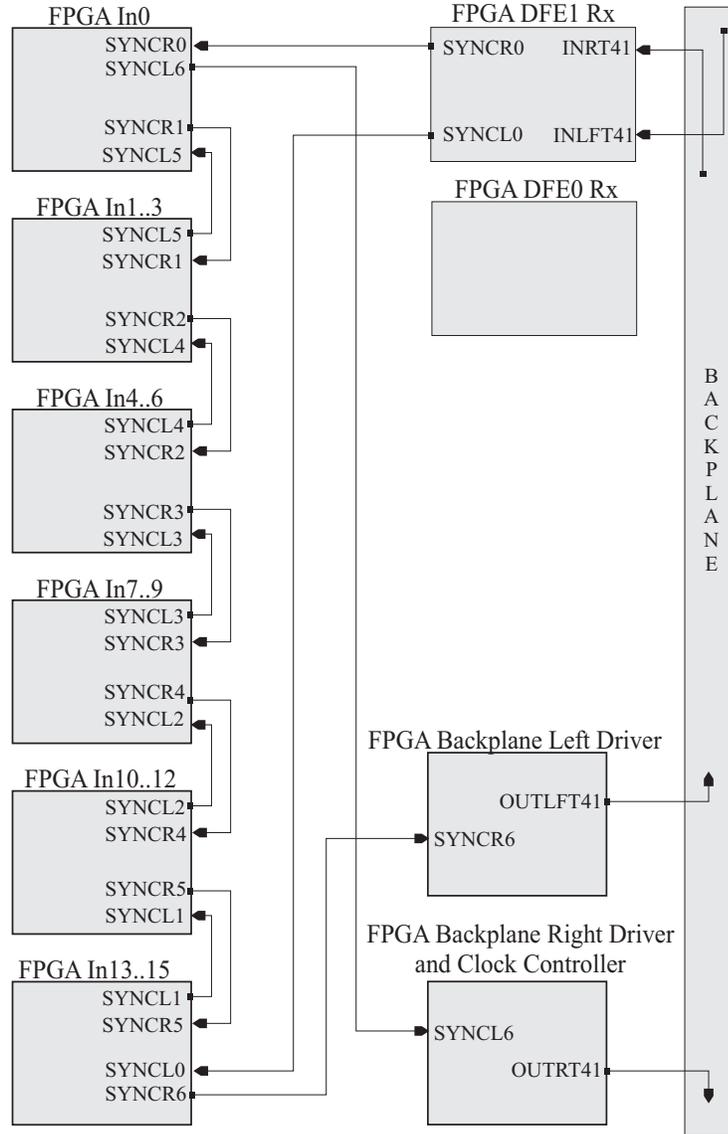


Figure 8.10, Mixer System Data Synchronization

8.9 Mixer Board Frame Synchronization

Frame synchronization signals are part of the mixer design in order to allow for automatic input links frame alignment in a mixer subsystem. This feature is not currently implemented in firmware.



On Mixer Board #1 SYNCL0 is grounded internally on the FPGA DFE1RX
 On Mixer Board #4 SYNCR0 is grounded internally on the FPGA DFE1RX

Figure 8.11, Mixer Board Frame Synchronization signals

8.10 Mixer Board spare connections

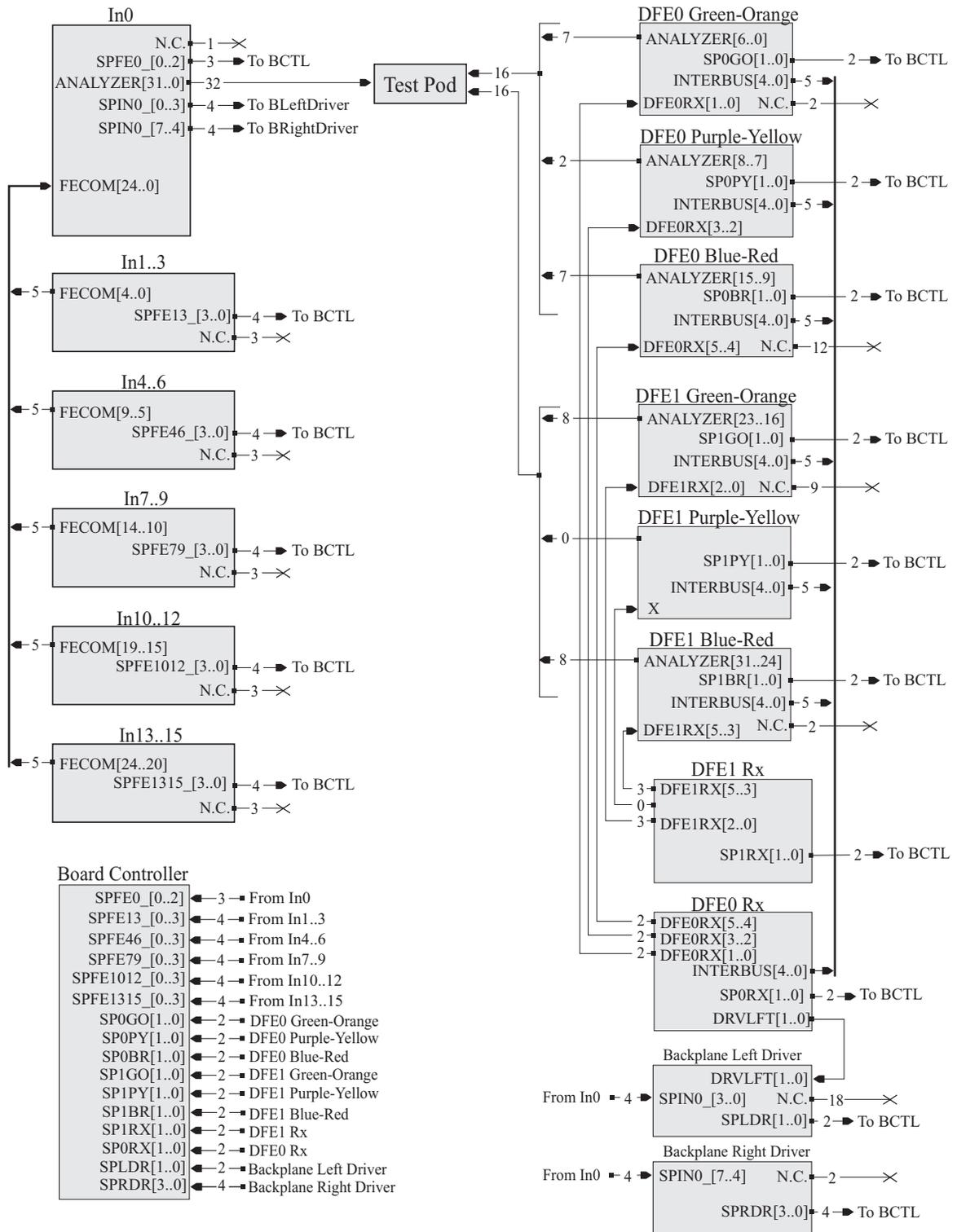


Figure 8.12, Mixer Board spare connections

The mixer design has some spare connections to allow for fixes and new features. Figure 8.12 shows all the available spare signals. Table 8.1 lists the spare connections currently used.

FPGA	Signal name	Connected to	Use
Board Controller	SPRDR[3]	Backplane Right Driver	Connected with a wire to the output enable of a local bus driver (U27pin19).
Backplane DFE1 RX	SP1RX[1]	Board Controller	Signal "Backplane DLL Locked" from Backplane DFE1 RX to Backplane Right Driver.
Board Controller	SPRDR[2]	Backplane DFE1 RX	
IN0	SPIN0_[7]	Backplane Right Driver	Signal "Link#0 DLL Locked" from FE IN0 FPGA to Backplane Right Driver.
Backplane Right Driver	SPIN0_[6]	IN0	Signal "Global Clock FAIL" from clock controller to Front-End FPGAs
IN0	FECOM[0]	IN1..3	
IN0	FECOM[5]	IN4..6	
IN0	FECOM[10]	IN7..9	
IN0	FECOM[15]	IN10..12	
IN0	FECOM[20]	IN13..15	
Backplane Right Driver	SPRDR[1]	Board Controller	Signal "Global Clock FAIL" from clock controller to Board Controller and then to Backplane FPGAs.
Board Controller	SP1RX[0]	Backplane DFE1 RX	
Board Controller	SP0RX[1]	Backplane DFE0 RX	
Board Controller	SPLDR[1]	Backplane Left Driver	
Board Controller	SPFE0_[2..0]	IN0	Signal "FE_SRST_DECODE" from Board Controller to Front-End FPGAs.
IN0	FECOM[3..1]	IN1..3	
IN0	FECOM[8..6]	IN4..6	
IN0	FECOM[13..11]	IN7..9	
IN0	FECOM[18..16]	IN10..12	
IN0	FECOM[23..21]	IN13..15	
Board Controller	SP0GO[1..0]	DFE0 Green-Orange	Enable output links test pattern transmission. SP0GO[0]: DFE0 Green (2 links) SP0GO[1]: DFE0 Orange
Board Controller	SP0PY[1..0]	DFE0 Purple-Yellow	SP0PY[0]: DFE0 Purple SP0PY[1]: DFE0 Yellow
Board Controller	SP0BR[1..0]	DFE0 Blue-Red	SP0BR[0]: DFE0 Blue SP0BR[1]: DFE0 Red (2 links)
Board Controller	SP1GO[1..0]	DFE1 Green-Orange	SP1GO[0]: DFE1 Green (2 links) SP1GO[1]: DFE1 Orange
Board Controller	SP1PY[1..0]	DFE1 Purple-Yellow	SP1PY[0]: DFE1 Purple SP1PY[1]: DFE1 Yellow

9. Appendix C - Mixer Board Printed Circuit Board Interconnection Matrix

The interconnection matrix consists of all the printed circuit board traces used to carry data between the front-end, back-end and backplane FPGAs. The following tables show the data interconnections for each of the mixer input links and for the two backplane receivers FPGAs.

The mixer board design is required to fit four different versions of firmware, one for each of the four boards handling the data of a supersector. Because of this requirement there are some connections that are not used in each of the four firmware versions. A table cell has a grey background when the corresponding data bit has a connection to a Back-End or Backplane FPGA. A "greyed" table cell will also contain at least one of four possible numbered icons (1 2 3 4) which are used to indicate the firmware version using the connection.

Link#0	DFE0			DFE1			Backplane driver	
	Green Orange	Yellow Purple	Red Blue	Green Orange	Yellow Purple	Red Blue	Left	Right
1	1 2 3 4							
2	1 2 3 4							
3		1 2 3 4						
4		1 2 3 4						
5		1 2 3 4						
6			1 2 3 4					
7			1 2 3 4					
8				1 2 3 4				
9				1 2 3 4				
10					1 2 3 4			
11					1 2 3 4			
12					1 2 3 4			
13						1 2 3 4		
14						1 2 3 4		
15	1 2 3 4							
16	1 2 3 4							
17		1 2 3 4						
18		1 2 3 4						
19		1 2 3 4						
20			1 2 3 4					
21			1 2 3 4					
22				1 2 3 4				
23				1 2 3 4				
24					1 2 3 4			
25					1 2 3 4			
26					1 2 3 4	1 2 3 4		
27						1 2 3 4		

Figure 9.1, Link #0 (CPS) Interconnection Matrix.

Link#1	DFE0			DFE1			Backplane driver	
	Green Orange	Yellow Purple	Red Blue	Green Orange	Yellow Purple	Red Blue	Left	Right
1	1 2 3 4							
2	1 2 3 4							
3	1 2 3 4							
4	1 2 3 4							
5	1 2 3 4							
6	1 2 3 4							
7	2	1 3 4						
8	2	1 3 4						
9		1 2 3 4						
10		1 2 3 4						
11			1 2 3 4					
12			1 2 3 4					
13			1 2 3 4		1 3			
14			2	4	1 3			
15			2	1 3 4				
16				1 2 3 4				
17				1 2 3 4				
18				1 2 3 4				
19				1 2 3 4				
20				1 2 3 4				

Figure 9.2, Link #1 Interconnection Matrix

Link#2	DFE0			DFE1			Backplane driver	
	Green Orange	Yellow Purple	Red Blue	Green Orange	Yellow Purple	Red Blue	Left	Right
1	1 2 3 4							
2	1 2 3 4							
3	1 2 3 4							
4	1 2 3 4							
5		1 2 3 4						
6		1 2 3 4						
7		1 2 3 4						
8		1 2 3 4						
9		1 2 3 4						
10		1 2 3 4						
11				1 2 3 4				
12				1 2 3 4				
13				1 2 3 4				
14				1 2 3 4				
15					1 2 3 4			
16					1 2 3 4			
17					1 2 3 4			
18					1 2 3 4			
19					1 2 3 4			
20					1 2 3 4			

Figure 9.3, Link #2 Interconnection Matrix

Link#3	DFE0			DFE1			Backplane driver	
	Green Orange	Yellow Purple	Red Blue	Green Orange	Yellow Purple	Red Blue	Left	Right
1		1 2 3 4						
2		1 2 3 4						
3		1 2 3 4						
4		1 2 3 4						
5		1 2 3 4						
6		1 2 3 4						
7			1 2 3 4					
8			1 2 3 4					
9			1 2 3 4					
10			1 2 3 4					
11					1 2 3 4			
12					1 2 3 4			
13					1 2 3 4			
14					1 2 3 4			
15					1 2 3 4			
16					1 2 3 4			
17						1 2 3 4		
18						1 2 3 4		
19						1 2 3 4		
20						1 2 3 4		

Figure 9.4, Link #3 Interconnection Matrix

Link#4	DFE0			DFE1			Backplane driver	
	Green Orange	Yellow Purple	Red Blue	Green Orange	Yellow Purple	Red Blue	Left	Right
1	1 2 4	4						
2	1 4	1 2 3 4						
3		1 2 3 4						
4		1 2 3 4						
5		1 2 3 4						
6		1 2 3 4						
7		2 4	1 3 4					
8		2	1 3 4					
9		2	1 3 4					
10		2	1 3 4					
11				1 2 3 4				
12				1 2 3 4				
13				1 2 3 4				
14				1 2 3	2 4			
15				1 3	2 4			
16				1 3	2 4			
17				1 3	2 4			
18				1 3	2 4			
19					1 2 3 4			
20					1 2 3 4			

Figure 9.5, Link #4 Interconnection Matrix

Link#5	DFE0			DFE1			Backplane driver	
	Green Orange	Yellow Purple	Red Blue	Green Orange	Yellow Purple	Red Blue	Left	Right
1	4	1 2	3					
2	4	1 2	3					
3	4	1 2	3					
4	4	1 2	3					
5	4	1 2	3					
6		1 2 4	3					
7		2 4	1 3					
8		2 4	1	3				
9		4	1 2	3				
10		4	1 2	3				
11					1 2 3 4			
12					1 2 3 4			
13					1 2 3 4			
14					1 2 3 4			
15					1 2 4	3		
16					1	2 3 4		
17					1	2 3 4		
18					1	2 3 4		
19					1	2 3 4		
20						2 3 4		

Figure 9.6, Link #5 Interconnection Matrix

Link#6	DFE0			DFE1			Backplane driver	
	Green Orange	Yellow Purple	Red Blue	Green Orange	Yellow Purple	Red Blue	Left	Right
1		1	2 3 4					
2		1	2 3 4					
3		1	2 3 4					
4		1	3 4	2				
5		1	3 4	2				
6		1		2 3 4				
7		1		2 3 4				
8			1	2 3 4				
9			1	2 3 4				
10			1	2 3 4				
11				1	3 4	2		
12				1	3 4	2		
13				1		2 3 4		
14					1	2 3 4		
15					1	2 3 4		
16					1	2 3 4		
17					1	2 3 4		
18					1	2 3 4		
19					1	2 3 4		
20					1	2 3 4		

Figure 9.7, Link #6 Interconnection Matrix

Link#7	DFE0			DFE1			Backplane driver	
	Green Orange	Yellow Purple	Red Blue	Green Orange	Yellow Purple	Red Blue	Left	Right
1	2 4					1 3		
2	2 4					1 3		
3	2 4					1 3		
4	2 4					1 3		
5	2 4					1 3		
6							2 4	1 3
7							2 4	1 3
8							2 4	1 3
9							2 4	1 3
10							2 4	1 3
11	1 3	2 4						
12	1 3	2 4						
13	1 3		2 4					
14	1 3		2 4					
15	1 3	1 3	2 4					
16		1 3	2 4					
17		1 3	2 4					
18			1 2 3 4					
19			1 2 3 4					
20			1 2 3 4					

Figure 9.8, Link #7 Interconnection Matrix

Link#8	DFE0			DFE1			Backplane driver	
	Green Orange	Yellow Purple	Red Blue	Green Orange	Yellow Purple	Red Blue	Left	Right
1	2 4				1 3	1 3		
2	2 4					1 3		
3	2 4					1 3		
4	2 4					1 3		
5	2 4					1 3		
6							2 4	1 3
7							2 4	1 3
8							2 4	1 3
9							2 4	1 3
10							2 4	1 3
11		1 2 3 4						
12		1 2 3 4	2 4					
13		1 3	1 2 3 4					
14			1 2 3 4					
15			1 2 3 4					
16			1 2 3 4					
17			1 2 3 4					
18				1 2 3 4				
19				1 2 3 4				
20				1 2 3 4				

Figure 9.9, Link #8 Interconnection Matrix

Link#9	DFE0			DFE1			Backplane driver	
	Green Orange	Yellow Purple	Red Blue	Green Orange	Yellow Purple	Red Blue	Left	Right
1			1	4			2 3	
2			1	4			2 3	
3			1	4			2 3	
4			1	4	4		2 3	
5			1		4		2 3	
6			1		4		2 3	
7			1		4		2 3	
8				1	4		2 3	
9				1		4	2 3	
10				1		4	2 3	
11	1	2 3 4						
12	1	2 3 4						
13	1	2 3 4	4					
14	1	2 3	4					
15	1	2 3	4					
16	1	2 3	4					
17	1	2	3 4					
18	1		2 3	4				
19	1		2 3	4				
20	1		2 3	4				

Figure 9.10, Link #9 Interconnection Matrix

Link#10	DFE0			DFE1			Backplane driver	
	Green Orange	Yellow Purple	Red Blue	Green Orange	Yellow Purple	Red Blue	Left	Right
1	1				4			2 3
2	1				4			2 3
3	1				4			2 3
4	1				4			2 3
5	1					4		2 3
6		1				4		2 3
7		1				4		2 3
8		1				4		2 3
9		1				4		2 3
10		1				4		2 3
11				1 2 3	4			
12				1 2 3	4			
13				2 3	1 4			
14					1 2 3 4			
15					1 2 3 4			
16					1 2 3	4		
17					1 2 3	4		
18					1 2 3	4		
19					1 2 3	4		
20					1 2 3	4		

Figure 9.11, Link #10 Interconnection Matrix

Link#11	DFE0			DFE1			Backplane driver	
	Green Orange	Yellow Purple	Red Blue	Green Orange	Yellow Purple	Red Blue	Left	Right
1	1			4				2 3
2	1			4				2 3
3	1			4	4			2 3
4	1				4			2 3
5	1				4			2 3
6		1				4		2 3
7		1				4		2 3
8		1				4		2 3
9		1				4		2 3
10		1				4		2 3
11				3	1 2	4		
12				3	1 2	4		
13					1 3	2 4		
14					1 3	2 4		
15					1 3	2 4		
16					3	1 2 4		
17					3	1 2 4		
18					3	1 2 4		
19					3	1 2 4		
20					3	1 2 4		

Figure 9.12, Link #11 Interconnection Matrix

Link#12	DFE0			DFE1			Backplane driver	
	Green Orange	Yellow Purple	Red Blue	Green Orange	Yellow Purple	Red Blue	Left	Right
1	1			4			3	2
2	1			4			3	2
3	1			4			3	2
4	1			4			3	2
5	1				4		3	2
6	1				4		3	2
7	1				4		3	2
8	1				4		3	2
9		1			4		3	2
10		1			4		3	2
11			1 2 3 4					
12			1 2 3 4					
13			1 2 3 4					
14			1	2 3 4				
15			1	2 3 4				
16				1 2 3 4				
17				1 2 3 4				
18				1 2 3 4	2 3 4			
19				1	2 3 4			
20				1	2 3 4			

Figure 9.13, Link #12 Interconnection Matrix

Link#13	DFE0			DFE1			Backplane driver	
	Green Orange	Yellow Purple	Red Blue	Green Orange	Yellow Purple	Red Blue	Left	Right
1							4	1 2 3
2							4	1 2 3
3							4	1 2 3
4							4	1 2 3
5							4	1 2 3
6							4	1 2 3
7							4	1 2 3
8							4	1 2 3
9							4	1 2 3
10							4	1 2 3
11				1 2 4	3			
12				1 2 4	3			
13				1 2 4	3			
14				1 2 4	2 3			
15					1 2 3 4			
16					1 2 3 4			
17					2 3	1 4		
18					2 3	1 4		
19					3	1 2 4		
20						1 2 3 4		

Figure 9.14, Link #13 Interconnection Matrix

Link#14	DFE0			DFE1			Backplane driver	
	Green Orange	Yellow Purple	Red Blue	Green Orange	Yellow Purple	Red Blue	Left	Right
1							2 3 4	1
2							2 3 4	1
3							2 3 4	1
4							2 3 4	1
5							2 3 4	1
6							2 3 4	1
7							2 3 4	1
8							2 3 4	1
9							2 3 4	1
10							2 3 4	1
11			1 2 3 4					
12			1 2 3 4					
13			1 2 3 4					
14			1 2 3 4					
15			1 2 3 4					
16		2		1 3 4				
17		2		1 3 4				
18		2		1 2 3 4				
19				1 2 3 4				
20				1 2 3 4				

Figure 9.15, Link #14 Interconnection Matrix

Link#15	DFE0			DFE1			Backplane driver	
	Green Orange	Yellow Purple	Red Blue	Green Orange	Yellow Purple	Red Blue	Left	Right
1							2 3 4	1
2							2 3 4	1
3							2 3 4	1
4							2 3 4	1
5							2 3 4	1
6							2 3 4	1
7							2 3 4	1
8							2 3 4	1
9							2 3 4	1
10							2 3 4	1
11	1 2 3 4							
12	1 2 3 4							
13	1 2 3 4							
14	1 2 3 4							
15	2 3	1 4						
16	2	1 3 4						
17		2 3	1 4					
18		2 3	1 4					
19		2 3	1 4					
20		2 3	1 4					

Figure 9.16, Link #15 Interconnection Matrix

0GRN_ORG Bit#	DFE0 Green Orange	0YEL_PUR Bit#	DFE0 Yellow Purple	0RED_BLU Bit#	DFE0 Red Blue
1	2 3 4	1	2 3 4	1	1 2 3 4
2	2 3 4	2	2 3 4	2	1 2 3 4
3	2 3 4	3	2 3 4	3	1 2 3 4
4	2 3 4	4	2 3 4	4	2 3
5	2 3 4	5	2 3 4	5	2 3
6	2 3 4	6	2 3 4	6	2 3
7	2 3 4	7	2 3 4	7	2 3
8	2 3 4	8	3 4	8	2 3
9	2 3 4	9	3 4	9	2 3
10	2 3 4	10	3 4	10	3
11	2 3 4	11	3 4		
12	2 3 4	12	3 4		
13	2 3 4	13	3 4		
14	2 3 4	14	3 4		
15	2 3 4	15	3 4		
16	2 3 4	16	3 4		
17	2 3 4	17	3 4		
18	2 3 4	18	4		
19	2 3 4	19	4		
20	3	20			
21	3	21			
22	3	22			
23	3				
24	3				
25	3				
26	3				

Figure 9.17, Backplane DFE0 Receiver Interconnection Matrix.

1GRN_ORG Bit#	DFE1 Green Orange	1YEL_PUR Bit#	DFE1 Yellow Purple	1RED_BLU Bit#	DFE1 Red Blue
1	1 2 3	1	1 2 3	1	1 2 3
2	1 2 3	2	1 2 3	2	1 2 3
3	1 2 3	3	1 2 3	3	1 2 3
4	1 2 3	4	1 2 3	4	1 2 3
5	1 2	5	1 2 3	5	1 2 3
6	2	6	1 2 3	6	1 2 3
7	2	7	1 2 3	7	1 2 3
8	2	8	1 2	8	1 2 3
9	2	9	2	9	1 2 3
10	2	10	2	10	1 2 3
11	2	11	2	11	1 2 3
12	2	12	2	12	1 2 3
		13	2	13	1 2 3
		14	2	14	1 2 3
		15		15	1 2 3
				16	1 2 3
				17	1 2 3
				18	1 2 3
				19	1 2 3
				20	1 2
				21	1 2
				22	1
				23	1
				24	
				25	
				26	
				27	
				28	
				29	
				30	

Figure 9.18, Backplane DFE1 Receiver Interconnection Matrix.

10. Appendix D - Mixer System Backplane connectors pinout

Pin #	Row 'z' (bottom shield)	Row 'a'	Row 'b'	Row 'c'	Row 'd'	Row 'e'	Row 'f' (top shield)
1	GND	INLFT2	GND	INLFT1	GND	OUTRT1	
2		GND	INLFT3	GND	OUTRT2	GND	GND
3	GND	INLFT4	GND	OUTRT3	GND	OUTRT4	
4		GND	INLFT5	GND	OUTRT5	GND	GND
5	GND	INLFT7	GND	INLFT6	GND	OUTRT6	
6		GND	INLFT8	GND	OUTRT7	GND	GND
7	GND	INLFT9	GND	OUTRT8	GND	OUTRT9	
8		GND	INLFT10	GND	OUTRT10	GND	GND
9	GND	INLFT12	GND	INLFT11	GND	OUTRT11	
10		GND	INLFT13	GND	OUTRT12	GND	GND
11	GND	INLFT14	GND	OUTRT13	GND	OUTRT14	
	polarizing and guiding peg						
12	GND	GND	INLFT15	GND	OUTRT15	GND	
13		INLFT17	GND	INLFT16	GND	OUTRT16	GND
14	GND	GND	INLFT18	GND	OUTRT17	GND	
15		INLFT19	GND	OUTRT18	GND	OUTRT19	GND
16	GND	GND	INLFT20	GND	OUTRT20	GND	
17		INLFT22	GND	INLFT21	GND	OUTRT21	GND
18	GND	GND	INLFT23	GND	OUTRT22	GND	
19		INLFT24	GND	OUTRT23	GND	OUTRT24	GND
20	GND	GND	INLFT25	GND	OUTRT25	GND	
21		INLFT27	GND	INLFT26	GND	OUTRT26	GND
22	GND	GND	INLFT28	GND	OUTRT27	GND	
1		INLFT29	GND	OUTRT28	GND	OUTRT29	GND
2	GND	GND	INLFT30	GND	OUTRT30	GND	
3		INLFT32	GND	INLFT31	GND	OUTRT31	GND
4	GND	GND	INLFT33	GND	OUTRT32	GND	
5		INLFT34	GND	OUTRT33	GND	OUTRT34	GND
6	GND	GND	INLFT35	GND	OUTRT35	GND	
7		INLFT37	GND	INLFT36	GND	OUTRT36	GND
8	GND	GND	INLFT38	GND	OUTRT37	GND	
9		INLFT39	GND	OUTRT38	GND	OUTRT39	GND
10	GND	GND	INLFT40	GND	OUTRT40	GND	
11		GND	GND	INLFT41	GND	OUTRT41	GND
12	GND	MOD_ID4	MOD_ID3	MOD_ID2	MOD_ID1	MOD_ID0	
13		+IN_CLK	GND	+OUT_CLK0	+OUT_CLK1	+OUT_CLK2	GND
14	GND	-IN_CLK	GND	-OUT_CLK0	-OUT_CLK1	-OUT_CLK2	
15		GND	GND	GND	GND	GND	GND
16	GND	STAT_CLK	GND	STAT_RST	GND	STAT	
17		Power 3.3V	GND				
18	GND	Power 3.3V					
19		Power 3.3V	GND				

Table 10.1, Pin/Signal assignments for the backplane top section connector

Pin #	Row 'z' (bottom shield)	Row 'a'	Row 'b'	Row 'c'	Row 'd'	Row 'e'	Row 'f' (top shield)
1	GND	VADDR7	VWRITE	VDAT6	VDAT5	VDAT2	
2		VADDR15	*SYSRST	VDAT7	VDAT0	VDAT3	GND
3	GND	VADDR12	VAS	VSYSCLK	VDAT1	VDAT4	
4		VADDR9	*VDTACK	*VBERR	VADDR13	VADDR5	GND
5	GND	VADDR11	VADDR2	VADDR10	VADDR0	VADDR3	
6		VADDR8	VADDR6	VADDR1	VADDR14	VADDR4	GND
7	GND	Power 3.3V					
8		Power 3.3V	GND				
9	GND	OUTLFT2	GND	OUTLFT1	GND	INRT1	
10		GND	OUTLFT3	GND	INRT2	GND	GND
11	GND	OUTLFT4	GND	INRT3	GND	INRT4	
	polarizing and guiding peg						
12	GND	GND	OUTLFT5	GND	INRT5	GND	
13		OUTLFT7	GND	OUTLFT6	GND	INRT6	GND
14	GND	GND	OUTLFT8	GND	INRT7	GND	
15		OUTLFT9	GND	INRT8	GND	INRT9	GND
16	GND	GND	OUTLFT10	GND	INRT10	GND	
17		OUTLFT12	GND	OUTLFT11	GND	INRT11	GND
18	GND	GND	OUTLFT13	GND	INRT12	GND	
19		OUTLFT14	GND	INRT13	GND	INRT14	GND
20	GND	GND	OUTLFT15	GND	INRT15	GND	
21		OUTLFT17	GND	OUTLFT16	GND	INRT16	GND
22	GND	GND	OUTLFT18	GND	INRT17	GND	
1		OUTLFT19	GND	INRT18	GND	INRT19	GND
2	GND	GND	OUTLFT20	GND	INRT20	GND	
3		OUTLFT22	GND	OUTLFT21	GND	INRT21	GND
4	GND	GND	OUTLFT23	GND	INRT22	GND	
5		OUTLFT24	GND	INRT23	GND	INRT24	GND
6	GND	GND	OUTLFT25	GND	INRT25	GND	
7		OUTLFT27	GND	OUTLFT26	GND	INRT26	GND
8	GND	GND	OUTLFT28	GND	INRT27	GND	
9		OUTLFT29	GND	INRT28	GND	INRT29	GND
10	GND	GND	OUTLFT30	GND	INRT30	GND	
11		OUTLFT32	GND	OUTLFT31	GND	INRT31	GND
12	GND	GND	OUTLFT33	GND	INRT32	GND	
13		OUTLFT34	GND	INRT33	GND	INRT34	GND
14	GND	GND	OUTLFT35	GND	INRT35	GND	
15		OUTLFT37	GND	OUTLFT36	GND	INRT36	GND
16	GND	GND	OUTLFT38	GND	INRT37	GND	
17		OUTLFT39	GND	INRT38	GND	INRT39	GND
18	GND	GND	OUTLFT40	GND	INRT40	GND	
19		GND	GND	OUTLFT41	GND	INRT41	GND

Table 10.2, Pin/Signal assignments for the backplane bottom section connector.

11. Appendix E - Test Patterns specification

11.1 Input links test patterns

The Mixer Board logic allows for recognition of two test patterns, a walking one (shown in Table 11.1) and a walking zero (the complementary pattern of the walking one with the exclusion of the SYNC bit). The pattern detection can be verified by setting the LEDs to monitoring mode #2 (walking 1) and mode #3 (walking 0). The pattern recognition feature is used to test input links integrity and to verifying the correctness of cabling.

The word at time slot #42 is used by the test pattern detection logic to synchronize itself with the test pattern received on the input link. No synchronization check is performed between the test patterns received on different links.

Time Slot	Bit number (Top Half Link)										Bit number (Bottom Half Link)										Sync bit
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
2	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
3	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
4	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
5	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
6	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
7	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1
8	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0
10	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0
11	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
12	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
13	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
14	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1
15	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
16	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0
18	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0
19	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0
20	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0
21	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
22	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
23	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
24	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
25	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
26	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
27	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0
28	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1
29	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0
30	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0
31	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
32	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
33	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
34	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
35	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1
36	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
37	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0
38	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0

39	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	
40	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0
41	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
42	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1
43	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
44	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
45	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
46	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
47	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
48	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0
49	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1
50	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0
51	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
52	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
53	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
54	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
55	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
56	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1
57	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0
58	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0
59	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0
60	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0
61	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
62	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
63	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
64	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
65	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
66	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
67	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
68	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0
69	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0
70	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1

Table 11.1, Input Links walking 1 test pattern.

11.2 Output links test patterns

The mixer board output links can send a test pattern instead of data. The test pattern is the same for every output link except for a link-identification word (Table 11.3), which is unique between all the links in a mixer subsystem. The DFE board logic is able to recognize the test pattern generated by the mixer. This feature allows verifying both link integrity and correctness of cabling.

The test pattern transmission can be enabled through the Output Links Test Mode registers (see Paragraph 4.5.13 page 41).

Time	Bit number																											
Slot	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
26	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
27	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
28	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
29	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Relative Sector		Link Color			

Table 11.2, Output Links test patterns.

Link Color			Link color identifier	Relative Sector				Relative Sector # within a supersector	Mixer Board #	Mixer Board link color and link#
0	0	0	red	0	0	0	0	1	1	green[00, 01], orange[02], purple[03]
0	0	1	green	0	0	0	1	2	1	yellow[04], blue[05], red[06]
0	1	0	blue	0	0	1	0	3	1	green[10, 11], orange[12], purple[13]
0	1	1	yellow	0	0	1	1	4	1	yellow[14], blue[15], red[16]
1	0	0	purple	0	1	0	0	5	2	green[00, 01], orange[02], purple[03]
1	0	1	orange	0	1	0	1	6	2	yellow[04], blue[05], red[06]
				0	1	1	0	7	2	green[10, 11], orange[12], purple[13]
				0	1	1	1	8	2	yellow[14], blue[15], red[16]
				1	0	0	0	9	3	green[00, 01], orange[02], purple[03]
				1	0	0	1	10	3	yellow[04], blue[05], red[06]
				1	0	1	0	11	3	green[10, 11], orange[12], purple[13]
				1	0	1	1	12	3	yellow[14], blue[15], red[16]
				1	1	0	0	13	4	green[00, 01], orange[02], purple[03]
				1	1	0	1	14	4	yellow[04], blue[05], red[06]
				1	1	1	0	15	4	green[10, 11], orange[12], purple[13]
				1	1	1	1	16	4	yellow[14], blue[15], red[16]

Table 11.3, Link relative sector and color encoding in the output links test pattern.

12. Appendix F – Mixer Board Components and Layout

Table 12.1 list the components used on the mixer board with the exclusions of resistors, capacitors, inductors and minor stock components. A complete list of all components is available in a separate document [Ref. 8]. Figure 12.1 is a drawing of the mixer board showing components location.

Component	Schematic and Layout identifier/s	Description
AMP 2510-6003UB	CON1, CON3.	10 pin JTAG header. [Ref. 13]
AMP 1-106014-1	J1, J2, J4, J6.	125 pin front panel header. [Ref. 13]
AMP 2-7674004-2	J3, J5, J7.	Surface mount header for HP Logic Analyzer. [Ref. 13]
Brookdale Electronics B500CTE3G	X1	Thru hole Half-DIP 53.104 MHZ oscillator. Used as board's local clock source. [Ref. 14]
Cypress CY7B9911V-5JC	U9.	PLCC32 3.3V RoboClock Low Voltage programmable Skew Clock Buffer. Used as clock source for the backplane clock transmitter (U15). [Ref. 18]
Cypress CY2308ZC-1H	U8, U13, U16.	16 pin TSSOP 3.3V Zero Delay Buffer. Used for on-board clock distribution. [Ref. 18]
C&K EP11S2D1ABE	S1	Front panel reset push-button. [Ref. 19]
Elmec Delay Line	U71, U72.	3 pin delay line. Not installed. [Ref. 20]
Fairchild 74LCX16244MEAX	U28, U36.	48 pin SSOP Low Voltage 16-Bit Buffer/Line Driver. [Ref. 22]
Fairchild 74LCX38MX	U30.	14 pin SOIC Low Voltage Quad 2-Input NAND Gate (open drain). [Ref. 22]
Harting 1721-110-2102	P1, P3.	110 pin keyed backplane connectors. [Ref. 24]
Harting 1725-095-2102	P2, P4.	95 pin backplane connectors. [Ref. 24]
IDT QS3VH126S1	U14.	14 pin SOIC Quickswitch® 3.3V QUAD Active High Analog Switch. Is used as clock multiplexer. [Ref. 27]
IDT QS53805AQ	U4, U7.	20 pin QSSOP Low Skew 3.3V CMOS Clock Driver/Buffer. Used for configuration (CCLK) and JTAG (TCK) clocks distribution. [Ref. 27]
Linear Technology LTC1326CS8-2.5	U20.	8 pin SO (S8) MicropowerPrecision Triple Supply Monitors. Used to monitor the 3.3Volt and 2.5Volt voltages. [Ref. 29]
Littlefuse 251004	F1	4 Ampere fuse. [Ref. 30]
Littlefuse 241012	F2	10 Ampere fuse. [Ref. 30]
Lumex SSL-LX3059IGW	D2, D3, D4, D5, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18.	Front panel bi-color LEDs. [Ref. 31]
Lumex SSL-LX3052DI	D1, D6	Front panel 3.3V and 2.5V LEDs. [Ref. 31]
Motorola MC74LCX245DT	U27, U29, U34.	20 pin TSSOP Low Voltage Bidirectional Transceiver. [Ref. 33]

Micrel MIC39500-2.5BU	U21.	TO263 5A Low-Voltage Low-Dropout Regulator. Used to generate the 2.5 Volt needed by the Virtex FPGAs (core voltage). [Ref. 32]
National Semiconductor DS90LV047ATMTC	U15.	16 pin TSSOP 3V LVDS Quad CMOS Differential Line Driver. Used as backplane clock transmitter on boards operation as masters. [Ref. 34]
National Semiconductor DS90LV018ATM	U17.	8 pin SOP 3V LVDS Single CMOS Differential Line Receiver. Used as backplane clock receiver on boards operating as slaves. [Ref. 34]
Philips 1N5908	D19.	1500W Zener Transient Voltage Suppressor. Used for over-voltage protection on the 3.3Volt power input. [Ref. 36]
Texas Instruments SN65LVDS93DGG	U53, U54, U55, U56, U57, U58, U59, U60, U61, U62, U63, U64, U65, U66, U67, U68.	TSOP LVDS SERDES Transmitter. Used as LVDS transmitter for the output links [Ref. 38] .
Texas Instruments SN65LVDS96DGG	U23, U24, U25, U26, U37, U38, U39, U40, U41, U42, U43, U44, U49, U50, U51.	20 pin TSOP LVDS SERDES Receiver. Used as LVDS receiver for links 1 to 15 (21 bit wide links). [Ref. 38]
Texas Instruments SN65LVDS94DGG	U52.	TSOP LVDS SERDES Receiver. Used as LVDS receiver for link 0 (28 bit wide link). [Ref. 38]
Texas Instruments 74LCX16244T	U3, U69, U70.	48pin TSSOP Low Voltage 16-Bit Buffer/Line Driver. [Ref. 38]
Xilinx XCV50-6 PQ240C	U5, U6, U12, U31, U32, U33, U45, U46, U47, U48.	PQFP240 Virtex™ 2.5Volt FPGA. Used for the Front End and Backplane FPGAs. [Ref. 40]
Xilinx XCS40XL-5 PQ240C	U1, U2, U10, U11, U18, U19, U22.	PQFP240 Spartan FPGA. Used for the Back-End and for the Board Controller FPGAs. [Ref. 40]
Xilinx XC18V01SO20C	U35.	SOIC Configuration EEPROM. Is used for the configuration of the board controller FPGA (U22). [Ref.40]

Table 12.1, Mixer Board component list.

The Mixer printed circuit board has a total of fourteen metal layers seven of which are signal layers. Table 12.2 shows the layers stacking.

PCB Layer	Description	Impedance control
Top	Signal layer	50 (\pm 10%) Ω coated microstrip.
Inner 1	Ground plane layer	n.a.
Inner 2	Signal layer	50 (\pm 10%) Ω symmetrical stripline.
Inner 3	2.5 Volt power plane layer	n.a.
Inner 4	Signal layer	50 (\pm 10%) Ω symmetrical stripline.
Inner 5	Ground plane layer	n.a.
Inner 6	3.3 Volt power plane layer	n.a.
Inner 7	Signal layer	50 (\pm 10%) Ω symmetrical stripline.
Inner 8	Ground plane layer	n.a.
Inner 9	Signal layer	50 (\pm 10%) Ω symmetrical stripline.
Inner 10	3.3 Volt power plane layer	n.a.
Inner 11	Signal layer	50 (\pm 10%) Ω symmetrical stripline.
Inner 12	Ground plane layer	n.a.
Bottom	Signal layer	50 (\pm 10%) Ω coated microstrip.

Table 12.2, Printed Circuit Board stacking.

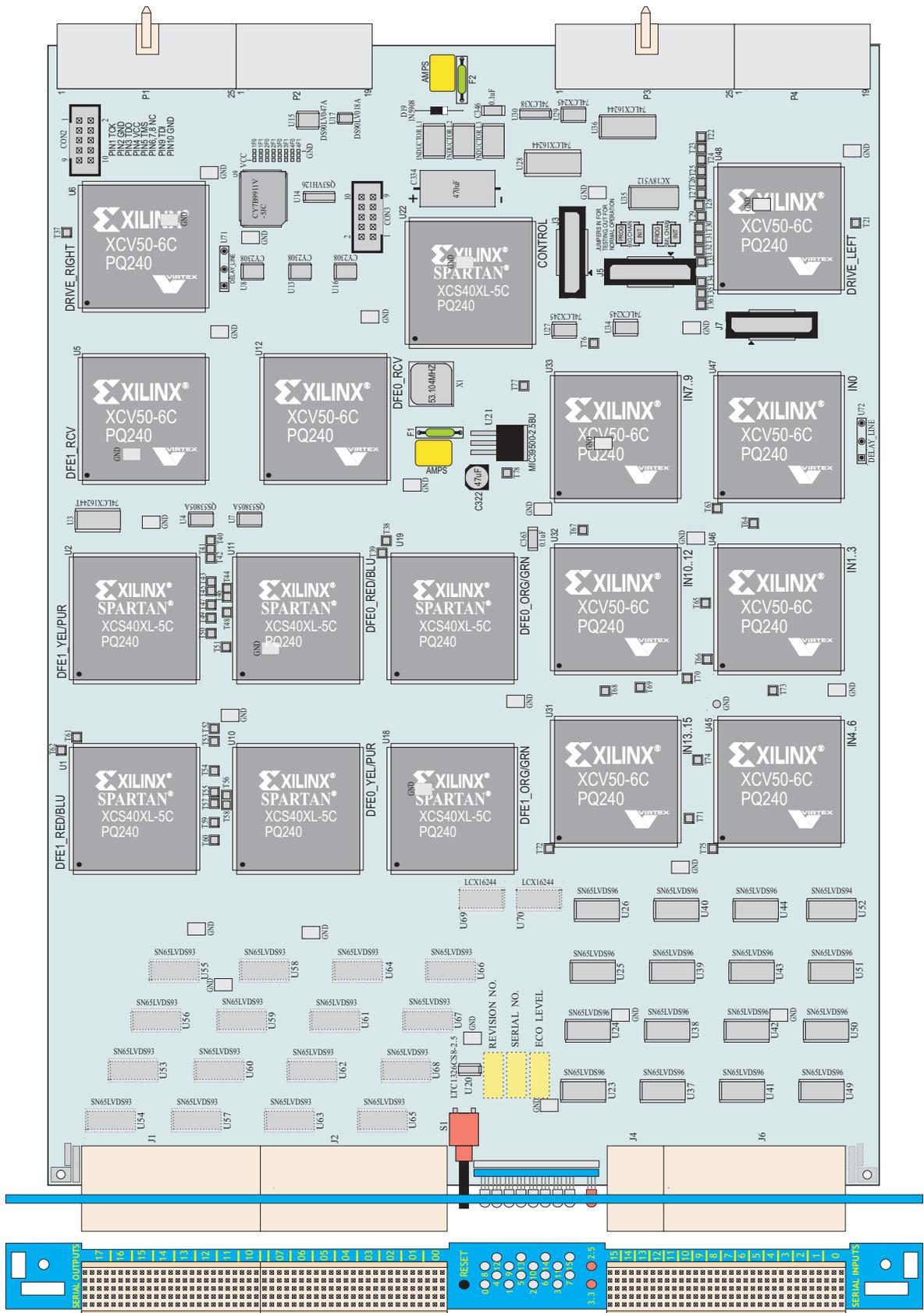


Figure 12.1, Mixer Board.

13. Appendix G – Input and Output Links cabling

13.1 Mixer System Input Links cabling map

Mapping information are derived from several documents Ref[20].

<i>Slot # 2</i>	<i>MixerB # 1</i>	<i>Supersector # 4</i>			<i>Slot # 3</i>	<i>MixerB # 2</i>	<i>Supersector # 4</i>		
Mixer Link#	AFE relative Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#	Mixer Link#	AFE Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#
15	1	59	LHB	2	15	8	58	LHB	2
14	5	56	RHB	1	14	7	53	RHB	1
13	1	59	RHB	3	13	8	58	RHB	2
12	6	57	LHB	1	12	3	52	RHB	3
11	5	56	LHB	4	11	6	57	RHB	2
10	3	52	LHB	1	10	6	57	LHB	3
9	8	58	LHB	1	9	6	57	LHB	2
8	3	52	RHB	4	8	2	54	LHB	3
7	7	53	LHB	4	7	8	58	RHB	3
6	6	57	RHB	4	6	8	58	LHB	3
5	2	54	RHB	1	5	3	52	LHB	2
4	8	58	RHB	4	4	2	54	RHB	2
3	4	55	RHB	1	3	4	55	RHB	2
2	4	55	LHB	4	2	4	55	LHB	3
1	2	54	LHB	4	1	6	57	RHB	3
0	CPS	70	RHB	2	0	CPS	70	LHB	3

Table 13.1, Slot#2 and Slot#3 (Supersector#4).

<i>Slot # 4</i>	<i>MixerB # 3</i>	<i>Supersector # 4</i>			<i>Slot # 5</i>	<i>MixerB # 4</i>	<i>Supersector # 4</i>		
Mixer Link#	AFE relative Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#	Mixer Link#	AFE Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#
15	5	56	LHB	3	15	1	59	LHB	1
14	5	56	RHB	2	14	5	56	LHB	2
13	2	54	LHB	1	13	1	59	RHB	4
12	7	53	LHB	3	12	3	52	LHB	4
11	3	52	RHB	2	11	7	53	RHB	3
10	6	57	RHB	1	10	3	52	RHB	1
9	2	54	LHB	2	9	7	53	LHB	2
8	3	52	LHB	3	8	2	54	RHB	4
7	7	53	RHB	2	7	7	53	LHB	1
6	6	57	LHB	4	6	5	56	RHB	4
5	8	58	RHB	1	5	5	56	RHB	3
4	8	58	LHB	4	4	5	56	LHB	1
3	4	55	RHB	3	3	4	55	RHB	4
2	4	55	LHB	2	2	4	55	LHB	1
1	2	54	RHB	3	1	7	53	RHB	4
0	CPS	70	RHB	3	0	CPS	70	LHB	2

Table 13.2, Slot#4 and Slot#5 (Supersector#4).

<i>Slot #6</i>	<i>MixerB # 1</i>	<i>Supersector # 5</i>			<i>Slot # 7</i>	<i>MixerB # 2</i>	<i>Supersector # 5</i>		
Mixer Link#	AFE relative Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#	Mixer Link#	AFE Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#
15	1	51	LHB	2	15	8	47	LHB	2
14	5	45	RHB	1	14	7	48	RHB	1
13	1	51	RHB	3	13	8	47	RHB	2
12	6	44	LHB	1	12	3	49	RHB	3
11	5	45	LHB	4	11	6	44	RHB	2
10	3	49	LHB	1	10	6	44	LHB	3
9	8	47	LHB	1	9	6	44	LHB	2
8	3	49	RHB	4	8	2	50	LHB	3
7	7	48	LHB	4	7	8	47	RHB	3
6	6	44	RHB	4	6	8	47	LHB	3
5	2	50	RHB	1	5	3	49	LHB	2
4	8	47	RHB	4	4	2	50	RHB	2
3	4	46	RHB	1	3	4	46	RHB	2
2	4	46	LHB	4	2	4	46	LHB	3
1	2	50	LHB	4	1	6	44	RHB	3
0	CPS	72	RHB	2	0	CPS	72	LHB	3

Table 13.3, Slot#6 and Slot#7 (Supersector#5).

<i>Slot #8</i>	<i>MixerB # 3</i>	<i>Supersector # 5</i>			<i>Slot # 9</i>	<i>MixerB # 4</i>	<i>Supersector # 5</i>		
Mixer Link#	AFE relative Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#	Mixer Link#	AFE Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#
15	5	45	LHB	3	15	1	51	LHB	1
14	5	45	RHB	2	14	5	45	LHB	2
13	2	50	LHB	1	13	1	51	RHB	4
12	7	48	LHB	3	12	3	49	LHB	4
11	3	49	RHB	2	11	7	48	RHB	3
10	6	44	RHB	1	10	3	49	RHB	1
9	2	50	LHB	2	9	7	48	LHB	2
8	3	49	LHB	3	8	2	50	RHB	4
7	7	48	RHB	2	7	7	48	LHB	1
6	6	44	LHB	4	6	5	45	RHB	4
5	8	47	RHB	1	5	5	45	RHB	3
4	8	47	LHB	4	4	5	45	LHB	1
3	4	46	RHB	3	3	4	46	RHB	4
2	4	46	LHB	2	2	4	46	LHB	1
1	2	50	RHB	3	1	7	48	RHB	4
0	CPS	72	RHB	3	0	CPS	72	LHB	2

Table 13.4, Slot#8 and Slot#9 (Supersector#5).

<i>Slot #10</i>	<i>MixerB # 1</i>	<i>Supersector # 1</i>			<i>Slot # 11</i>	<i>MixerB # 2</i>	<i>Supersector # 1</i>		
Mixer Link#	AFE relative Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#	Mixer Link#	AFE Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#
15	1	36	LHB	4	15	8	43	LHB	2
14	5	41	RHB	1	14	7	39	RHB	1
13	1	36	RHB	1	13	8	43	RHB	2
12	6	42	LHB	1	12	3	38	RHB	3
11	5	41	LHB	4	11	6	42	RHB	2
10	3	38	LHB	1	10	6	42	LHB	3
9	8	43	LHB	1	9	6	42	LHB	2
8	3	38	RHB	4	8	2	37	LHB	3
7	7	39	LHB	4	7	8	43	RHB	3
6	6	42	RHB	4	6	8	43	LHB	3
5	2	37	RHB	1	5	3	38	LHB	2
4	8	43	RHB	4	4	2	37	RHB	2
3	4	40	RHB	1	3	4	40	RHB	2
2	4	40	LHB	4	2	4	40	LHB	3
1	2	37	LHB	4	1	6	42	RHB	3
0	CPS	26	RHB	2	0	CPS	26	LHB	3

Table 13.5, Slot#10 and Slot#11 (Supersector#1).

<i>Slot # 12</i>	<i>MixerB # 3</i>	<i>Supersector # 1</i>			<i>Slot # 13</i>	<i>MixerB # 4</i>	<i>Supersector # 1</i>		
Mixer Link#	AFE relative Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#	Mixer Link#	AFE Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#
15	5	41	LHB	3	15	1	36	LHB	3
14	5	41	RHB	2	14	5	41	LHB	2
13	2	37	LHB	1	13	1	36	RHB	2
12	7	39	LHB	3	12	3	38	LHB	4
11	3	38	RHB	2	11	7	39	RHB	3
10	6	42	RHB	1	10	3	38	RHB	1
9	2	37	LHB	2	9	7	39	LHB	2
8	3	38	LHB	3	8	2	37	RHB	4
7	7	39	RHB	2	7	7	39	LHB	1
6	6	42	LHB	4	6	5	41	RHB	4
5	8	43	RHB	1	5	5	41	RHB	3
4	8	43	LHB	4	4	5	41	LHB	1
3	4	40	RHB	3	3	4	40	RHB	4
2	4	40	LHB	2	2	4	40	LHB	1
1	2	37	RHB	3	1	7	39	RHB	4
0	CPS	26	RHB	3	0	CPS	26	LHB	2

Table 13.6, Slot#12 and Slot#13 (Supersector#1).

<i>Slot #14</i>	<i>MixerB # 1</i>	<i>Supersector # 2</i>		
Mixer Link#	AFE relative Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#
15	1	36	LHB	2
14	5	30	RHB	1
13	1	36	RHB	3
12	6	29	LHB	1
11	5	30	LHB	4
10	3	34	LHB	1
9	8	32	LHB	1
8	3	34	RHB	4
7	7	33	LHB	4
6	6	29	RHB	4
5	2	35	RHB	1
4	8	32	RHB	4
3	4	31	RHB	1
2	4	31	LHB	4
1	2	35	LHB	4
0	CPS	28	RHB	2

<i>Slot # 15</i>	<i>MixerB # 2</i>	<i>Supersector # 2</i>		
Mixer Link#	AFE Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#
15	8	32	LHB	2
14	7	33	RHB	1
13	8	32	RHB	2
12	3	34	RHB	3
11	6	29	RHB	2
10	6	29	LHB	3
9	6	29	LHB	2
8	2	35	LHB	3
7	8	32	RHB	3
6	8	32	LHB	3
5	3	34	LHB	2
4	2	35	RHB	2
3	4	31	RHB	2
2	4	31	LHB	3
1	6	29	RHB	3
0	CPS	28	LHB	3

Table 13.7, Slot#14 and Slot#15 (Supersector#2).

<i>Slot # 16</i>	<i>MixerB # 3</i>	<i>Supersector # 2</i>		
Mixer Link#	AFE relative Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#
15	5	30	LHB	3
14	5	30	RHB	2
13	2	35	LHB	1
12	7	33	LHB	3
11	3	34	RHB	2
10	6	29	RHB	1
9	2	35	LHB	2
8	3	34	LHB	3
7	7	33	RHB	2
6	6	29	LHB	4
5	8	32	RHB	1
4	8	32	LHB	4
3	4	31	RHB	3
2	4	31	LHB	2
1	2	35	RHB	3
0	CPS	28	RHB	3

<i>Slot # 17</i>	<i>MixerB # 4</i>	<i>Supersector # 2</i>		
Mixer Link#	AFE Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#
15	1	36	LHB	1
14	5	30	LHB	2
13	1	36	RHB	4
12	3	34	LHB	4
11	7	33	RHB	3
10	3	34	RHB	1
9	7	33	LHB	2
8	2	35	RHB	4
7	7	33	LHB	1
6	5	30	RHB	4
5	5	30	RHB	3
4	5	30	LHB	1
3	4	31	RHB	4
2	4	31	LHB	1
1	7	33	RHB	4
0	CPS	28	LHB	2

Table 13.8, Slot#16 and Slot#17 (Supersector#2).

<i>Slot #18</i>	<i>MixerB # 1</i>	<i>Supersector # 3</i>		
Mixer Link#	AFE relative Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#
15	1	59	LHB	4
14	5	63	RHB	1
13	1	59	RHB	1
12	6	64	LHB	1
11	5	63	LHB	4
10	3	61	LHB	1
9	8	66	LHB	1
8	3	61	RHB	4
7	7	65	LHB	4
6	6	64	RHB	4
5	2	60	RHB	1
4	8	66	RHB	4
3	4	62	RHB	1
2	4	62	LHB	4
1	2	60	LHB	4
0	CPS	68	RHB	2

<i>Slot # 19</i>	<i>MixerB # 2</i>	<i>Supersector # 3</i>		
Mixer Link#	AFE Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#
15	8	66	LHB	2
14	7	65	RHB	1
13	8	66	RHB	2
12	3	61	RHB	3
11	6	64	RHB	2
10	6	64	LHB	3
9	6	64	LHB	2
8	2	60	LHB	3
7	8	66	RHB	3
6	8	66	LHB	3
5	3	61	LHB	2
4	2	60	RHB	2
3	4	62	RHB	2
2	4	62	LHB	3
1	6	64	RHB	3
0	CPS	68	LHB	3

Table 13.9, Slot#18 and Slot#19 (Supersector#3).

<i>Slot # 20</i>	<i>MixerB # 3</i>	<i>Supersector # 3</i>		
Mixer Link#	AFE relative Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#
15	5	63	LHB	3
14	5	63	RHB	2
13	2	60	LHB	1
12	7	65	LHB	3
11	3	61	RHB	2
10	6	64	RHB	1
9	2	60	LHB	2
8	3	61	LHB	3
7	7	65	RHB	2
6	6	64	LHB	4
5	8	66	RHB	1
4	8	66	LHB	4
3	4	62	RHB	3
2	4	62	LHB	2
1	2	60	RHB	3
0	CPS	68	RHB	3

<i>Slot # 21</i>	<i>MixerB # 4</i>	<i>Supersector # 3</i>		
Mixer Link#	AFE Cassette	AFE absolute Cassette	AFE LHB/RHB	AFE Link#
15	1	59	LHB	3
14	5	63	LHB	2
13	1	59	RHB	2
12	3	61	LHB	4
11	7	65	RHB	3
10	3	61	RHB	1
9	7	65	LHB	2
8	2	60	RHB	4
7	7	65	LHB	1
6	5	63	RHB	4
5	5	63	RHB	3
4	5	63	LHB	1
3	4	62	RHB	4
2	4	62	LHB	1
1	7	65	RHB	4
0	CPS	68	LHB	2

Table 13.10, Slot#20 and Slot#21 (Supersector#3).

13.2 Mixer System Input Links cabling map organized by cassette

<i>Absolute Cassette# 26</i>		<i>Relative Cassette# CPS</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1			
L	2	13 [4]	0	1
L	3	11 [2]	0	1
L	4			
R	1			
R	2	10 [1]	0	1
R	3	12 [3]	0	1
R	4			

<i>Absolute Cassette# 28</i>		<i>Relative Cassette# CPS</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1			
L	2	17 [4]	0	2
L	3	15 [2]	0	2
L	4			
R	1			
R	2	14 [1]	0	2
R	3	16 [3]	0	2
R	4			

Table 13.11, AFE Cassettes 26 (CPS) and 28 (CPS).

<i>Absolute Cassette# 29</i>		<i>Relative Cassette# 6</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	14 [1]	12	2
L	2	15 [2]	9	2
L	3	15 [2]	10	2
L	4	16 [3]	6	2
R	1	16 [3]	10	2
R	2	15 [2]	11	2
R	3	15 [2]	1	2
R	4	14 [1]	6	2

<i>Absolute Cassette# 30</i>		<i>Relative Cassette# 5</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	17 [4]	4	2
L	2	17 [4]	14	2
L	3	16 [3]	15	2
L	4	14 [1]	11	2
R	1	14 [1]	14	2
R	2	16 [3]	14	2
R	3	17 [4]	5	2
R	4	17 [4]	6	2

Table 13.12, AFE Cassettes 29 and 30.

<i>Absolute Cassette# 31</i>		<i>Relative Cassette# 4</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	17 [4]	2	2
L	2	16 [3]	2	2
L	3	15 [2]	2	2
L	4	14 [1]	2	2
R	1	14 [1]	3	2
R	2	15 [2]	3	2
R	3	16 [3]	3	2
R	4	17 [4]	3	2

<i>Absolute Cassette# 32</i>		<i>Relative Cassette# 8</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	14 [1]	9	2
L	2	15 [2]	15	2
L	3	15 [2]	6	2
L	4	16 [3]	4	2
R	1	16 [3]	5	2
R	2	15 [2]	13	2
R	3	15 [2]	7	2
R	4	14 [1]	4	2

Table 13.13, AFE Cassettes 31 and 32

<i>Absolute Cassette# 33</i>		<i>Relative Cassette# 7</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	17 [4]	7	2
L	2	17 [4]	9	2
L	3	16 [3]	12	2
L	4	14 [1]	7	2
R	1	15 [2]	14	2
R	2	16 [3]	7	2
R	3	17 [4]	11	2
R	4	17 [4]	1	2

<i>Absolute Cassette# 34</i>		<i>Relative Cassette# 3</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	14 [1]	10	2
L	2	15 [2]	5	2
L	3	16 [3]	8	2
L	4	17 [4]	12	2
R	1	17 [4]	10	2
R	2	16 [3]	11	2
R	3	15 [2]	12	2
R	4	14 [1]	8	2

Table 13.14, AFE Cassettes 33 and 34

<i>Absolute Cassette# 35</i>		<i>Relative Cassette# 2</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	16 [3]	13	2
L	2	16 [3]	9	2
L	3	15 [2]	8	2
L	4	14 [1]	1	2
R	1	14 [1]	5	2
R	2	15 [2]	4	2
R	3	16 [3]	1	2
R	4	17 [4]	8	2

<i>Absolute Cassette# 36</i>		<i>Relative Cassette# 1</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	17 [4]	15	2
L	2	14 [1]	15	2
L	3	13 [4]	15	1
L	4	10 [1]	15	1
R	1	10 [1]	13	1
R	2	13 [4]	13	1
R	3	14 [1]	13	2
R	4	17 [4]	13	2

Table 13.15, AFE Cassettes 35 and 36

<i>Absolute Cassette# 37</i>		<i>Relative Cassette# 2</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	12 [3]	13	1
L	2	12 [3]	9	1
L	3	11 [2]	8	1
L	4	10 [1]	1	1
R	1	10 [1]	5	1
R	2	11 [2]	4	1
R	3	12 [3]	1	1
R	4	13 [4]	8	1

<i>Absolute Cassette# 38</i>		<i>Relative Cassette# 3</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	10 [1]	10	1
L	2	11 [2]	5	1
L	3	12 [3]	8	1
L	4	13 [4]	12	1
R	1	13 [4]	10	1
R	2	12 [3]	11	1
R	3	11 [2]	12	1
R	4	10 [1]	8	1

Table 13.16, AFE Cassettes 37 and 38

<i>Absolute Cassette# 39</i>		<i>Relative Cassette# 7</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	13 [4]	7	1
L	2	13 [4]	9	1
L	3	12 [3]	12	1
L	4	10 [1]	7	1
R	1	11 [2]	14	1
R	2	12 [3]	7	1
R	3	13 [4]	11	1
R	4	13 [4]	1	1

<i>Absolute Cassette# 40</i>		<i>Relative Cassette#4</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	13 [4]	2	1
L	2	12 [3]	2	1
L	3	11 [2]	2	1
L	4	10 [1]	2	1
R	1	10 [1]	3	1
R	2	11 [2]	3	1
R	3	12 [3]	3	1
R	4	13 [4]	3	1

Table 13.17, AFE Cassettes 39 and 40

<i>Absolute Cassette#41</i>		<i>Relative Cassette#5</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	13 [4]	4	1
L	2	13 [4]	14	1
L	3	12 [3]	15	1
L	4	10 [1]	11	1
R	1	10 [1]	14	1
R	2	12 [3]	14	1
R	3	13 [4]	5	1
R	4	13 [4]	6	1

<i>Absolute Cassette#42</i>		<i>Relative Cassette#6</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	10 [1]	12	1
L	2	11 [2]	9	1
L	3	11 [2]	10	1
L	4	12 [3]	6	1
R	1	12 [3]	10	1
R	2	11 [2]	11	1
R	3	11 [2]	1	1
R	4	10 [1]	6	1

Table 13.18, AFE Cassettes 41 and 42

<i>Absolute Cassette#43</i>		<i>Relative Cassette#8</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	10 [1]	9	1
L	2	11 [2]	15	1
L	3	11 [2]	6	1
L	4	12 [3]	4	1
R	1	12 [3]	5	1
R	2	11 [2]	13	1
R	3	11 [2]	7	1
R	4	10 [1]	4	1

<i>Absolute Cassette#44</i>		<i>Relative Cassette#6</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	6 [1]	12	5
L	2	7 [2]	9	5
L	3	7 [2]	10	5
L	4	8 [3]	6	5
R	1	8 [3]	10	5
R	2	7 [2]	11	5
R	3	7 [2]	1	5
R	4	6 [1]	6	5

Table 13.19, AFE Cassettes 43 and 44

<i>Absolute Cassette#45</i>		<i>Relative Cassette#5</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	9 [4]	4	5
L	2	9 [4]	14	5
L	3	8 [3]	15	5
L	4	6 [1]	11	5
R	1	6 [1]	14	5
R	2	8 [3]	14	5
R	3	9 [4]	5	5
R	4	9 [4]	6	5

<i>Absolute Cassette#46</i>		<i>Relative Cassette#4</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	9 [4]	2	5
L	2	8 [3]	2	5
L	3	7 [2]	2	5
L	4	6 [1]	2	5
R	1	6 [1]	3	5
R	2	7 [2]	3	5
R	3	8 [3]	3	5
R	4	9 [4]	3	5

Table 13.20, AFE Cassettes 45 and 46

<i>Absolute Cassette#47</i>		<i>Relative Cassette#8</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	6 [1]	9	5
L	2	7 [2]	15	5
L	3	7 [2]	6	5
L	4	8 [3]	4	5
R	1	8 [3]	5	5
R	2	7 [2]	13	5
R	3	7 [2]	7	5
R	4	6 [1]	4	5

<i>Absolute Cassette#48</i>		<i>Relative Cassette#7</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	9 [4]	7	5
L	2	9 [4]	9	5
L	3	8 [3]	12	5
L	4	6 [1]	7	5
R	1	7 [2]	14	5
R	2	8 [3]	7	5
R	3	9 [4]	11	5
R	4	9 [4]	1	5

Table 13.21, AFE Cassettes 47 and 48

<i>Absolute Cassette#49</i>		<i>Relative Cassette#3</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	6 [1]	10	5
L	2	7 [2]	5	5
L	3	8 [3]	8	5
L	4	9 [4]	12	5
R	1	9 [4]	10	5
R	2	8 [3]	11	5
R	3	7 [2]	12	5
R	4	6 [1]	8	5

<i>Absolute Cassette#50</i>		<i>Relative Cassette#2</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	8 [3]	13	5
L	2	8 [3]	9	5
L	3	7 [2]	8	5
L	4	6 [1]	1	5
R	1	6 [1]	5	5
R	2	7 [2]	4	5
R	3	8 [3]	1	5
R	4	9 [4]	8	5

Table 13.22, AFE Cassettes 49 and 50

<i>Absolute Cassette#51</i>		<i>Relative Cassette#1</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	9 [4]	15	5
L	2	6 [1]	15	5
L	3			
L	4			
R	1			
R	2			
R	3	6 [1]	13	5
R	4	9 [4]	13	5

<i>Absolute Cassette#52</i>		<i>Relative Cassette#3</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	2 [1]	10	4
L	2	3 [2]	5	4
L	3	4 [3]	8	4
L	4	5 [4]	12	4
R	1	5 [4]	10	4
R	2	4 [3]	11	4
R	3	3 [2]	12	4
R	4	2 [1]	8	4

Table 13.23, AFE Cassettes 51 and 52

<i>Absolute Cassette#53</i>		<i>Relative Cassette#7</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	5 [4]	7	4
L	2	5 [4]	9	4
L	3	4 [3]	12	4
L	4	2 [1]	7	4
R	1	3 [2]	14	4
R	2	4 [3]	7	4
R	3	5 [4]	11	4
R	4	5 [4]	1	4

<i>Absolute Cassette#54</i>		<i>Relative Cassette#2</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	4 [3]	13	4
L	2	4 [3]	9	4
L	3	3 [2]	8	4
L	4	2 [1]	1	4
R	1	2 [1]	5	4
R	2	3 [2]	4	4
R	3	4 [3]	1	4
R	4	5 [4]	8	4

Table 13.24, AFE Cassettes 53 and 54

<i>Absolute Cassette#55</i>		<i>Relative Cassette#4</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	5 [4]	2	4
L	2	4 [3]	2	4
L	3	3 [2]	2	4
L	4	2 [1]	2	4
R	1	2 [1]	3	4
R	2	3 [2]	3	4
R	3	4 [3]	3	4
R	4	5 [4]	3	4

<i>Absolute Cassette#56</i>		<i>Relative Cassette#5</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	5 [4]	4	4
L	2	5 [4]	14	4
L	3	4 [3]	15	4
L	4	2 [1]	11	4
R	1	2 [1]	14	4
R	2	4 [3]	14	4
R	3	5 [4]	5	4
R	4	5 [4]	6	4

Table 13.25, AFE Cassettes 55 and 56

<i>Absolute Cassette#57</i>		<i>Relative Cassette#6</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	2 [1]	12	4
L	2	3 [2]	9	4
L	3	3 [2]	10	4
L	4	4 [3]	6	4
R	1	4 [3]	10	4
R	2	3 [2]	11	4
R	3	3 [2]	1	4
R	4	2 [1]	6	4

<i>Absolute Cassette#58</i>		<i>Relative Cassette#8</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	2 [1]	9	4
L	2	3 [2]	15	4
L	3	3 [2]	6	4
L	4	4 [3]	4	4
R	1	4 [3]	5	4
R	2	3 [2]	13	4
R	3	3 [2]	7	4
R	4	2 [1]	4	4

Table 13.26, AFE Cassettes 57 and 58

<i>Absolute Cassette#59</i>		<i>Relative Cassette#1</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	5 [4]	15	4
L	2	2 [1]	15	4
L	3	21 [4]	15	3
L	4	18 [1]	15	3
R	1	18 [1]	13	3
R	2	21 [4]	13	3
R	3	2 [1]	13	4
R	4	5 [4]	13	4

<i>Absolute Cassette#60</i>		<i>Relative Cassette#2</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	20 [3]	13	3
L	2	20 [3]	9	3
L	3	19 [2]	8	3
L	4	18 [1]	1	3
R	1	18 [1]	5	3
R	2	19 [2]	4	3
R	3	20 [3]	1	3
R	4	21 [4]	8	3

Table 13.27, AFE Cassettes 59 and 60

<i>Absolute Cassette#61</i>		<i>Relative Cassette#3</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	18 [1]	10	3
L	2	19 [2]	5	3
L	3	20 [3]	8	3
L	4	21 [4]	12	3
R	1	21 [4]	10	3
R	2	20 [3]	11	3
R	3	19 [2]	12	3
R	4	18 [1]	8	3

<i>Absolute Cassette#62</i>		<i>Relative Cassette#4</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	21 [4]	2	3
L	2	20 [3]	2	3
L	3	19 [2]	2	3
L	4	18 [1]	2	3
R	1	18 [1]	3	3
R	2	19 [2]	3	3
R	3	20 [3]	3	3
R	4	21 [4]	3	3

Table 13.28, AFE Cassettes 61 and 62

<i>Absolute Cassette#63</i>		<i>Relative Cassette#5</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	21 [4]	4	3
L	2	21 [4]	14	3
L	3	20 [3]	15	3
L	4	18 [1]	11	3
R	1	18 [1]	14	3
R	2	20 [3]	14	3
R	3	21 [4]	5	3
R	4	21 [4]	6	3

<i>Absolute Cassette#64</i>		<i>Relative Cassette#6</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	18 [1]	12	3
L	2	19 [2]	9	3
L	3	19 [2]	10	3
L	4	20 [3]	6	3
R	1	20 [3]	10	3
R	2	19 [2]	11	3
R	3	19 [2]	1	3
R	4	18 [1]	6	3

Table 13.29, AFE Cassettes 63 and 64

<i>Absolute Cassette#65</i>		<i>Relative Cassette#7</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	21 [4]	7	3
L	2	21 [4]	9	3
L	3	20 [3]	12	3
L	4	18 [1]	7	3
R	1	19 [2]	14	3
R	2	20 [3]	7	3
R	3	21 [4]	11	3
R	4	21 [4]	1	3

<i>Absolute Cassette#66</i>		<i>Relative Cassette#8</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1	18 [1]	9	3
L	2	19 [2]	15	3
L	3	19 [2]	6	3
L	4	20 [3]	4	3
R	1	20 [3]	5	3
R	2	19 [2]	13	3
R	3	19 [2]	7	3
R	4	18 [1]	4	3

Table 13.30, AFE Cassettes 65 and 66

<i>Absolute Cassette# 68</i>		<i>Relative Cassette# CPS</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1			
L	2	21 [4]	0	3
L	3	19 [2]	0	3
L	4			
R	1			
R	2	18 [1]	0	3
R	3	20 [3]	0	3
R	4			

<i>Absolute Cassette# 70</i>		<i>Relative Cassette# CPS</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1			
L	2	5 [4]	0	4
L	3	3 [2]	0	4
L	4			
R	1			
R	2	2 [1]	0	4
R	3	4 [3]	0	4
R	4			

Table 13.31, AFE Cassettes 68 (CPS) and 70 (CPS).

<i>Absolute Cassette# 72</i>		<i>Relative Cassette# CPS</i>		
L/R	AFE Link#	Mixer Slot # [MB#]	Mixer Link#	Super Sector #
L	1			
L	2	9 [4]	0	5
L	3	7 [2]	0	5
L	4			
R	1			
R	2	6 [1]	0	5
R	3	8 [3]	0	5
R	4			

Table 13.32, AFE Cassette 72 (CPS).

Relative Cassette#	Absolute Cassette Number				
	Super sector 1	Super sector 2	Super sector 3	Super sector 4	Super sector 5
1	36(Module 1-4)	36(Module 5-8)	59(Module 1-4)	59(Module 5-8)	51(Module 5-8)
2	37	35	60	54	50
3	38	34	61	52	49
4	40	31	62	55	46
5	41	30	63	56	45
6	42	29	64	57	44
7	39	33	65	53	48
8	43	32	66	58	47
CPS	26	28	68	70	72

Table 13.33, Relative and Absolute Cassette numbers.

13.3 Mixer System Output Links cabling map

Mixer board output links arrangement on the front panel			DFE board input links arrangement on the front panel		
Mixer Link#	Link Color [DFE Link#]	Mixer Link PORT# (for cabling)	DFE Link#	Link Color	DFE Link PORT# (for cabling)
Row of pins used for JTAG			1 unused row of pins		
17	Red [0]	1	0	Red (copy)	1
16	Red [5]	2	2 unused row of pins		
15	Blue [7]	3	1	not used.	2
14	Yellow [6]	4	2 unused row of pins		
13	Purple [3]	5	2	Orange	3
12	Orange [2]	6	2 unused row of pins		
11	Green [4]	7	4	Green	4
10	Green [9]	8	2 unused row of pins		
Unused row of pins			3	Purple	5
07	Red [0]	9	2 unused row of pins		
06	Red [5]	10	5	Red	6
05	Blue [7]	11	2 unused row of pins		
04	Yellow [6]	12	7	Blue	7
03	Purple [3]	13	2 unused row of pins		
02	Orange [2]	14	6	Yellow	8
01	Green [4]	15	2 unused row of pins		
00	Green [9]	16	8	not used	9
			2 unused row of pins		
			9	Green (copy)	10
			1 unused row of pins		

Table 13.34, Mixer Board output links and DFE input links arrangements on the front panels.

Slot# 2	MB# 1	Supersector# 4	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-3	4
16	Red [L5-P6]	PC03-3	3
15	Blue [L7-P7]	PC03-3	3
14	Yellow [L6-P8]	PC03-3	3
13	Purple [L3-P5]	PC03-3	3
12	Orange [L2-P3]	PC03-3	3
11	Green [L4-P4]	PC03-3	3
10	Green [L9-P10]	PC03-3	2
07	Red [L0-P1]	PC03-3	3
06	Red [L5-P6]	PC03-3	2
05	Blue [L7-P7]	PC03-3	2
04	Yellow [L6-P8]	PC03-3	2
03	Purple [L3-P5]	PC03-3	2
02	Orange [L2-P3]	PC03-3	2
01	Green [L4-P4]	PC03-3	2
00	Green [L9-P10]	PC03-2	21

Slot# 3	MB# 2	Supersector# 4	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-3	6
16	Red [L5-P6]	PC03-3	5
15	Blue [L7-P7]	PC03-3	5
14	Yellow [L6-P8]	PC03-3	5
13	Purple [L3-P5]	PC03-3	5
12	Orange [L2-P3]	PC03-3	5
11	Green [L4-P4]	PC03-3	5
10	Green [L9-P10]	PC03-3	4
07	Red [L0-P1]	PC03-3	5
06	Red [L5-P6]	PC03-3	4
05	Blue [L7-P7]	PC03-3	4
04	Yellow [L6-P8]	PC03-3	4
03	Purple [L3-P5]	PC03-3	4
02	Orange [L2-P3]	PC03-3	4
01	Green [L4-P4]	PC03-3	4
00	Green [L9-P10]	PC03-3	3

Table 13.35, Slot#2 and Slot#3 (Supersector#4).

Slot# 4	MB# 3	Supersector# 4	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-3	8
16	Red [L5-P6]	PC03-3	7
15	Blue [L7-P7]	PC03-3	7
14	Yellow [L6-P8]	PC03-3	7
13	Purple [L3-P5]	PC03-3	7
12	Orange [L2-P3]	PC03-3	7
11	Green [L4-P4]	PC03-3	7
10	Green [L9-P10]	PC03-3	6
07	Red [L0-P1]	PC03-3	7
06	Red [L5-P6]	PC03-3	6
05	Blue [L7-P7]	PC03-3	6
04	Yellow [L6-P8]	PC03-3	6
03	Purple [L3-P5]	PC03-3	6
02	Orange [L2-P3]	PC03-3	6
01	Green [L4-P4]	PC03-3	6
00	Green [L9-P10]	PC03-3	5

Slot# 5	MB# 4	Supersector# 4	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-3	10
16	Red [L5-P6]	PC03-3	9
15	Blue [L7-P7]	PC03-3	9
14	Yellow [L6-P8]	PC03-3	9
13	Purple [L3-P5]	PC03-3	9
12	Orange [L2-P3]	PC03-3	9
11	Green [L4-P4]	PC03-3	9
10	Green [L9-P10]	PC03-3	8
07	Red [L0-P1]	PC03-3	9
06	Red [L5-P6]	PC03-3	8
05	Blue [L7-P7]	PC03-3	8
04	Yellow [L6-P8]	PC03-3	8
03	Purple [L3-P5]	PC03-3	8
02	Orange [L2-P3]	PC03-3	8
01	Green [L4-P4]	PC03-3	8
00	Green [L9-P10]	PC03-3	7

Table 13.36, Slot#4 and Slot#5 (Supersector#4).

Slot# 6	MB# 1	Supersector# 5	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-3	12
16	Red [L5-P6]	PC03-3	11
15	Blue [L7-P7]	PC03-3	11
14	Yellow [L6-P8]	PC03-3	11
13	Purple [L3-P5]	PC03-3	11
12	Orange [L2-P3]	PC03-3	11
11	Green [L4-P4]	PC03-3	11
10	Green [L9-P10]	PC03-3	10
07	Red [L0-P1]	PC03-3	11
06	Red [L5-P6]	PC03-3	10
05	Blue [L7-P7]	PC03-3	10
04	Yellow [L6-P8]	PC03-3	10
03	Purple [L3-P5]	PC03-3	10
02	Orange [L2-P3]	PC03-3	10
01	Green [L4-P4]	PC03-3	10
00	Green [L9-P10]	PC03-3	9

Slot# 7	MB# 2	Supersector# 5	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-3	14
16	Red [L5-P6]	PC03-3	13
15	Blue [L7-P7]	PC03-3	13
14	Yellow [L6-P8]	PC03-3	13
13	Purple [L3-P5]	PC03-3	13
12	Orange [L2-P3]	PC03-3	13
11	Green [L4-P4]	PC03-3	13
10	Green [L9-P10]	PC03-3	12
07	Red [L0-P1]	PC03-3	13
06	Red [L5-P6]	PC03-3	12
05	Blue [L7-P7]	PC03-3	12
04	Yellow [L6-P8]	PC03-3	12
03	Purple [L3-P5]	PC03-3	12
02	Orange [L2-P3]	PC03-3	12
01	Green [L4-P4]	PC03-3	12
00	Green [L9-P10]	PC03-3	11

Table 13.37, Slot#6 and Slot#7 (Supersector#5).

Slot# 8	MB# 3	Supersector# 5	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-3	16
16	Red [L5-P6]	PC03-3	15
15	Blue [L7-P7]	PC03-3	15
14	Yellow [L6-P8]	PC03-3	15
13	Purple [L3-P5]	PC03-3	15
12	Orange [L2-P3]	PC03-3	15
11	Green [L4-P4]	PC03-3	15
10	Green [L9-P10]	PC03-3	14
07	Red [L0-P1]	PC03-3	15
06	Red [L5-P6]	PC03-3	14
05	Blue [L7-P7]	PC03-3	14
04	Yellow [L6-P8]	PC03-3	14
03	Purple [L3-P5]	PC03-3	14
02	Orange [L2-P3]	PC03-3	14
01	Green [L4-P4]	PC03-3	14
00	Green [L9-P10]	PC03-3	13

Slot# 9	MB# 4	Supersector# 5	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-3	18
16	Red [L5-P6]	PC03-3	17
15	Blue [L7-P7]	PC03-3	17
14	Yellow [L6-P8]	PC03-3	17
13	Purple [L3-P5]	PC03-3	17
12	Orange [L2-P3]	PC03-3	17
11	Green [L4-P4]	PC03-3	17
10	Green [L9-P10]	PC03-3	16
07	Red [L0-P1]	PC03-3	17
06	Red [L5-P6]	PC03-3	16
05	Blue [L7-P7]	PC03-3	16
04	Yellow [L6-P8]	PC03-3	16
03	Purple [L3-P5]	PC03-3	16
02	Orange [L2-P3]	PC03-3	16
01	Green [L4-P4]	PC03-3	16
00	Green [L9-P10]	PC03-3	15

Table 13.38, Slot#8 and Slot#9 (Supersector#5).

Slot# 10	MB# 1	Supersector# 1	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-3	20
16	Red [L5-P6]	PC03-3	19
15	Blue [L7-P7]	PC03-3	19
14	Yellow [L6-P8]	PC03-3	19
13	Purple [L3-P5]	PC03-3	19
12	Orange [L2-P3]	PC03-3	19
11	Green [L4-P4]	PC03-3	19
10	Green [L9-P10]	PC03-3	18
07	Red [L0-P1]	PC03-3	19
06	Red [L5-P6]	PC03-3	18
05	Blue [L7-P7]	PC03-3	18
04	Yellow [L6-P8]	PC03-3	18
03	Purple [L3-P5]	PC03-3	18
02	Orange [L2-P3]	PC03-3	18
01	Green [L4-P4]	PC03-3	18
00	Green [L9-P10]	PC03-3	17

Slot# 11	MB# 2	Supersector# 1	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-2	2
16	Red [L5-P6]	PC03-3	21
15	Blue [L7-P7]	PC03-3	21
14	Yellow [L6-P8]	PC03-3	21
13	Purple [L3-P5]	PC03-3	21
12	Orange [L2-P3]	PC03-3	21
11	Green [L4-P4]	PC03-3	21
10	Green [L9-P10]	PC03-3	20
07	Red [L0-P1]	PC03-3	21
06	Red [L5-P6]	PC03-3	20
05	Blue [L7-P7]	PC03-3	20
04	Yellow [L6-P8]	PC03-3	20
03	Purple [L3-P5]	PC03-3	20
02	Orange [L2-P3]	PC03-3	20
01	Green [L4-P4]	PC03-3	20
00	Green [L9-P10]	PC03-3	19

Table 13.39, Slot#10 and Slot#11 (Supersector#1).

Slot# 12	MB# 3	Supersector# 1	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-2	4
16	Red [L5-P6]	PC03-2	3
15	Blue [L7-P7]	PC03-2	3
14	Yellow [L6-P8]	PC03-2	3
13	Purple [L3-P5]	PC03-2	3
12	Orange [L2-P3]	PC03-2	3
11	Green [L4-P4]	PC03-2	3
10	Green [L9-P10]	PC03-2	2
07	Red [L0-P1]	PC03-2	3
06	Red [L5-P6]	PC03-2	2
05	Blue [L7-P7]	PC03-2	2
04	Yellow [L6-P8]	PC03-2	2
03	Purple [L3-P5]	PC03-2	2
02	Orange [L2-P3]	PC03-2	2
01	Green [L4-P4]	PC03-2	2
00	Green [L9-P10]	PC03-3	21

Slot# 13	MB# 4	Supersector# 1	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-2	6
16	Red [L5-P6]	PC03-2	5
15	Blue [L7-P7]	PC03-2	5
14	Yellow [L6-P8]	PC03-2	5
13	Purple [L3-P5]	PC03-2	5
12	Orange [L2-P3]	PC03-2	5
11	Green [L4-P4]	PC03-2	5
10	Green [L9-P10]	PC03-2	4
07	Red [L0-P1]	PC03-2	5
06	Red [L5-P6]	PC03-2	4
05	Blue [L7-P7]	PC03-2	4
04	Yellow [L6-P8]	PC03-2	4
03	Purple [L3-P5]	PC03-2	4
02	Orange [L2-P3]	PC03-2	4
01	Green [L4-P4]	PC03-2	4
00	Green [L9-P10]	PC03-2	3

Table 13.40, Slot#12 and Slot#13 (Supersector#1).

Slot# 14	MB# 1	Supersector# 2	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-2	8
16	Red [L5-P6]	PC03-2	7
15	Blue [L7-P7]	PC03-2	7
14	Yellow [L6-P8]	PC03-2	7
13	Purple [L3-P5]	PC03-2	7
12	Orange [L2-P3]	PC03-2	7
11	Green [L4-P4]	PC03-2	7
10	Green [L9-P10]	PC03-2	6
07	Red [L0-P1]	PC03-2	7
06	Red [L5-P6]	PC03-2	6
05	Blue [L7-P7]	PC03-2	6
04	Yellow [L6-P8]	PC03-2	6
03	Purple [L3-P5]	PC03-2	6
02	Orange [L2-P3]	PC03-2	6
01	Green [L4-P4]	PC03-2	6
00	Green [L9-P10]	PC03-2	5

Slot# 15	MB# 2	Supersector# 2	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-2	10
16	Red [L5-P6]	PC03-2	9
15	Blue [L7-P7]	PC03-2	9
14	Yellow [L6-P8]	PC03-2	9
13	Purple [L3-P5]	PC03-2	9
12	Orange [L2-P3]	PC03-2	9
11	Green [L4-P4]	PC03-2	9
10	Green [L9-P10]	PC03-2	8
07	Red [L0-P1]	PC03-2	9
06	Red [L5-P6]	PC03-2	8
05	Blue [L7-P7]	PC03-2	8
04	Yellow [L6-P8]	PC03-2	8
03	Purple [L3-P5]	PC03-2	8
02	Orange [L2-P3]	PC03-2	8
01	Green [L4-P4]	PC03-2	8
00	Green [L9-P10]	PC03-2	7

Table 13.41, Slot#14 and Slot#15 (Supersector#2).

Slot# 16	MB# 3	Supersector# 2	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-2	12
16	Red [L5-P6]	PC03-2	11
15	Blue [L7-P7]	PC03-2	11
14	Yellow [L6-P8]	PC03-2	11
13	Purple [L3-P5]	PC03-2	11
12	Orange [L2-P3]	PC03-2	11
11	Green [L4-P4]	PC03-2	11
10	Green [L9-P10]	PC03-2	10
07	Red [L0-P1]	PC03-2	11
06	Red [L5-P6]	PC03-2	10
05	Blue [L7-P7]	PC03-2	10
04	Yellow [L6-P8]	PC03-2	10
03	Purple [L3-P5]	PC03-2	10
02	Orange [L2-P3]	PC03-2	10
01	Green [L4-P4]	PC03-2	10
00	Green [L9-P10]	PC03-2	9

Slot# 17	MB# 4	Supersector# 2	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-2	14
16	Red [L5-P6]	PC03-2	13
15	Blue [L7-P7]	PC03-2	13
14	Yellow [L6-P8]	PC03-2	13
13	Purple [L3-P5]	PC03-2	13
12	Orange [L2-P3]	PC03-2	13
11	Green [L4-P4]	PC03-2	13
10	Green [L9-P10]	PC03-2	12
07	Red [L0-P1]	PC03-2	13
06	Red [L5-P6]	PC03-2	12
05	Blue [L7-P7]	PC03-2	12
04	Yellow [L6-P8]	PC03-2	12
03	Purple [L3-P5]	PC03-2	12
02	Orange [L2-P3]	PC03-2	12
01	Green [L4-P4]	PC03-2	12
00	Green [L9-P10]	PC03-2	11

Table 13.42, Slot#16 and Slot#17 (Supersector#2).

Slot# 18	MB# 1	Supersector# 3	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-2	16
16	Red [L5-P6]	PC03-2	15
15	Blue [L7-P7]	PC03-2	15
14	Yellow [L6-P8]	PC03-2	15
13	Purple [L3-P5]	PC03-2	15
12	Orange [L2-P3]	PC03-2	15
11	Green [L4-P4]	PC03-2	15
10	Green [L9-P10]	PC03-2	14
07	Red [L0-P1]	PC03-2	15
06	Red [L5-P6]	PC03-2	14
05	Blue [L7-P7]	PC03-2	14
04	Yellow [L6-P8]	PC03-2	14
03	Purple [L3-P5]	PC03-2	14
02	Orange [L2-P3]	PC03-2	14
01	Green [L4-P4]	PC03-2	14
00	Green [L9-P10]	PC03-2	13

Slot# 19	MB# 2	Supersector# 3	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-2	18
16	Red [L5-P6]	PC03-2	17
15	Blue [L7-P7]	PC03-2	17
14	Yellow [L6-P8]	PC03-2	17
13	Purple [L3-P5]	PC03-2	17
12	Orange [L2-P3]	PC03-2	17
11	Green [L4-P4]	PC03-2	17
10	Green [L9-P10]	PC03-2	16
07	Red [L0-P1]	PC03-2	17
06	Red [L5-P6]	PC03-2	16
05	Blue [L7-P7]	PC03-2	16
04	Yellow [L6-P8]	PC03-2	16
03	Purple [L3-P5]	PC03-2	16
02	Orange [L2-P3]	PC03-2	16
01	Green [L4-P4]	PC03-2	16
00	Green [L9-P10]	PC03-2	15

Table 13.43, Slot#18 and Slot#19 (Supersector#3).

Slot# 20	MB# 3	Supersector# 3	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-2	20
16	Red [L5-P6]	PC03-2	19
15	Blue [L7-P7]	PC03-2	19
14	Yellow [L6-P8]	PC03-2	19
13	Purple [L3-P5]	PC03-2	19
12	Orange [L2-P3]	PC03-2	19
11	Green [L4-P4]	PC03-2	19
10	Green [L9-P10]	PC03-2	18
07	Red [L0-P1]	PC03-2	19
06	Red [L5-P6]	PC03-2	18
05	Blue [L7-P7]	PC03-2	18
04	Yellow [L6-P8]	PC03-2	18
03	Purple [L3-P5]	PC03-2	18
02	Orange [L2-P3]	PC03-2	18
01	Green [L4-P4]	PC03-2	18
00	Green [L9-P10]	PC03-2	17

Slot# 21	MB# 4	Supersector# 3	
Mixer Link#	Color [DFE Link#, Port#]	DFE Subrack	DFE Slot
17	Red [L0-P1]	PC03-3	2
16	Red [L5-P6]	PC03-2	21
15	Blue [L7-P7]	PC03-2	21
14	Yellow [L6-P8]	PC03-2	21
13	Purple [L3-P5]	PC03-2	21
12	Orange [L2-P3]	PC03-2	21
11	Green [L4-P4]	PC03-2	21
10	Green [L9-P10]	PC03-2	20
07	Red [L0-P1]	PC03-2	21
06	Red [L5-P6]	PC03-2	20
05	Blue [L7-P7]	PC03-2	20
04	Yellow [L6-P8]	PC03-2	20
03	Purple [L3-P5]	PC03-2	20
02	Orange [L2-P3]	PC03-2	20
01	Green [L4-P4]	PC03-2	20
00	Green [L9-P10]	PC03-2	19

Table 13.44, Slot#20 and Slot#21 (Supersector#3).

14. Appendix H – Subrack Controller

14.1 Subrack Controller

Most of the subrack controller information is derived from [Ref. 5].

The Digital Front End Controller (DFEC) sits in slot 1 of the DFE and Mixer subracks, and is responsible for downloading device configuration data files to DFE motherboards and Mixer boards. Additionally, the DFEC monitors the status of the boards in the subrack and makes this data available (via a 1553 interface) to the DZERO slow monitoring system.

The primary function of the DFEC is to quickly download configuration data to the devices on the DFE motherboards and Mixer boards.

Each subrack hosts 20 boards, and each board can have up to 16 devices. Furthermore, the firmware in each of the devices may be unique, thus the controller must be able to manage configuration files for up to 320 devices. For diagnostic reasons, the DFEC board includes enough non-volatile memory (CompactFlash™ card) so that at least two configuration files for each device can be stored locally. The Mixer subrack requires a 128MB or 64MB CompactFlash™ card.

The DFEC uses MSDOS FAT16 file system, allowing for easy file transfers directly to and from the CompactFlash™ card using a commercially available card reader. Files can also be accessed over the 1553 network once the DFEC is installed on the D0 detector platform.

Communications between the Mixer and DFE subracks and the outside world occur through a 1553 interface. The DFEC appears on the 1553 network as a single Remote Terminal (RT). The 1553 bus master can read and write to a small dual port memory located on the DFEC. Using a dual port memory allows for greater decoupling between the 1553 protocol timing and the DFEC microcontroller.

Essentially the DFEC microcontroller acts as a command processor. The 1553 master writes commands and data into the dual port memory, and then generates an interrupt on the microcontroller. The microcontroller wakes up, executes the command(s) and then goes back to idle [Ref. 5d].

Basic status information is read from the Mixer and DFE boards over a dedicated slow monitoring serial bus. This information is continually being collected on the DFEC and made available to the 1553 host. The information collected from the mixer system boards is described in paragraph 4.6.

The DFEC communicates with the Mixer boards over a simple 16-bit address 8-bit data bus (Paragraph 4.5). This bus is not VME compatible.

An Atmel ATMEGA103 is used on the DFEC. It is flash based and supports in-system programmability and contains a debugger that allows the user to step through the code one instruction at a time and set breakpoints, etc. The microcontroller on the DFEC runs off of a 6MHz clock.

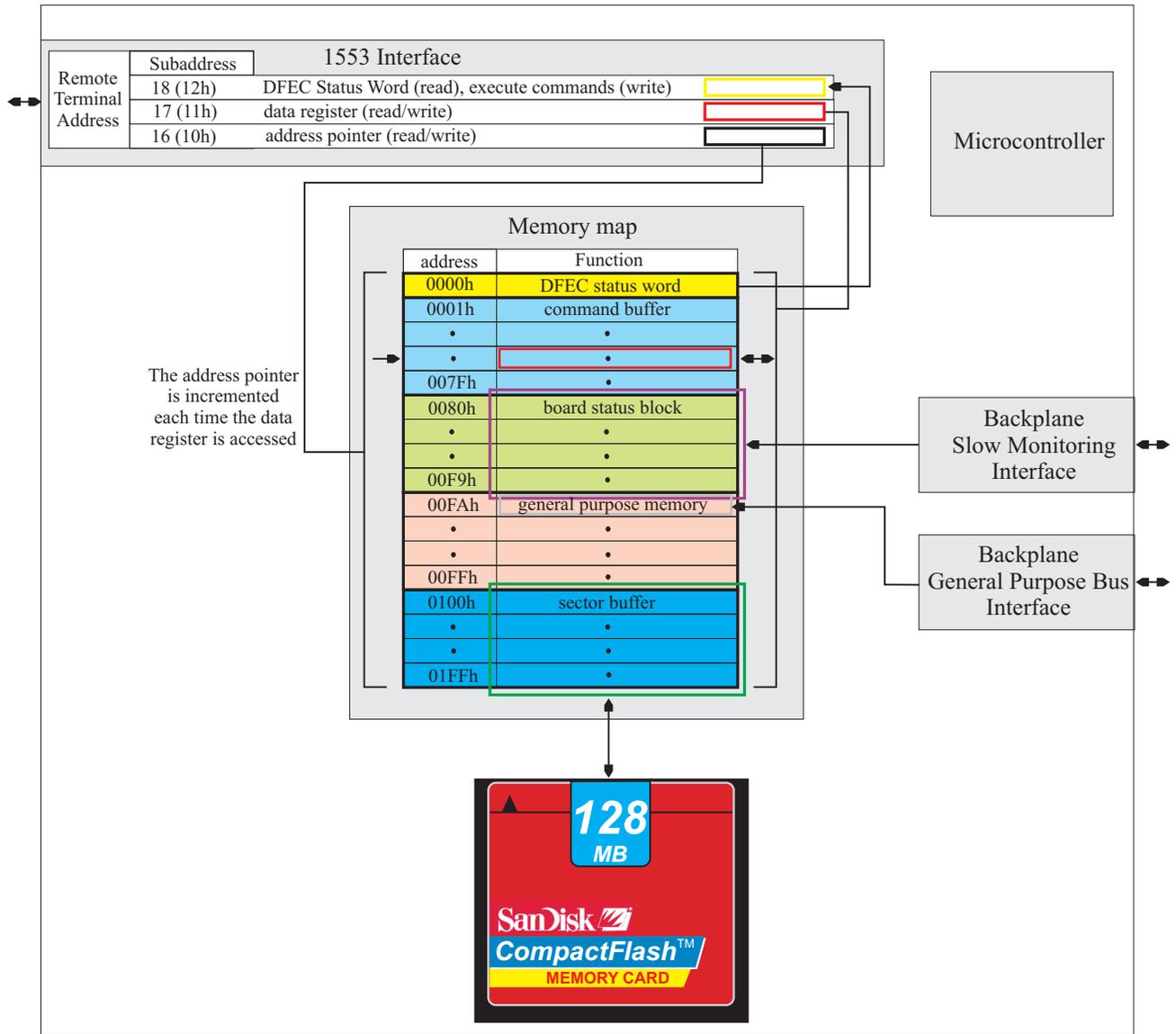


Figure 14.1, Subrack controller simplified block diagram

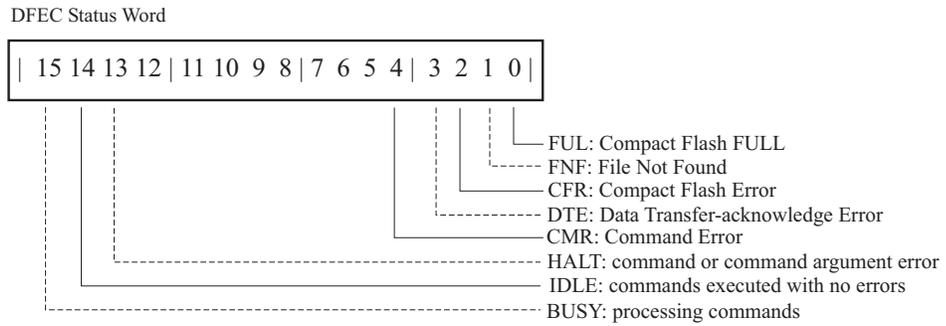


Figure 14.2, Subrack Controller (DFEC) Status Word.

14.2 CompactFlash™ card

The subrack controller uses a CompactFlash™ [Ref. 37] memory card to store the files needed for configuration of the mixer board FPGAs. The FPGA's configuration files are listed in Table 5.1. The memory card also stores up to ten files containing the sequence of commands to be executed by the subrack controller at power-up. Each command file can contain a maximum of 127 bytes, which match the length of the subrack controller command buffer.

The command files are numbered sequentially in the same order they will be executed; their filenames must be "autoexec.000" to "autoexec.009". The subrack controller will stop after executing "autoexec.009" or when the next command file in the sequence is not found.

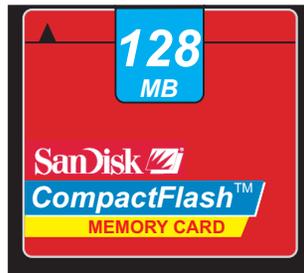


Figure 14.3, CompactFlash card.

14.2.1 General information about Compact Flash cards [Ref. 15]

CompactFlash™ is a small removable mass storage device. First introduced in 1994 by SanDisk Corporation [Ref. 37], CF™ cards weigh a half-ounce and are the size of a matchbook (43mm [1.7"] x 36mm [1.4"] x 3.3mm [0.13"]).

CompactFlash cards are designed with flash technology, a non-volatile storage solution that does not require a battery to retain data indefinitely. CompactFlash storage products are solid state, meaning they contain no moving parts.

Dual 3.3V & 5V Operation – CompactFlash cards support both 3.3V and 5V operation and can be interchanged between 3.3V and 5V systems.

Shock – CF cards have an operating shock rating of 2,000 Gs, which is equivalent to a 10-foot drop. With typical usage, a CF card can be used for more than 100 years with no loss or deterioration of data.

Data Reliability – CompactFlash data is protected by built-in dynamic defect management and error correction technologies.

The CompactFlash card can be read/written with the SanDisk ImageMate™ external flash card reader that connects to a computer through a USB port. Another option is the SanDisk PCMCIA card adapter.

14.2.2 Standard subrack controller commands (autoexec) files

The following two tables describe the content of the two standard "autoexec" or "command" binary files stored on the CompactFlash card to handle the mixer board FPGAs configuration at

power-up. The files have been written using a Hex editor [Ref. 43]. Beside the autoexec files the CompactFlash contains the mixer board FPGA's configuration files.

Refer to paragraph 14.3 for a list of the subrack controller commands. The complete description of subrack controller is in available [Ref. 5].

command (0x)	Notes
1200 8102	Write byte 0x00 to backplane, offset 0x81 (subrack broadcasting to relative address 0x01 Device Status/Control register), slot# 02. This command will write to all the Mixer Boards setting the device select pointer to device 0x00.
5300 4202 0200	Copy file to backplane, offset 0x42 (mixer board # broadcasting to relative address 0x02 Device Configuration Data register), slot# 02. This command will download to Mixer Boards in slot# 02, 06, 10, 14, 18 the Mixer1/device 00 configuration file "0200_PC.bin".
5300 4203 0300	Copy file to backplane, offset 0x42 (mixer board # broadcasting to relative address 0x02 Device Configuration Data register), slot# 03. This command will download to Mixer Boards in slot# 03, 07, 11, 15, 19 the Mixer2/device 00 configuration file "0300_PC.bin".
5300 4204 0400	Copy file to backplane, offset 0x42, slot# 04. This command will download to Mixer Boards in slot# 04, 08, 12, 16, 20 the Mixer3/device 00 configuration file "0400_PC.bin".
5300 4205 0500	Copy file to backplane, offset 0x42, slot# 05. This command will download to Mixer Boards in slot# 05, 09, 13, 17, 21 the Mixer4/device 00 configuration file "0400_PC.bin".
1201 8102	Write byte 0x01 to backplane, offset 0x81 (subrack broadcasting to relative address 0x01 Device Status/Control register), slot# 02. This command will write to all the Mixer Boards setting the device select pointer to device 0x01.
5300 4202 0201	Copy file to backplane, Mixer1/device 01 configuration file "0201_PC.bin".
5300 4203 0301	Copy file to backplane, Mixer2/device 01 configuration file "0301_PC.bin".
5300 4204 0401	Copy file to backplane, Mixer3/device 01 configuration file "0401_PC.bin".
5300 4205 0501	Copy file to backplane, Mixer4/device 01 configuration file "0501_PC.bin".
1202 8102	Write byte 0x02 to backplane. Sets the device select pointer to device 0x02 in all mixer boards.
5300 4202 0202	Copy file to backplane, Mixer1/device 02 configuration file "0202_PC.bin".
5300 4203 0302	Copy file to backplane, Mixer2/device 02 configuration file "0302_PC.bin".
5300 4204 0402	Copy file to backplane, Mixer3/device 02 configuration file "0402_PC.bin".
5300 4205 0502	Copy file to backplane, Mixer4/device 02 configuration file "0502_PC.bin".
1203 8102	Write byte 0x03 to backplane. Sets the device select pointer to device 0x03 in all mixer boards.
5300 4202 0203	Copy file to backplane, Mixer1/device 03 configuration file "0203_PC.bin".
5300 4203 0303	Copy file to backplane, Mixer2/device 03 configuration file "0303_PC.bin".
5300 4204 0403	Copy file to backplane, Mixer3/device 03 configuration file "0403_PC.bin".
5300 4205 0503	Copy file to backplane, Mixer4/device 03 configuration file "0503_PC.bin".
1204 8102	Write byte 0x04 to backplane. Sets the device select pointer to device 0x04 in all mixer boards.
5300 4202 0204	Copy file to backplane, Mixer1/device 04 configuration file "0204_PC.bin".
5300 4203 0304	Copy file to backplane, Mixer2/device 04 configuration file "0304_PC.bin".
5300 4204 0404	Copy file to backplane, Mixer3/device 04 configuration file "0404_PC.bin".
5300 4205 0504	Copy file to backplane, Mixer4/device 04 configuration file "0504_PC.bin".
1205 8102	Write byte 0x05 to backplane. Sets the device select pointer to device 0x05 in all mixer boards.

5300 4202 0205	Copy file to backplane, Mixer1/device 05 configuration file "0205_PC.bin".
5300 4203 0305	Copy file to backplane, Mixer2/device 05 configuration file "0305_PC.bin".
5300 4204 0405	Copy file to backplane, Mixer3/device 05 configuration file "0405_PC.bin".
5300 4205 0505	Copy file to backplane, Mixer4/device 05 configuration file "0505_PC.bin".
1206 8102	Write byte 0x06 to backplane. Sets the device select pointer to device 0x06 in all mixer boards.
5300 4202 0206	Copy file to backplane, Mixer1/device 06 configuration file "0206_PC.bin".
5300 4203 0306	Copy file to backplane, Mixer2/device 06 configuration file "0306_PC.bin".
5300 4204 0406	Copy file to backplane, Mixer3/device 06 configuration file "0406_PC.bin".
5300 4205 0506	Copy file to backplane, Mixer4/device 06 configuration file "0506_PC.bin".
1207 8102	Write byte 0x07 to backplane. Sets the device select pointer to device 0x07 in all mixer boards.
5300 4202 0207	Copy file to backplane, Mixer1/device 07 configuration file "0207_PC.bin".
5300 4203 0307	Copy file to backplane, Mixer2/device 07 configuration file "0307_PC.bin".
5300 4204 0407	Copy file to backplane, Mixer3/device 07 configuration file "0407_PC.bin".
5300 4205 0507	Copy file to backplane, Mixer4/device 07 configuration file "0507_PC.bin".
A100	End of list command. Stop the subrack controller execution of the commands in the command buffer and make him look for next autoexec file.

Table 14.1, content of file "autoexec.000".

command (0x)	Notes
1208 8102	Write byte 0x08 to backplane. Sets the device select pointer to device 0x08 in all mixer boards.
5300 4202 0208	Copy file to backplane, Mixer1/device 08 configuration file "0208_PC.bin".
5300 4203 0308	Copy file to backplane, Mixer2/device 08 configuration file "0308_PC.bin".
5300 4204 0408	Copy file to backplane, Mixer3/device 08 configuration file "0408_PC.bin".
5300 4205 0508	Copy file to backplane, Mixer4/device 08 configuration file "0508_PC.bin".
1209 8102	Write byte 0x09 to backplane. Sets the device select pointer to device 0x09 in all mixer boards.
5300 4202 0209	Copy file to backplane, Mixer1/device 09 configuration file "0209_PC.bin".
5300 4203 0309	Copy file to backplane, Mixer2/device 09 configuration file "0309_PC.bin".
5300 4204 0409	Copy file to backplane, Mixer3/device 09 configuration file "0409_PC.bin".
5300 4205 0509	Copy file to backplane, Mixer4/device 09 configuration file "0509_PC.bin".
120A 8102	Write byte 0x0A to backplane. Sets the device select pointer to device 0x0A in all mixer boards.
5300 4202 020A	Copy file to backplane, Mixer1/device 0A configuration file "020A_PC.bin".
5300 4203 030A	Copy file to backplane, Mixer2/device 0A configuration file "030A_PC.bin".
5300 4204 040A	Copy file to backplane, Mixer3/device 0A configuration file "040A_PC.bin".
5300 4205 050A	Copy file to backplane, Mixer4/device 0A configuration file "050A_PC.bin".
120B 8102	Write byte 0x0B to backplane. Sets the device select pointer to device 0x0B in all mixer boards.
5300 4202 020B	Copy file to backplane, Mixer1/device 0B configuration file "020B_PC.bin".
5300 4203 030B	Copy file to backplane, Mixer2/device 0B configuration file "030B_PC.bin".

5300 4204 040B	Copy file to backplane, Mixer3/device 0B configuration file "040B_PC.bin".
5300 4205 050B	Copy file to backplane, Mixer4/device 0B configuration file "050B_PC.bin".
120C 8102	Write byte 0x0C to backplane. Sets the device select pointer to device 0x0C in all mixer boards.
5300 4202 020C	Copy file to backplane, Mixer1/device 0C configuration file "020C_PC.bin".
5300 4203 030C	Copy file to backplane, Mixer2/device 0C configuration file "030C_PC.bin".
5300 4204 040C	Copy file to backplane, Mixer3/device 0C configuration file "040C_PC.bin".
5300 4205 050C	Copy file to backplane, Mixer4/device 0C configuration file "050C_PC.bin".
120D 8102	Write byte 0x0D to backplane. Sets the device select pointer to device 0x0D in all mixer boards.
5300 4202 020D	Copy file to backplane, Mixer1/device 0D configuration file "020D_PC.bin".
5300 4203 030D	Copy file to backplane, Mixer2/device 0D configuration file "030D_PC.bin".
5300 4204 040D	Copy file to backplane, Mixer3/device 0D configuration file "040D_PC.bin".
5300 4205 050D	Copy file to backplane, Mixer4/device 0D configuration file "050D_PC.bin".
120E 8102	Write byte 0x0E to backplane. Sets the device select pointer to device 0x0E in all mixer boards.
5300 4202 020E	Copy file to backplane, Mixer1/device 0E configuration file "020E_PC.bin".
5300 4203 030E	Copy file to backplane, Mixer2/device 0E configuration file "030E_PC.bin".
5300 4204 040E	Copy file to backplane, Mixer3/device 0E configuration file "040E_PC.bin".
5300 4205 050E	Copy file to backplane, Mixer4/device 0E configuration file "050E_PC.bin".
120F 8102	Write byte 0x0F to backplane. Sets the device select pointer to device 0x0F in all mixer boards.
5300 4202 020F	Copy file to backplane, Mixer1/device 0F configuration file "020F_PC.bin".
5300 4203 030F	Copy file to backplane, Mixer2/device 0F configuration file "030F_PC.bin".
5300 4204 040F	Copy file to backplane, Mixer3/device 0F configuration file "040F_PC.bin".
5300 4205 050F	Copy file to backplane, Mixer4/device 0F configuration file "050F_PC.bin".
A100	End of list command. Stop the subrack controller execution of the commands in the command buffer and make him look for next autoexec file.

Table 14.2, content of file "autoexec.001".

14.3 Subrack Controller Commands

The following tables provide the list of the subrack controller commands. For complete documentation refer to [Ref. 5].

Write Byte to Backplane															
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0x1				0x2				data byte							
offset												slot number			

Read Byte from Backplane															
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0x2				0x2											
offset												slot number			

CompactFlash to Sector Buffer															
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0x3				0x2				lba high byte							
lba mid byte								lba low byte							

SectorBuffer to CompactFlash															
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0x4				0x2				lba high byte							
lba mid byte								lba low byte							

Copy File to Backplane															
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0x5				0x3											
offset												slot number			
file name															

Delete File from CompactFlash															
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0x9				0x2											
file name															

Append Sector to File															
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0x8				0x2											
file name															

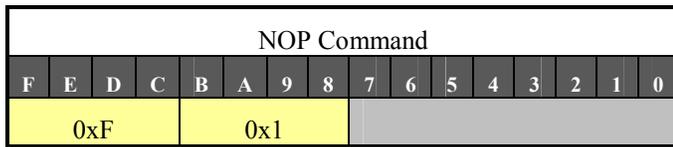
Generate File Checksum															
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0x7				0x2											
file name															

Reset Board															
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0x7				0x1								slot number			

Set Clock Bits															
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0xC				0x1						clk		slot number			

Configure Device															
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0x6				0x3								slot number			
				device #				firmware rev byte							
file name															

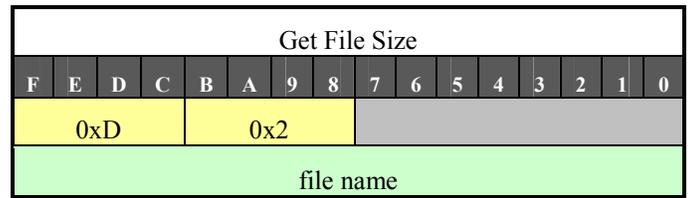
Get Firmware Revision															
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0xB				0x2								slot number			
				device #											



bit #

1stword

2ndword



bit #

1stword

14.3.1 Examples of command usage

command (0x)	Notes
1202 0015	Write 0x02 to the Board Status/Control register of mixer board in slot# 21 (0x15). This operation will force the board in the reset state. The FPGAs configuration will be retained.
1200 0015	Write 0x00 to the Board Status/Control register of mixer board in slot# 21 (0x15). The mixer board will be forced out of the reset state and resume normal operations.

Table 14.3, Example of mixer board reset operation.

command (0x)	Notes
1200 8B0C	Write 0x00 to the Monitoring Mode register of all mixer boards. This operation will change the LED monitoring mode to mode#0 (input links clock and DLL status).

Table 14.4, Example of change LED monitoring mode operation.

command (0x)	Notes
1217 2409	Write 0x17 to the Mode of Operation register (address 0x04) of the boards in the second mixer subsystem (slot# 6, 7, 8, 9). This operation enables the "Device Access Registers", allowing to access registers located on mixer board FPGAs.
120A 2109	Write 0x0A to the Device Status/Control register (address 0x01) of the boards in the second mixer subsystem (slot# 6, 7, 8, 9). This operation point the board controller to talk to device# 0A (IN0 FPGA)
12<reg> 2709	Write <reg> to the Device Access Address register (address 0x07) of the boards in the second mixer subsystem (slot# 6, 7, 8, 9). This operation point the board controller to talk to the specific register address <reg> inside the device specified in the previous operation. If the LED monitoring mode is set to mode 8 the front panel LEDs 0..7 will display the content of the local bus that is continuously driven by the content of the register <reg> of device #0A.
2200 0806	Readback the content of the Device Access Data register on the mixer board in slot #6. The byte read is the content of register <reg> inside device# 0A.
12<data_byte> 0806	Write <data_byte> to the Device Access Data register on the mixer board in slot #6. This operation will write the <data_byte> to the register <reg> of device #0A.

Table 14.5, Example of device access operations.

14.4 Test procedures information

A separate document provides **[Ref. 8c]** information on mixer board/system test procedures.

14.5 Diagnostic procedures information

A separate document provides **[Ref. 8d]** information and examples on mixer system diagnostic procedures.

15. Appendix I – CPS re-mapping conversion tables

The following 4 four tables provide the re-mapping information for the CPS data bits received by the mixer system. The original CPS data stream was sent to each mixer board over a 28 bit wide links (one of the 28 bits is used for frame synchronization). The new CPS data stream will be sent over a 21 bit wide data stream (one of the 21 bits used for frame synchronization). The original data stream had a total of 128 data bits per frame (seven clock cycles), the new one has only 64 data bits per frame.

Data bits marked as "X" (blue background color) are lost due to 28 to 21 bits re-mapping.

Data bits marked as "S" (gray background color) are still handled by the mixer but will not be used by the AFEs to send data and will be ignored by the DFEs.

Re-mapping of the CPS link data bits sent to Mixer 1							
old designation	new designation	old designation	new designation	old designation	new designation	old designation	new designation
CPSL1	CPS1	CPSL33	CPS33	CPSH1	CPS6	CPSH33	S
CPSL2	CPS2	CPSL34	CPS34	CPSH2	CPS7	CPSH34	CPS41
CPSL3	CPS3	CPSL35	CPS35	CPSH3	CPS8	CPSH35	S
CPSL4	CPS4	CPSL36	CPS36	CPSH4	CPS9	CPSH36	CPS43
CPSL5	S	CPSL37	CPS37	CPSH5	CPS10	CPSH37	S
CPSL6	CPS5	CPSL38	CPS38	CPSH6	S	CPSH38	CPS40
CPSL7	S	CPSL39	CPS39	CPSH7	S	CPSH39	CPS42
CPSL8	S	CPSL40	S	CPSH8	X	CPSH40	X
CPSL9	CPS11	CPSL41	X	CPSH9	X	CPSH41	CPS44
CPSL10	CPS12	CPSL42	X	CPSH10	X	CPSH42	CPS45
CPSL11	CPS13	CPSL43	X	CPSH11	X	CPSH43	CPS46
CPSL12	CPS14	CPSL44	X	CPSH12	X	CPSH44	CPS47
CPSL13	CPS15	CPSL45	X	CPSH13	X	CPSH45	CPS48
CPSL14	CPS16	CPSL46	X	CPSH14	X	CPSH46	CPS49
CPSL15	S	CPSL47	X	CPSH15	X	CPSH47	CPS50
CPSL16	S	CPSL48	X	CPSH16	S	CPSH48	S
CPSL17	CPS17	CPSL49	X	CPSH17	S	CPSH49	CPS51
CPSL18	S	CPSL50	X	CPSH18	CPS21	CPSH50	CPS52
CPSL19	CPS18	CPSL51	X	CPSH19	S	CPSH51	CPS53
CPSL20	CPS19	CPSL52	X	CPSH20	S	CPSH52	S
CPSL21	S	CPSL53	X	CPSH21	CPS22	CPSH53	S
CPSL22	CPS20	CPSL54	X	CPSH22	S	CPSH54	CPS54
CPSL23	X	CPSL55	S	CPSH23	S	CPSH55	S
CPSL24	X	CPSL56	S	CPSH24	S	CPSH56	S
CPSL25	CPS23	CPSL57	CPS55	CPSH25	S	CPSH57	CPS62
CPSL26	CPS24	CPSL58	CPS56	CPSH26	S	CPSH58	CPS63
CPSL27	CPS25	CPSL59	CPS57	CPSH27	S	CPSH59	S
CPSL28	CPS26	CPSL60	CPS58	CPSH28	S	CPSH60	CPS64
CPSL29	CPS27	CPSL61	CPS59	CPSH29	CPS30	CPSH61	S
CPSL30	CPS28	CPSL62	CPS60	CPSH30	CPS31	CPSH62	X
CPSL31	CPS29	CPSL63	CPS61	CPSH31	CPS32	CPSH63	X
CPSL32	S	CPSL64	S	CPSH32	S	CPSH64	X

Table 15.1, Mixer 1 CPS data bits re-mapping.

Re-mapping of the CPS link data bits sent to Mixer 2							
old designation	new designation	old designation	new designation	old designation	new designation	old designation	new designation
CPSL65	CPS65	CPSL97	CPS97	CPSH65	CPS70	CPSH97	S
CPSL66	CPS66	CPSL98	CPS98	CPSH66	CPS71	CPSH98	CPS105
CPSL67	CPS67	CPSL99	CPS99	CPSH67	CPS72	CPSH99	S
CPSL68	CPS68	CPSL100	CPS100	CPSH68	CPS73	CPSH100	CPS107
CPSL69	S	CPSL101	CPS101	CPSH69	CPS74	CPSH101	S
CPSL70	CPS69	CPSL102	CPS102	CPSH70	S	CPSH102	CPS104
CPSL71	S	CPSL103	CPS103	CPSH71	S	CPSH103	CPS106
CPSL72	S	CPSL104	S	CPSH72	X	CPSH104	X
CPSL73	CPS75	CPSL105	X	CPSH73	X	CPSH105	CPS108
CPSL74	CPS76	CPSL106	X	CPSH74	X	CPSH106	CPS109
CPSL75	CPS77	CPSL107	X	CPSH75	X	CPSH107	CPS110
CPSL76	CPS78	CPSL108	X	CPSH76	X	CPSH108	CPS111
CPSL77	CPS79	CPSL109	X	CPSH77	X	CPSH109	CPS112
CPSL78	CPS80	CPSL110	X	CPSH78	X	CPSH110	CPS113
CPSL79	S	CPSL111	X	CPSH79	X	CPSH111	CPS114
CPSL80	S	CPSL112	X	CPSH80	S	CPSH112	S
CPSL81	CPS81	CPSL113	X	CPSH81	CPS85	CPSH113	CPS115
CPSL82	S	CPSL114	X	CPSH82	S	CPSH114	S
CPSL83	CPS82	CPSL115	X	CPSH83	S	CPSH115	CPS116
CPSL84	CPS83	CPSL116	X	CPSH84	S	CPSH116	CPS117
CPSL85	S	CPSL117	X	CPSH85	CPS86	CPSH117	S
CPSL86	CPS84	CPSL118	X	CPSH86	S	CPSH118	CPS118
CPSL87	X	CPSL119	S	CPSH87	S	CPSH119	S
CPSL88	X	CPSL120	S	CPSH88	S	CPSH120	S
CPSL89	CPS87	CPSL121	CPS119	CPSH89	S	CPSH121	CPS126
CPSL90	CPS88	CPSL122	CPS120	CPSH90	S	CPSH122	S
CPSL91	CPS89	CPSL123	CPS121	CPSH91	S	CPSH123	CPS127
CPSL92	CPS90	CPSL124	CPS122	CPSH92	S	CPSH124	CPS128
CPSL93	CPS91	CPSL125	CPS123	CPSH93	CPS94	CPSH125	S
CPSL94	CPS92	CPSL126	CPS124	CPSH94	CPS95	CPSH126	X
CPSL95	CPS93	CPSL127	CPS125	CPSH95	CPS96	CPSH127	X
CPSL96	S	CPSL128	S	CPSH96	S	CPSH128	X

Table 15.2, Mixer 2 CPS data bits re-mapping.

Re-mapping of the CPS link data bits sent to Mixer 3							
old designation	new designation	old designation	new designation	old designation	new designation	old designation	new designation
CPSL129	CPS129	CPSL161	CPS161	CPSH129	CPS134	CPSH161	S
CPSL130	CPS130	CPSL162	CPS162	CPSH130	CPS135	CPSH162	CPS169
CPSL131	CPS131	CPSL163	CPS163	CPSH131	CPS136	CPSH163	S
CPSL132	CPS132	CPSL164	CPS164	CPSH132	CPS137	CPSH164	CPS171
CPSL133	S	CPSL165	CPS165	CPSH133	CPS138	CPSH165	S
CPSL134	CPS133	CPSL166	CPS166	CPSH134	S	CPSH166	CPS168
CPSL135	S	CPSL167	CPS167	CPSH135	S	CPSH167	CPS170
CPSL136	S	CPSL168	S	CPSH136	X	CPSH168	X
CPSL137	CPS139	CPSL169	X	CPSH137	X	CPSH169	CPS172
CPSL138	CPS140	CPSL170	X	CPSH138	X	CPSH170	CPS173
CPSL139	CPS141	CPSL171	X	CPSH139	X	CPSH171	CPS174
CPSL140	CPS142	CPSL172	X	CPSH140	X	CPSH172	CPS175
CPSL141	CPS143	CPSL173	X	CPSH141	X	CPSH173	CPS176
CPSL142	CPS144	CPSL174	X	CPSH142	X	CPSH174	CPS177
CPSL143	S	CPSL175	X	CPSH143	X	CPSH175	CPS178
CPSL144	S	CPSL176	X	CPSH144	S	CPSH176	S
CPSL145	CPS145	CPSL177	X	CPSH145	S	CPSH177	CPS179
CPSL146	S	CPSL178	X	CPSH146	CPS149	CPSH178	S
CPSL147	S	CPSL179	X	CPSH147	S	CPSH179	CPS180
CPSL148	CPS146	CPSL180	X	CPSH148	S	CPSH180	CPS181
CPSL149	CPS147	CPSL181	X	CPSH149	CPS150	CPSH181	S
CPSL150	CPS148	CPSL182	X	CPSH150	S	CPSH182	CPS182
CPSL151	X	CPSL183	S	CPSH151	S	CPSH183	S
CPSL152	X	CPSL184	S	CPSH152	S	CPSH184	S
CPSL153	CPS151	CPSL185	CPS183	CPSH153	S	CPSH185	CPS190
CPSL154	CPS152	CPSL186	CPS184	CPSH154	S	CPSH186	S
CPSL155	CPS153	CPSL187	CPS185	CPSH155	S	CPSH187	CPS191
CPSL156	CPS154	CPSL188	CPS186	CPSH156	S	CPSH188	S
CPSL157	CPS155	CPSL189	CPS187	CPSH157	CPS158	CPSH189	CPS192
CPSL158	CPS156	CPSL190	CPS188	CPSH158	CPS159	CPSH190	X
CPSL159	CPS157	CPSL191	CPS189	CPSH159	CPS160	CPSH191	X
CPSL160	S	CPSL192	S	CPSH160	S	CPSH192	X

Table 15.3, Mixer 3 CPS data bits re-mapping.

Re-mapping of the CPS link data bits sent to Mixer 4							
old designation	new designation	old designation	new designation	old designation	new designation	old designation	new designation
CPSL193	CPS193	CPSL225	CPS225	CPSH193	CPS198	CPSH225	S
CPSL194	CPS194	CPSL226	CPS226	CPSH194	CPS199	CPSH226	CPS233
CPSL195	CPS195	CPSL227	CPS227	CPSH195	CPS200	CPSH227	S
CPSL196	CPS196	CPSL228	CPS228	CPSH196	CPS201	CPSH228	CPS235
CPSL197	CPS197	CPSL229	CPS229	CPSH197	CPS202	CPSH229	S
CPSL198	S	CPSL230	CPS230	CPSH198	S	CPSH230	CPS232
CPSL199	S	CPSL231	CPS231	CPSH199	S	CPSH231	CPS234
CPSL200	S	CPSL232	S	CPSH200	X	CPSH232	X
CPSL201	CPS203	CPSL233	X	CPSH201	X	CPSH233	CPS236
CPSL202	CPS204	CPSL234	X	CPSH202	X	CPSH234	CPS237
CPSL203	CPS205	CPSL235	X	CPSH203	X	CPSH235	CPS238
CPSL204	CPS206	CPSL236	X	CPSH204	X	CPSH236	CPS239
CPSL205	CPS207	CPSL237	X	CPSH205	X	CPSH237	CPS240
CPSL206	CPS208	CPSL238	X	CPSH206	X	CPSH238	CPS241
CPSL207	S	CPSL239	X	CPSH207	X	CPSH239	CPS242
CPSL208	S	CPSL240	X	CPSH208	S	CPSH240	S
CPSL209	CPS209	CPSL241	X	CPSH209	S	CPSH241	CPS243
CPSL210	S	CPSL242	X	CPSH210	CPS213	CPSH242	S
CPSL211	CPS210	CPSL243	X	CPSH211	S	CPSH243	CPS244
CPSL212	CPS211	CPSL244	X	CPSH212	S	CPSH244	CPS245
CPSL213	S	CPSL245	X	CPSH213	CPS214	CPSH245	S
CPSL214	CPS212	CPSL246	X	CPSH214	S	CPSH246	CPS246
CPSL215	X	CPSL247	S	CPSH215	S	CPSH247	S
CPSL216	X	CPSL248	S	CPSH216	S	CPSH248	S
CPSL217	CPS215	CPSL249	CPS247	CPSH217	S	CPSH249	CPS254
CPSL218	CPS216	CPSL250	CPS248	CPSH218	S	CPSH250	S
CPSL219	CPS217	CPSL251	CPS249	CPSH219	S	CPSH251	CPS255
CPSL220	CPS218	CPSL252	CPS250	CPSH220	S	CPSH252	S
CPSL221	CPS219	CPSL253	CPS251	CPSH221	CPS222	CPSH253	CPS256
CPSL222	CPS220	CPSL254	CPS252	CPSH222	CPS223	CPSH254	X
CPSL223	CPS221	CPSL255	CPS253	CPSH223	CPS224	CPSH255	X
CPSL224	S	CPSL256	S	CPSH224	S	CPSH256	X

Table 15.4, Mixer 4 CPS data bits re-mapping.

16. Appendix L - Notes about Input Links swapping

The 20 data bits of each LVDS input Link (excluding the SYNC bit) can be divided in two sets of ten bits, the 10 Least Significant bits and the 10 Most Significant bits. The two sets of bits may have to be swapped (i.e. exchange their position) before any operation of data multiplexing is performed in the backend (backplane FPGAs and backend FPGAs). This swapping depends on the particular link considered and the Mixer Board position inside a supersector (i.e. MB1, 2, 3 or 4). This feature was used to simplify the hardware design and reduce the number of required connections on the Mixer Board. Furthermore it allowed the use of just one hardware design for the 4 different firmware codes used (for Mixer#1, 2, 3, 4).

There is another reason for link swapping. The AFE LHBs (Left Hand Boards) have the top and bottom ten bits of the link swapped from what was the original specification. The link swapping is used to correct this problem. The link swapping is then completely defined by the system of which the mixer system is part of (D0 Central Tracker Trigger). The swapping information embedded in the mixer system firmware is reported in Table 16.1.

Mixer Board#		Link swapping top eight input links		Link swapping bottom eight input links	
		Binary content	Swapped links	Binary content	Swapped links
1	Mixer swap only (a)	11110100	15, 14, 13, 12, 10	11010000	7, 6, 4
	AFE LHB swap only (b)	10011110	15, 12, 11, 10, 9	10000110	7, 2, 1
	both Mixer and AFE swaps = (a) XOR (b)	01101010 (0x6A)	14, 13, 11, 9	01010110 (0x56)	6, 4, 2, 1
2	Mixer swap only (a)	10000010	15, 9	11100010	7, 6, 5, 1
	AFE LHB swap only (b)	10000111	15, 10, 9, 8	01100100	6, 5, 2
	both Mixer and AFE swaps = (a) XOR (b)	00000101 (0x05)	10, 8	10000110 (0x86)	7, 2, 1
3	Mixer swap only (a)	00100000	13	11110000	7, 6, 5, 4
	AFE LHB swap only (b)	10110011	15, 13, 12, 9, 8	01010100	6, 4, 2
	both Mixer and AFE swaps = (a) XOR (b)	10010011 (0x93)	15, 12, 9, 8	10100100 (0xA4)	7, 5, 2
4	Mixer swap only (a)	00000010	9	11010010	7, 6, 4, 1
	AFE LHB swap only (b)	11010010	15, 14, 12, 9	10010100	7, 4, 2
	both Mixer and AFE swaps = (a) XOR (b)	11010000 (0xD0)	15, 14, 12	01000110 (0x46)	6, 2, 1

Table 16.1, Link swapping information.

17. Glossary

AFE: acronym for Analog Front-End Board.

Analog Front-End Board (AFE): It has the function of receiving charge signals from the Central Fiber Tracker (CFT) and providing digital hit pattern for those charge signals. The AFEs are located on the VLPC cassette cryostat. More details in Chapter 3 and [Ref. 7].

ANSI: American National Standards Institute. More information is available on the Internet: <http://www.ansi.org/>

BIST: Built-In Self Test, the method of designing circuits with additional logic that can be used to test correct operation of the primary (functional) logic.

BSDL: Boundary Scan Description Language. IEEE 1149.1-1993b defines a language that describes IEEE 1149.1 architecture for an integrated circuit. This language is known as the Boundary Scan Description Language (BSDL). Updated BSDL files for the XILINX devices used on the Mixer Board can be found at: http://support.xilinx.com/support/sw_bsd.htm

Compact Flash card: is a removable mass storage device. The card is designed based on the PC Card (PCMCIA) standard [Ref. 37].

CFT: Central Fiber Tracker.

CPS: Central Pre-Shower.

DFE: Digital Front-End board.

Digital Front-End Board: it has the function of generating the trigger using the data received from the mixer system. More details in Chapter 3 and [Ref. 5].

EDIF: Electronic Data Interchange Format. Industry-standard for specifying a logic design in text (ASCII) form.

EIA: Electronics Industries Alliance. More information is available on the Internet: <http://www.eia.org/>

File types:

JEDEC files

JEDEC files are CPLD programming files generated by the CPLD fitter. They are ASCII text files containing programming information and, optionally, functional test vectors that can be used to verify the correct functional behavior of the programmed device. One JEDEC file is required for each device in the JTAG programming chain. The extension for JEDEC files is .jed.

BSDL Summary files

The Boundary-Scan Description Language (BSDL) files use a subset of VHDL to describe the boundary scan features of a device. The Xilinx JTAG Programmer automatically extracts the length of the instruction register from the BSDL file to place non-Xilinx devices in bypass mode. Xilinx BSDL files are located automatically by the JTAG Programmer. The name of the BSDL file is assumed to be <device name>.bsd.

BIT Files

Bit files are Xilinx FPGA configuration files generated by the Xilinx FPGA design software. They are proprietary format binary files containing configuration information. One BIT file is required for each Xilinx FPGA in the JTAG boundary-scan chain. The extension for BIT files is ".bit".

(MCS/EXO) PROM Files

PROM programming files are generated by the Xilinx PROM file formatter. They are ascii text files used to specify configuration data. One PROM file is required for each Xilinx PROM in the JTAG boundary-scan chain. Use the device properties (Edit>Properties) dialog to specify the location of the MCS/EXO files for each Xilinx PROM. The required extensions for MCS and EXO files are ".mcs" and ".exo" respectively.

FPGA: Field Programmable Gate Array. An integrated circuit that contains configurable (programmable) logic blocks and configurable (programmable) interconnect between these blocks.

IEEE: Institute of Electrical and Electronics Engineers, Inc. More information is available on the Internet:
<http://www.ieee.org/>

Jedec: The JEDEC Solid State Technology Association (once known as the Joint Electron Device Engineering Council), is the semiconductor engineering standardization body of the Electronic Industries Alliance (EIA), a trade association that represents all areas of the electronics industry. More information is available on the Internet:
<http://www.jedec.org/>

Jitter: The JEDEC Standard No. 65 (EIA/JESD65) defines jitter as the magnitude of the time deviation of a controlled edge from its nominal position.

JTAG: Joint Test Action Group. Older name for IEEE 1149.1 boundary scan, a method to test printed circuit boards and also integrated circuits. See also BSDL.

Design complexity, difficulty of loaded board testing, and the limited pin access of surface mount technology led industry leaders to seek accord on a standard to support the solution of these problems.

The standard defines a hardware architecture and the mechanisms for its use.

The standard itself defines instructions that can be used to perform functional and interconnect tests as well as built-in self test procedures. Vendor-specific extensions to the standard have been developed to allow execution of maintenance and diagnostic applications as well as programming algorithms for re-configurable parts.

The top level schematic of the test logic defined by IEEE Std 1149.1 includes three key blocks:

The TAP Controller

This responds to the control sequences supplied through the test access port (TAP) and generates the clock and control signals required for correct operation of the other circuit blocks.

The Instruction Register

This shift register-based circuit is serially loaded with the instruction that selects an operation to be performed.

The Data Registers

These are a bank of shift register based circuits. The stimuli required by an operation are serially loaded into the data registers selected by the current instruction. Following execution of the operation, results can be shifted out for examination.

The *JTAG Test Access Port* (TAP) contains four pins that drive the circuit blocks and control the operations specified. The TAP facilitates the serial loading and unloading of instructions and data. The four pins of the TAP are: TMS (Test Mode Select), TCK (Test Clock), TDI (Test Data In) and TDO (Test Data Out). The function of each TAP pin is as follows:

TCK - this pin is the JTAG test clock. It sequences the TAP controller as well as all of the JTAG registers.

TMS - this pin is the mode input signal to the TAP Controller. The TAP controller is a FSM that provides the control logic for JTAG. The state of TMS at the rising edge of TCK determines the sequence of states for the TAP controller. TMS has an internal pull-up resistor on it to provide a logic 1 to the system if the pin is not driven.

TDI - this pin is the serial data input to all JTAG instruction and data registers. The state of the TAP controller as well as the particular instruction held in the instruction register determines which register is fed by TDI for a specific operation. TDI has an internal pull-up resistor on it to provide a logic 1 to the system if the pin is not driven. TDI is sampled into the JTAG registers on the rising edge of TCK.

TDO - this pin is the serial data output for all JTAG instruction and data registers. The state of the TAP controller as well as the particular instruction held in the instruction register determines which register feeds TDO for a specific operation. Only one register (instruction or data) is allowed to be the active connection between TDI and TDO for any given operation. TDO changes state on the falling edge of TCK and is only active during the shifting of data through the device. This pin is three-stated at all other times.

LVDS: Low Voltage Differential Signaling, otherwise known as TIA/EIA-644. Is a signaling method used for high-speed, low-power transmission of binary data over copper [Ref. 38].

LVTTTL: Low Voltage TTL. Is one of the several switching standards used in digital electronics [Ref. 38].

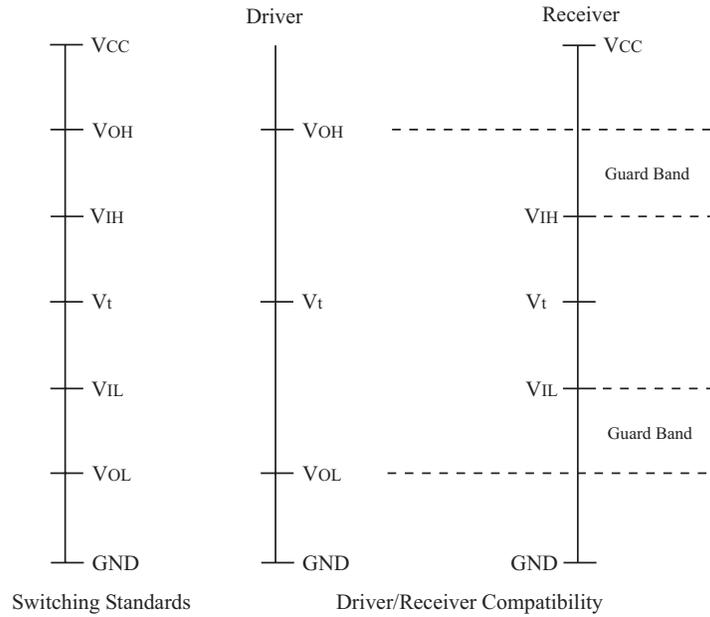


Figure 17.1, Switching standards.

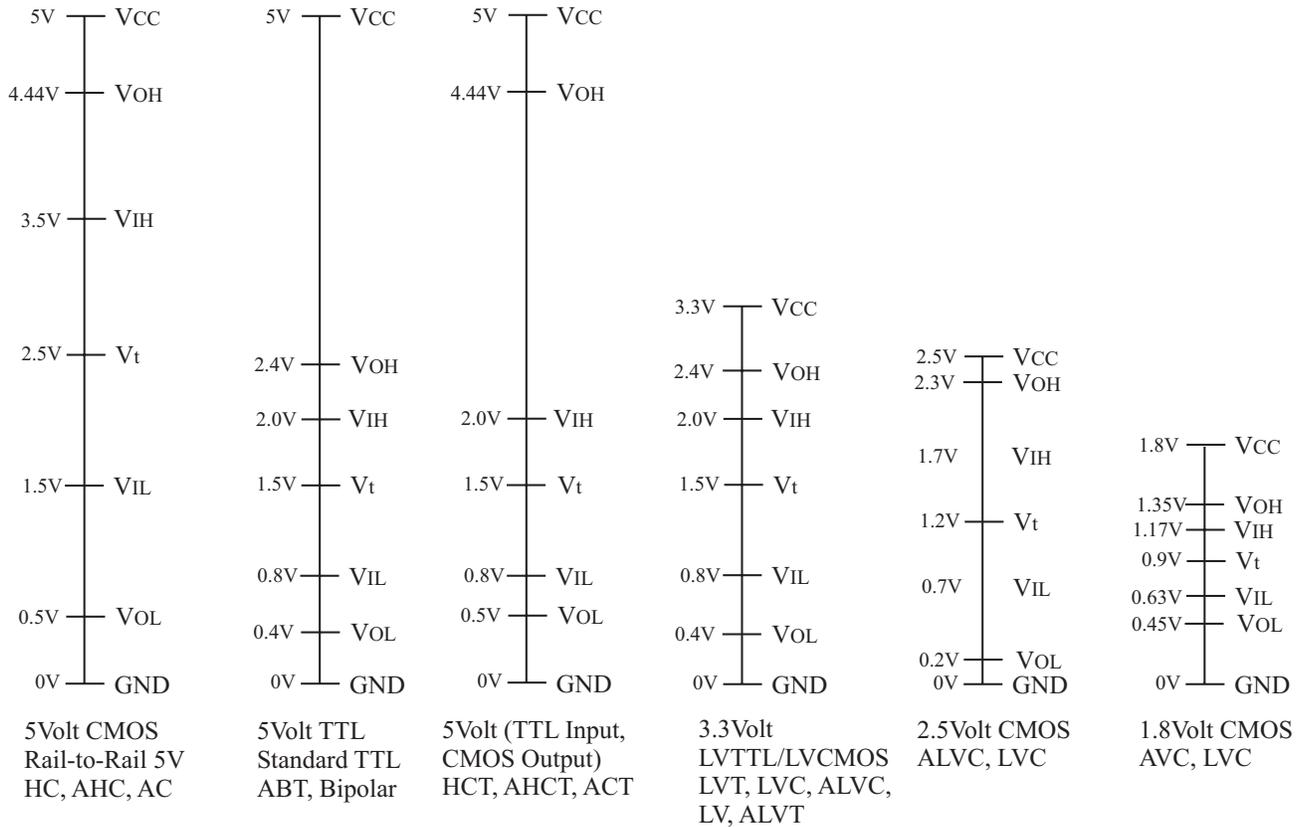


Figure 17.2, Comparison of switching standards.

MCU: Micro-Controller Unit.

MIL-STD-1553: standard developed to define a serial communications bus to interconnect different subsystems which need to share or exchange information.

SERDES: Serializer/Deserializer. Used to indicate LVDS components using data serialization (also called Data Channel Compression) to reduce the number of physical connection required for a data channel.

Skew: The JEDEC Standard No. 65 (EIA/JESD65) defines skew as The magnitude of the time difference between two events that ideally would occur simultaneously.

VHDL: "V" stands for Very High Speed Integrated Circuit and "HDL" stands for Hardware Description Language.

18. References

- [1] Paul Horowitz, Winfield Hill, "The Art of Electronics", 1995, Cambridge University Press. ISBN 0-521-37095-7.
- [2] Howard Johnson, Martin Graham, "High Speed Digital Design", 1993, Prentice Hall PTR. ISBN 0-13-395724-1.
- [3] Wade D. Peterson, VMEbus International Trade Association, "The VMEbus Handbook", Fourth edition 1997. ISBN 1-885731-08-6.
- [4] Design Specification Master Document for the Electronic Mixing Box System, D0 Electronics Group.
Information available on Internet:
http://d0server1.fnal.gov/Projects/TriggerElectronics/WebDocs/MixerBox/doc_indx.html
- [5] Jamieson T. Olsen,
b) "Digital Front End Mother Board register map", Engineering Note 2000-01-28a.
c) "DFE and Mixer Board Registers ", Engineering Note 2000-01-28a.
d) "DFE backplane address/data bus protocol", Engineering Note 2000-03-28a.
e) "DFE slow monitoring custom serial bus specification", Engineering Note 2000-01-31a.
f) Digital Front End Controller (DFEc) Board:
<http://d0server1.fnal.gov/users/jamieson/www/projects/dfec/index.html>
Information available on the internet:
<http://d0server1.fnal.gov/users/jamieson/www/index.html>
- [6] Robert D. Angstad, technical documentation.
Information available on the internet:
<http://d0server1.fnal.gov/users/angstadt/www/datapump/datapump.htm>
- [7] John T. Anderson,
a) "D-Zero Central Fiber Tracker 8-MCM Analog Front End Board, Design Specification", January 7, 2000.
Information available on Internet:
http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/default.html.
- [8] Mixer System documentation
a) Neal Wilcer, John Anderson, Stefano Rapisarda "Central Tracker Trigger (CTT) Mixer System Backplane Description & Power Distribution Specification", July 4, 2000. Document#: ESE-D0-000704.
b) Makoto Tomoto, "Note on cable mapping from AFE to Mixer", October 26, 2001.
c) D0 Mixer System Test Procedures.
d) D0 Mixer System Diagnostic Procedures.
The mentioned documents and several others are available on Internet:
http://www-ese.fnal.gov/D0_CTT_Mixer/
- [9] Private communication from undisclosed source.

- [10] Private communication from John Smith.
- [11] Agilent (formerly Hewlett-Packard) documentation:
- a) Probing Solutions for Agilent Technologies Logic Analysis Systems.
Information available on Internet:
<http://www.agilent.com/>
- [12] Aldec. Web site: <http://www.aldec.com/>.
- [13] Amp. Web site: <http://www.amp.com/>.
- [14] Brookdale Electronics. Web site: <http://www.brookdale.com/> .
- [15] Compact Flash Association. Web site: <http://www.compactflash.org/>
- [16] Corel Draw is a drawing software package by Corel. Web site: <http://www.corel.com>
- [17] Corelis Web site: <http://www.corelis.com>
- [18] Cypress. Web site: <http://www.cypress.com>
- [19] C&K. It has been acquired by ITT Industries, Cannon connectors division.
Web site: <http://www.ittcannon.com/>
- [20] Elmec Technology. Web site: <http://www.elmectech.com/>
- [21] ERNI. Web site: <http://www.erni.com/>
- [22] Fairchild. Web site: <http://www.fairchildsemi.com/>
- [23] FPGA Express is an FPGA synthesis software tool by Synopsys. Web site:
<http://www.synopsys.com/>
- [24] Harting. Web site: <http://www.harting.com/>
- [25] Hyperlynx is a signal integrity software package by Innoveda. Web site:
<http://www.innoveda.com/>
- [26] I-Cube. Web site: <http://www.icube.com/>
- [27] IDT. Web site: <http://www.idt.com/>
- [28] Leonardo Spectrum is an FPGA synthesis software tool by Mentor Graphics. Web site:
<http://www.mentor.com/>
- [29] Linear Technology. Web site: <http://www.linear-tech.com/>
- [30] Littlefuse. Web site: <http://www.littlefuse.com/>
- [31] Lumex. Web site: <http://www.lumex.com/>
- [32] Micrel. Web site: <http://www.micrel.com/> .
- [33] Motorola (semiconductors division). Web site: <http://e-www.motorola.com/>
- [34] National Semiconductors. Web site: <http://www.national.com/>
- [35] ON Semiconductor. Web site: <http://www.onsemi.com/>
- [36] Philips. Web site: <http://www.philips.com/>

[37] SanDisk documentation. Information available on Internet:

<http://www.sandisk.com/>

[38] Texas Instrument documentation:

- g) Interface Circuits for TIA/EIA-644(LVDS), November 1998, document SLLA038.
- h) SN65LVDS93 LVDS SERDES Transmitter, data sheet document SLLS302F.
- i) SN65LVDS94 LVDS SERDES Receiver, data sheet document SLLS298E.
- j) SN65LVDS95 LVDS SERDES Transmitter, data sheet document SLLS297F.
- k) SN65LVDS96 LVDS SERDES Receiver, data sheet document SLLS296F.
- l) Comparing Bus Solutions, March 2000, application report document SLLA067.

Information available on Internet: <http://www.ti.com/>

[39] Vicor. Web site: <http://www.vicr.com/>

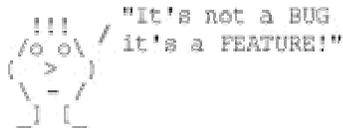
[40] Xilinx documentation:

- a) Spartan and Spartan-XL Families Field Programmable Gate Arrays, Product Specification, DS060 (v1.5) March 2, 2000 (Data Sheet file: ds060.pdf).
- b) Data Generation and Configuration for Spartan Spartan Series FPGAs, Application Note by Ashok Chotai, XAPP 126 June 14 1999 (version 1.1) (Application Note file: xapp126.pdf).
- c) XC18V00 Series of In-System Programmable Configuration PROMs, Product Specification, DS026 (v2.3) July 5, 2000 (Data Sheet file: ds026.pdf).
- d) Virtex 2.5V Field Programmable Gate Arrays, Final Product Specification, DS003 (v.2.2) May 23, 2000 (Data Sheet file: ds003.pdf).
- e) Virtex Configuration and ReadBack, Application Note by Carl Carmichael, XAPP 138 March 21, 1999 (Version 1.0) (Application Note file: xapp138.pdf).

Information available on Internet:

<http://www.xilinx.com/>

[41] Feedback is very welcome.



[42] MIL-STD-1553 is a military standard that defines the electrical and protocol characteristics for a data bus. Information on the 1553 standard is available on the internet from several sources, one of them is: <http://www.1553-mil-std.com/>

[43] Hex Workshop is a Hex editor software package by BreakPoint Software. Web site: <http://www.bpssoft.com/>