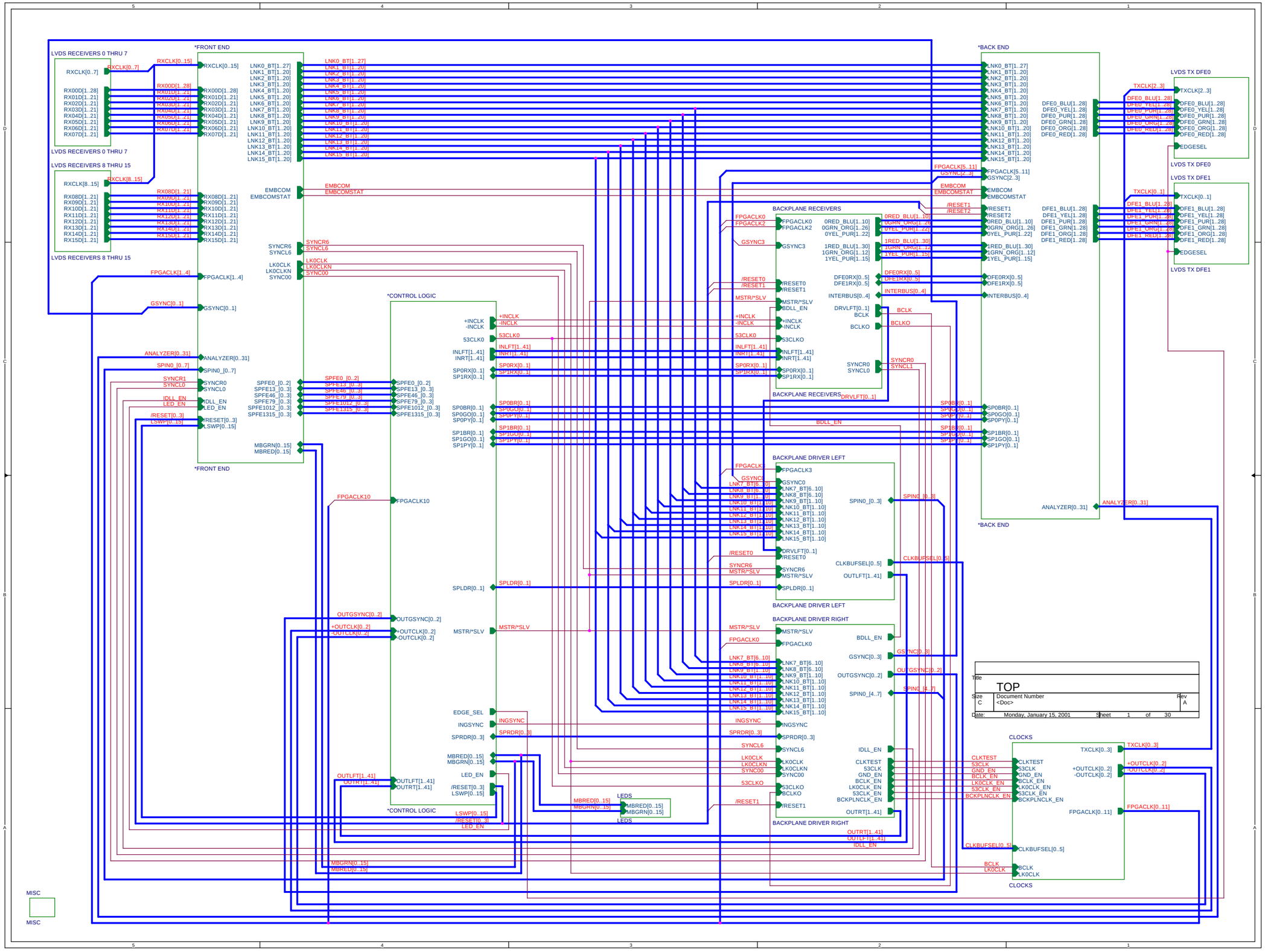
Fermi National Accelerator Laboratory

D-Zero Detector Central Fiber Tracker (CFT)
Axial Project Readout Electronics

Schematics for the Prototype Mixer Board

S. Marco Rapisarda, N. George Wilcer

April 5, 2002
Document # ESE-D0-040502


LVDS RECEIVERS 0 THRU 7
LVDS RECEIVERS 8 THRU 15
*FRONT END
*CONTROL LOGIC
*BACK END
BACKPLANE RECEIVERS
BACKPLANE DRIVER LEFT
BACKPLANE DRIVER RIGHT
LVDS TX DFE0
LVDS TX DFE1
CLOCKS
MISC
Title
TOP
Size
C
Document Number
<Doc>
Rev
A
Date:
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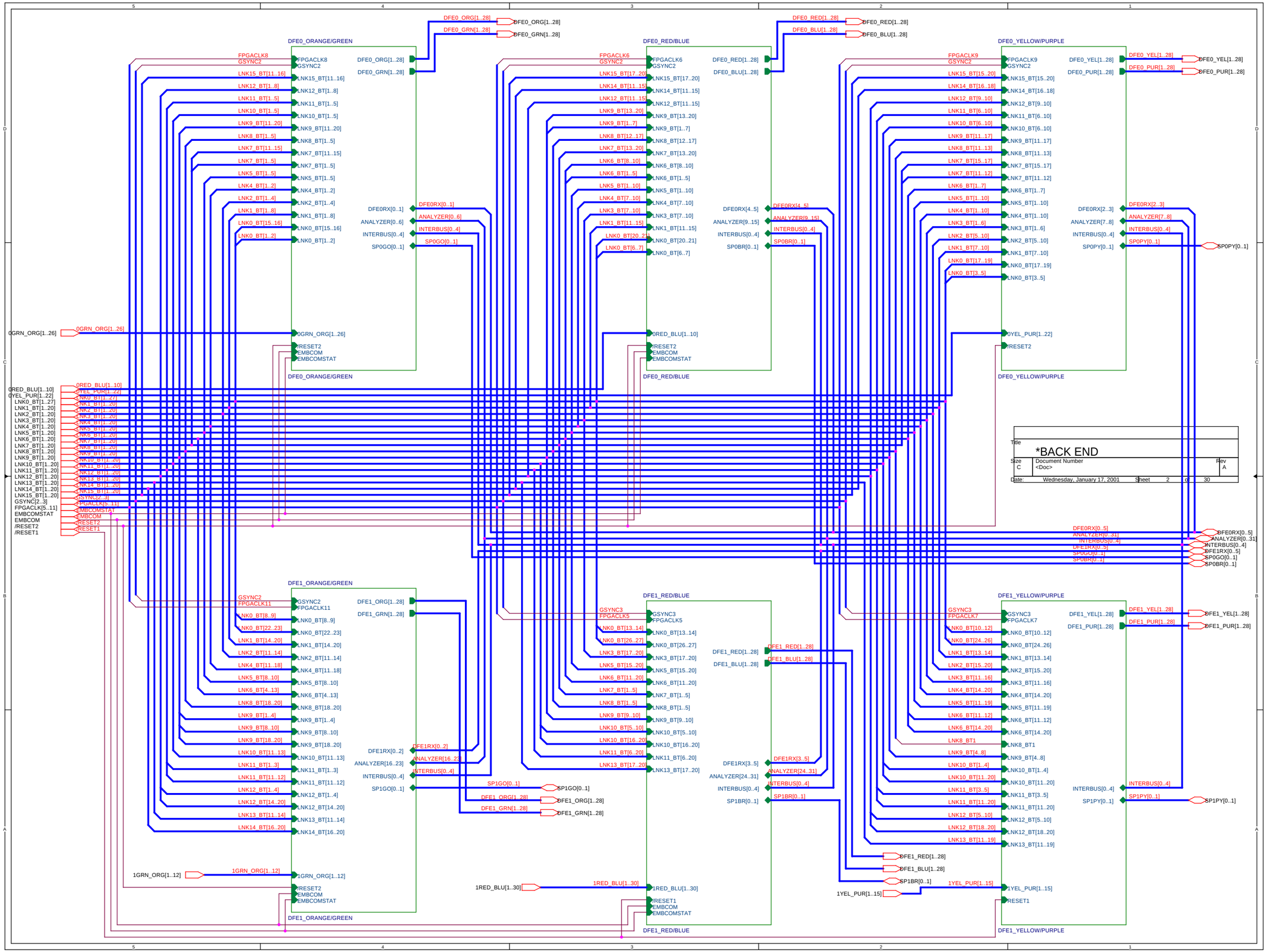
1
of
30


DFE0_ORANGE/GREEN
DFE0_RED/BLUE
DFE0_YELLOW/PURPLE
DFE1_ORANGE/GREEN
DFE1_RED/BLUE
DFE1_YELLOW/PURPLE
*BACK END
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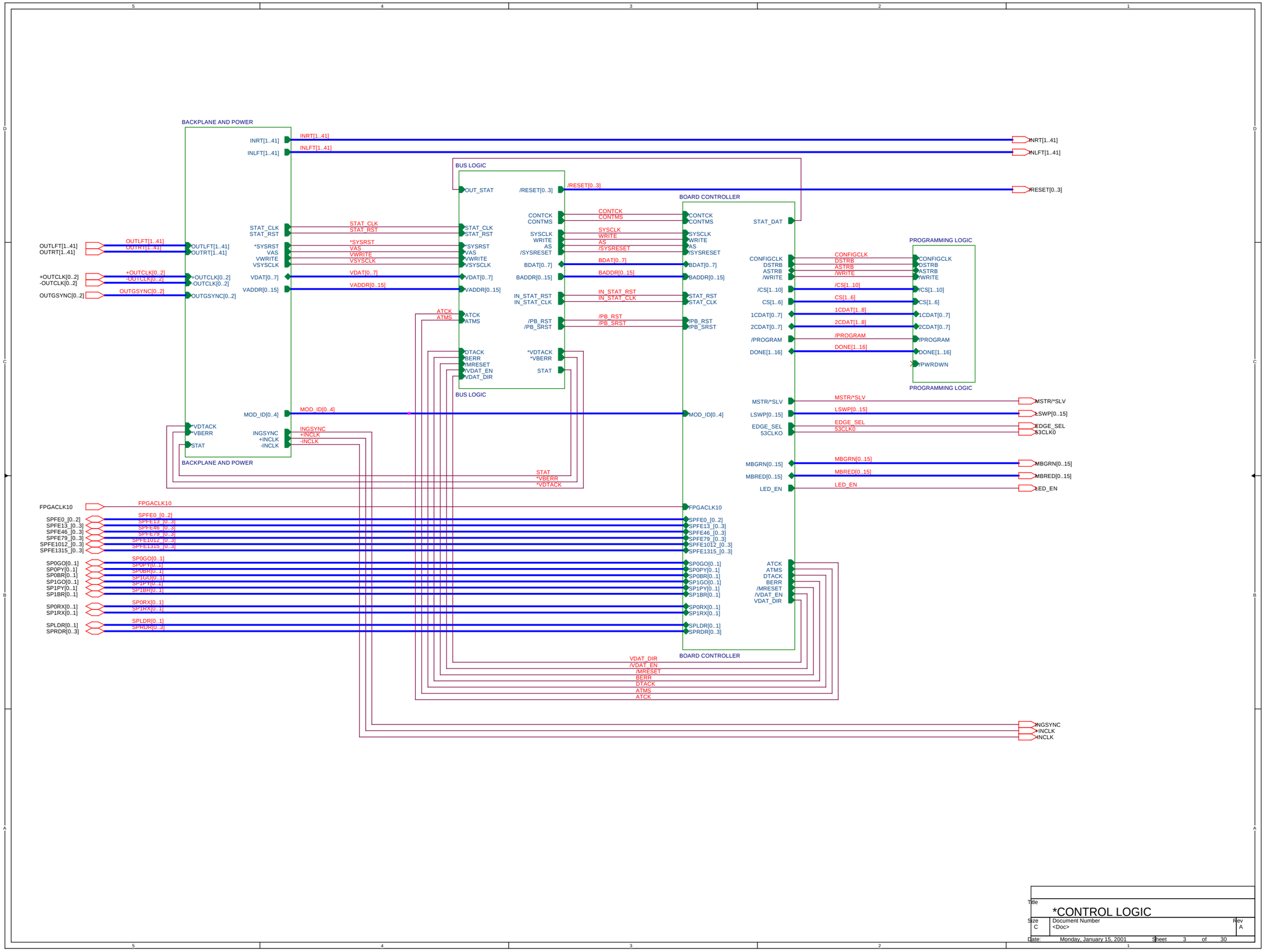

Title: *CONTROL LOGIC

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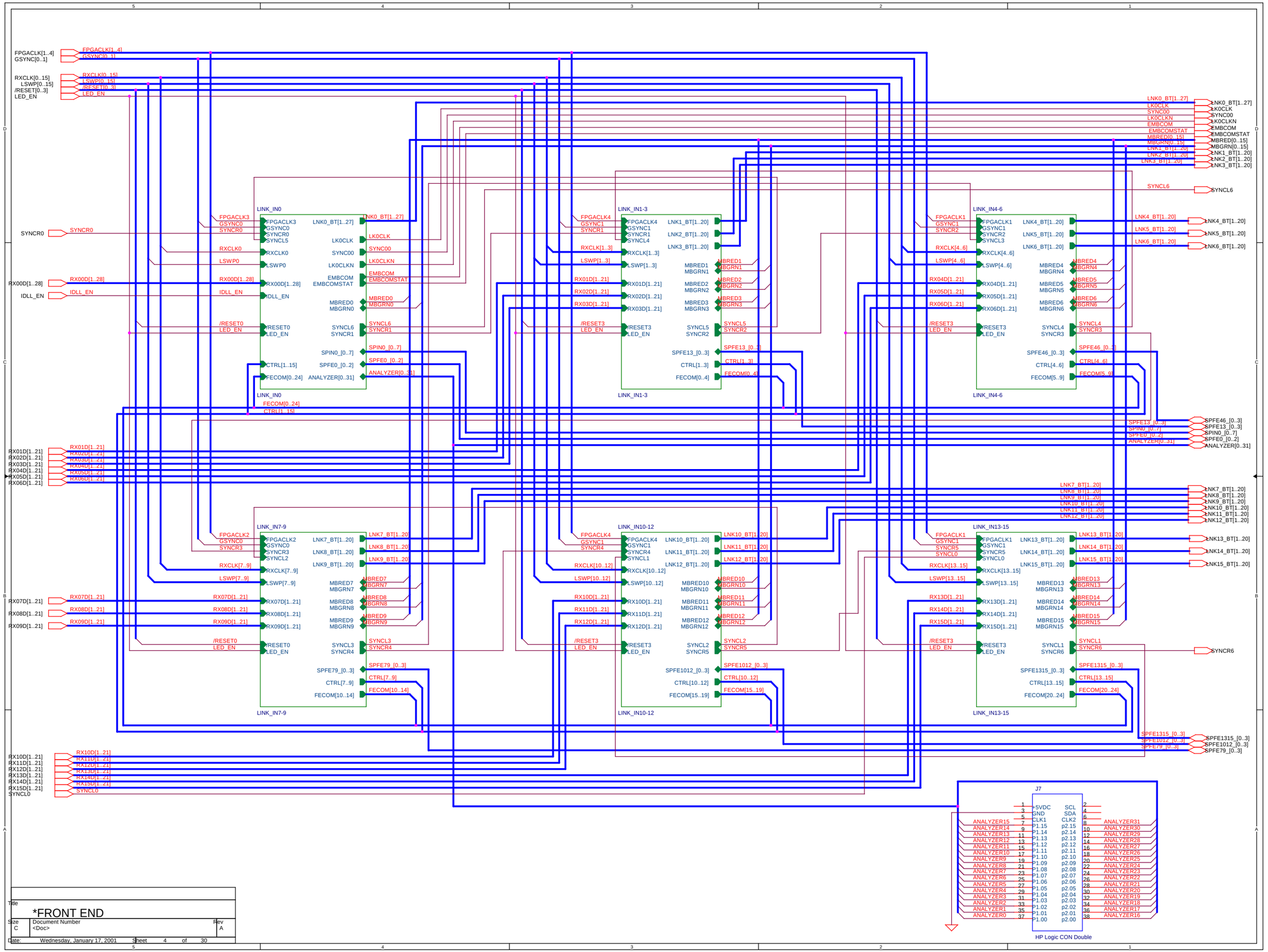

Title
*FRONT END

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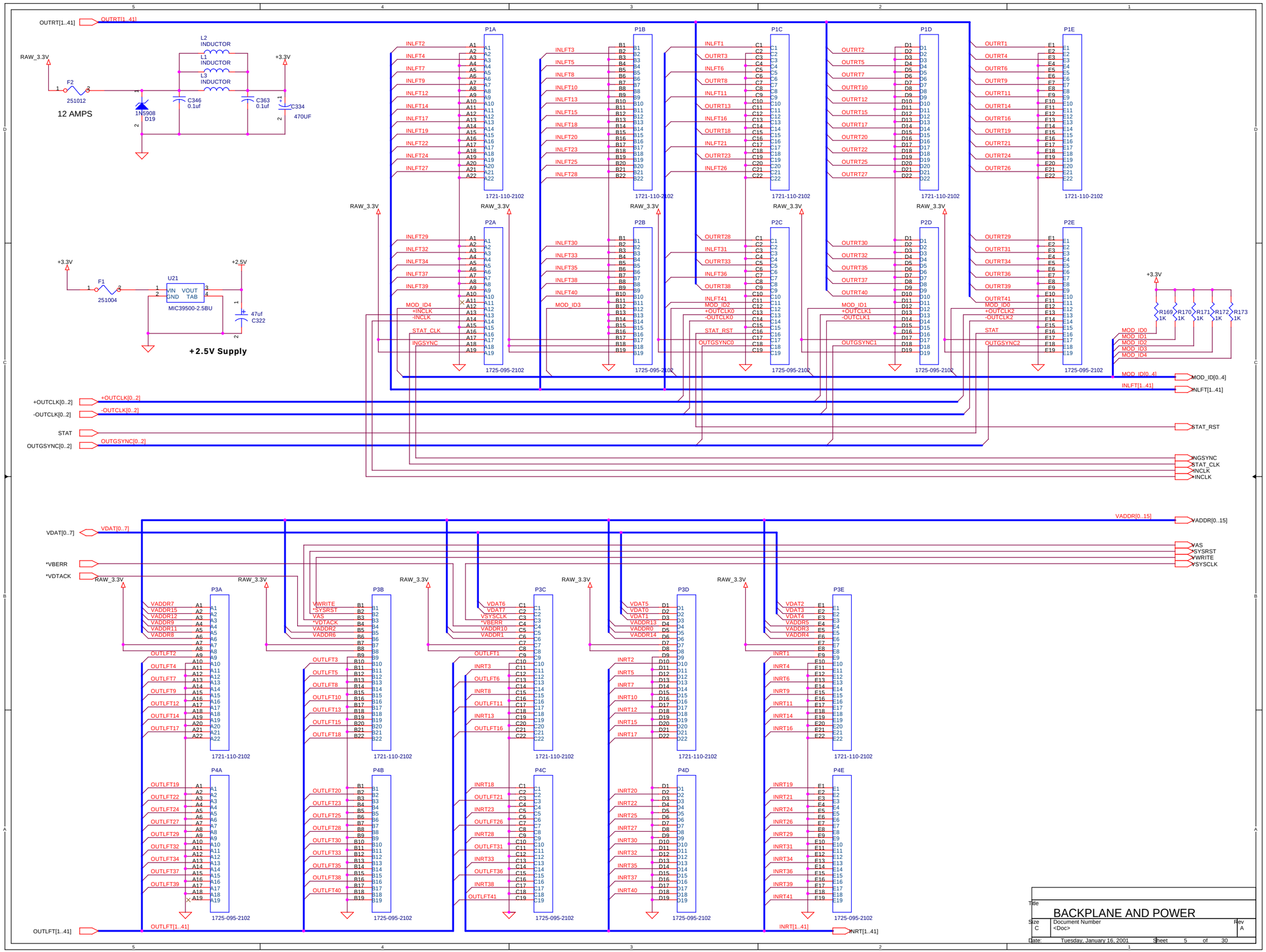
OUTRT[1..41]
RAW_3.3V
F2
251012
12 AMPS
1N5908
D19
L2
INDUCTOR
L1
INDUCTOR
L3
INDUCTOR
C346
0.1uf
C363
0.1uf
+3.3V
C334
470UF
P1A
P1B
P1C
P1D
P1E
1721-110-2102
P2A
P2B
P2C
P2D
P2E
1725-095-2102
+3.3V
F1
251004
U21
VIN VOUT
GND TAB
MIC39500-2.5BU
+2.5V
47uf
C322
+2.5V Supply
R169 1K
R170 1K
R171 1K
R172 1K
R173 1K
MOD_ID[0..4]
INLFT[1..41]
+OUTCLK[0..2]
-OUTCLK[0..2]
STAT
OUTGSYNC[0..2]
STAT_RST
INGSYNC
STAT_CLK
INCLK
*INCLK
VADDR[0..15]
VDAT[0..7]
*VBERR
*VDTACK
VAS
*SYSRST
*WRITE
*SYSCLK
P3A
P3B
P3C
P3D
P3E
P4A
P4B
P4C
P4D
P4E
OUTLFT[1..41]
INRT[1..41]
Title
BACKPLANE AND POWER
Size
C
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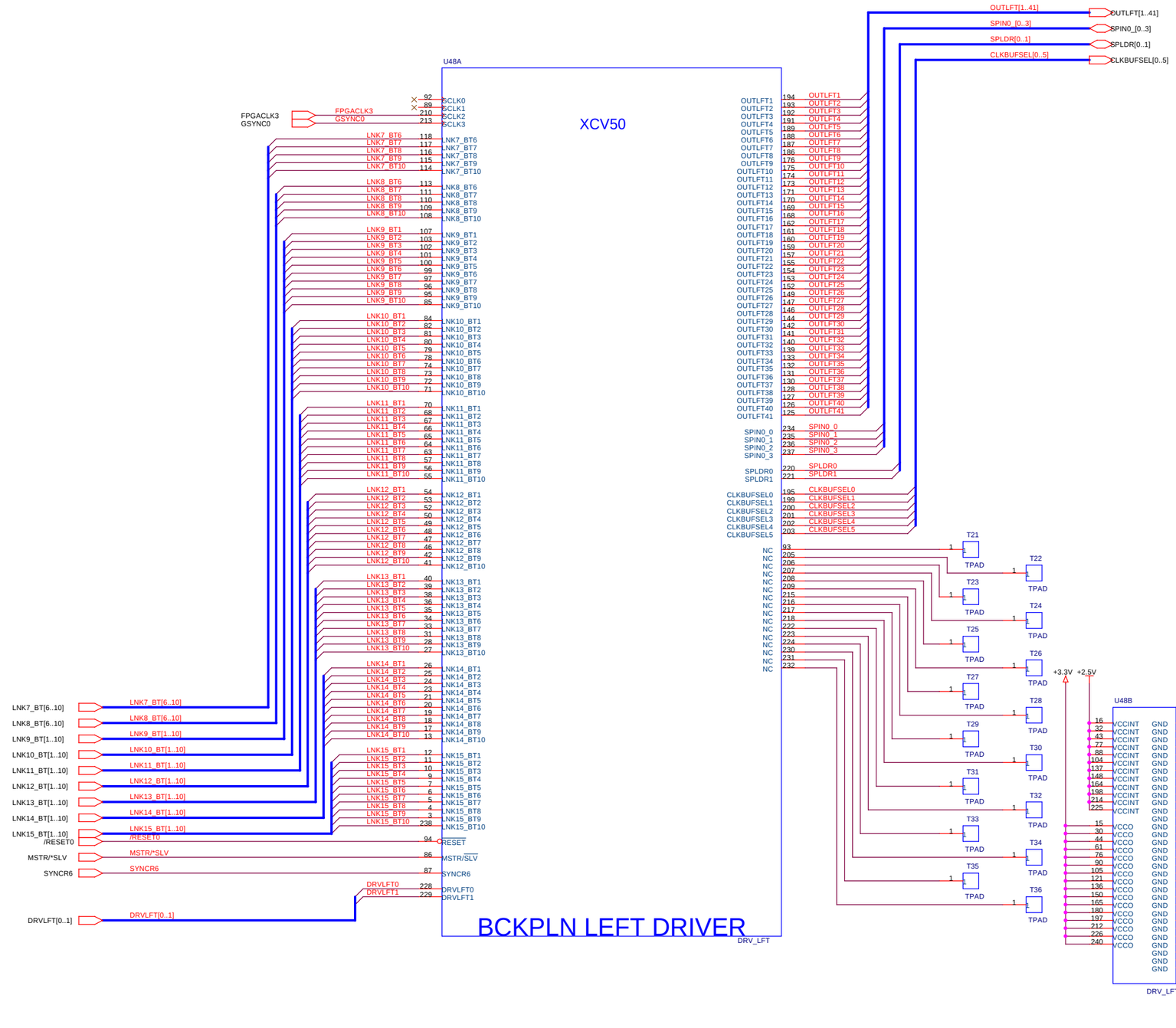

Title
BACKPLANE DRIVER LEFT

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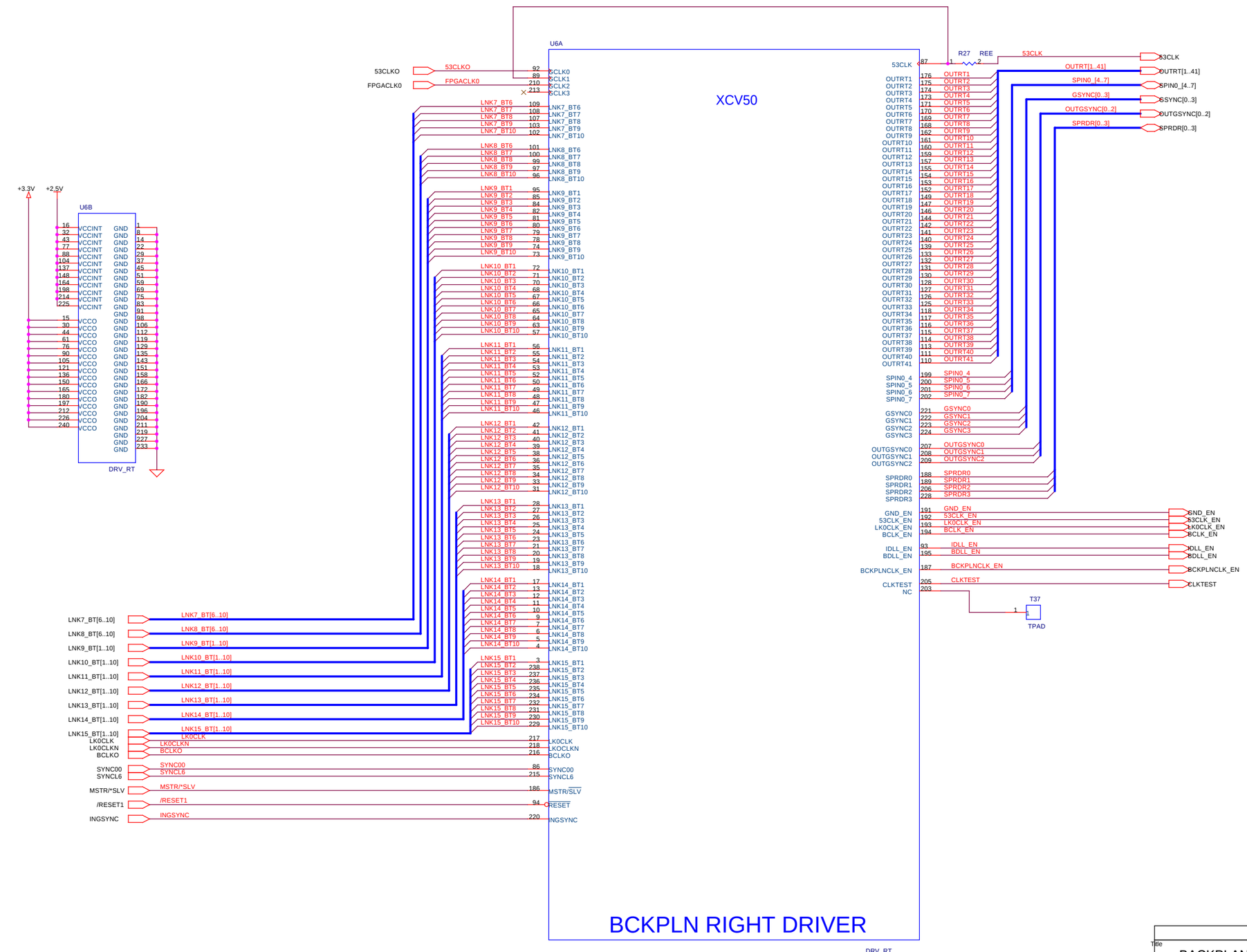

Title	BACKPLANE DRIVER RIGHT
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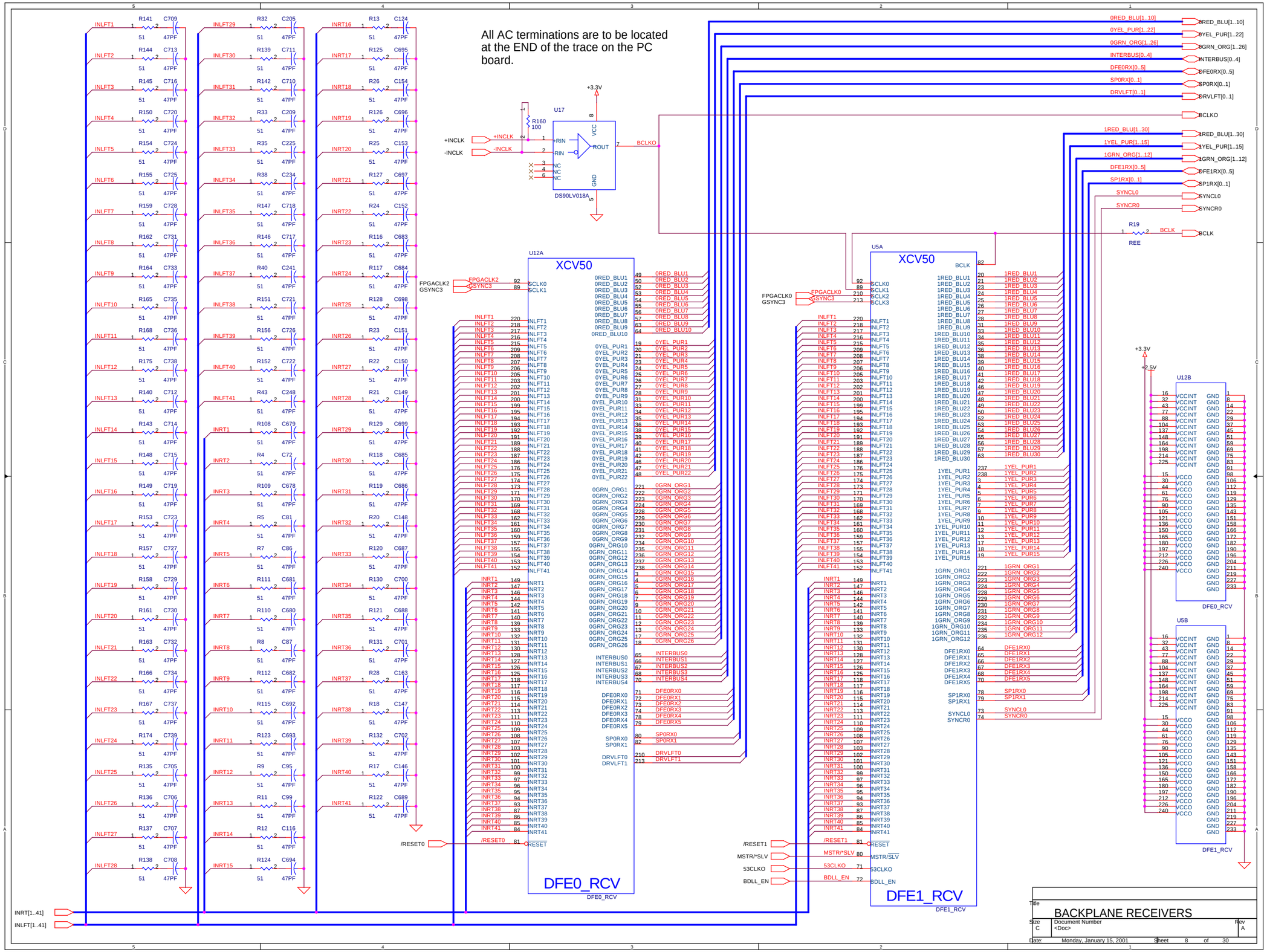
All AC terminations are to be located at the END of the trace on the PC board.
DFE0_RCV
DFE1_RCV
U17
DS90LV018A
U12A
U5A
U12B
U5B
XCV50
BACKPLANE RECEIVERS
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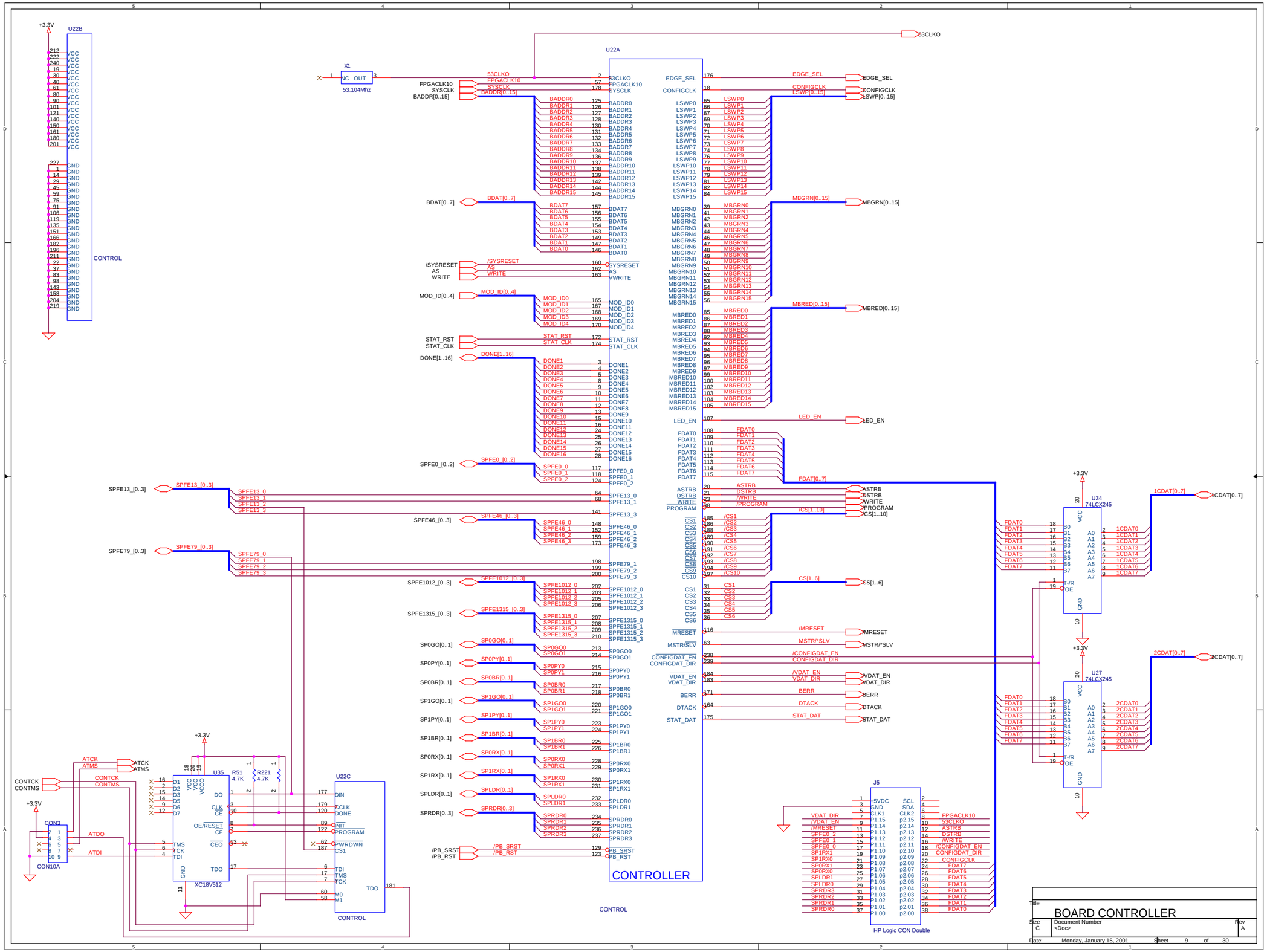
U22B
CONTROL
X1
53.104Mhz
U22A
CONTROLLER
CONTROL
U35
XC18V512
U22C
CONTROL
CON3
CON10A
U34
74LCX245
U27
74LCX245
J5
HP Logic CON Double
53CLKO
EDGE_SEL
CONFIGCLK
LSWP[0..15]
MBGRN[0..15]
MBRED[0..15]
LED_EN
FDAT[0..7]
ASTRB
DSTRB
WRITE
/PROGRAM
/CS[1..10]
CS[1..6]
/MRESET
MSTR/*SLV
/CONFIGDAT_EN
CONFIGDAT_DIR
/VDAT_EN
VDAT_DIR
BERR
DTACK
STAT_DAT
1CDAT[0..7]
2CDAT[0..7]
FPGACLK10
SYSCLK
BADDR[0..15]
BDAT[0..7]
/SYSRESET
AS
WRITE
MOD_ID[0..4]
STAT_RST
STAT_CLK
DONE[1..16]
SPFE0_[0..2]
SPFE13_[0..3]
SPFE46_[0..3]
SPFE79_[0..3]
SPFE1012_[0..3]
SPFE1315_[0..3]
SP0GO[0..1]
SP0PY[0..1]
SP0BR[0..1]
SP1GO[0..1]
SP1PY[0..1]
SP1BR[0..1]
SP0RX[0..1]
SP1RX[0..1]
SPLDR[0..1]
SPRDR[0..3]
/PB_SRST
/PB_RST
ATCK
ATMS
CONTCK
CONTMS
ATDO
ATDI
R51 4.7K
R221 4.7K
+3.3V
Title
BOARD CONTROLLER
Size C
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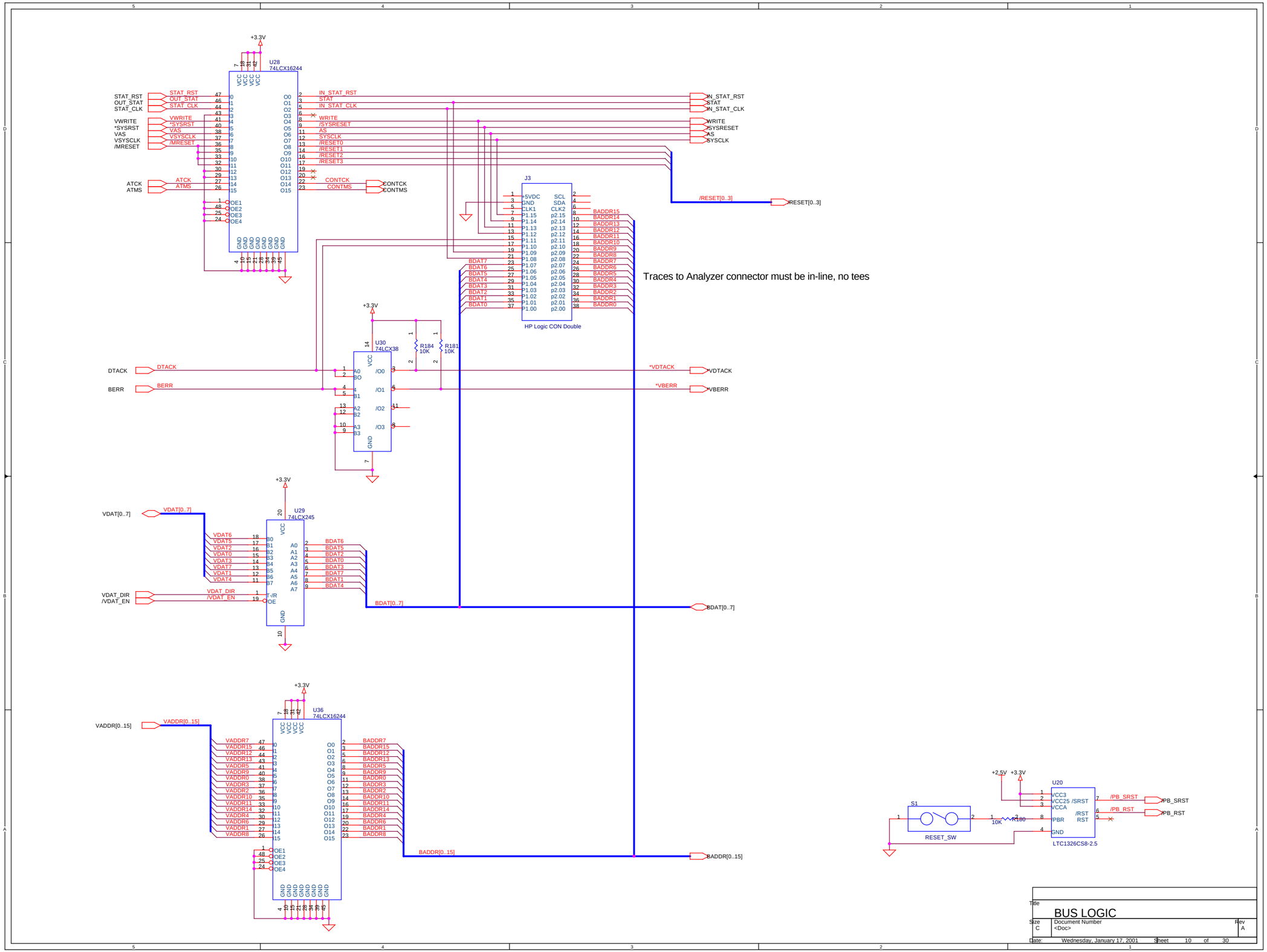

Title: BUS LOGIC

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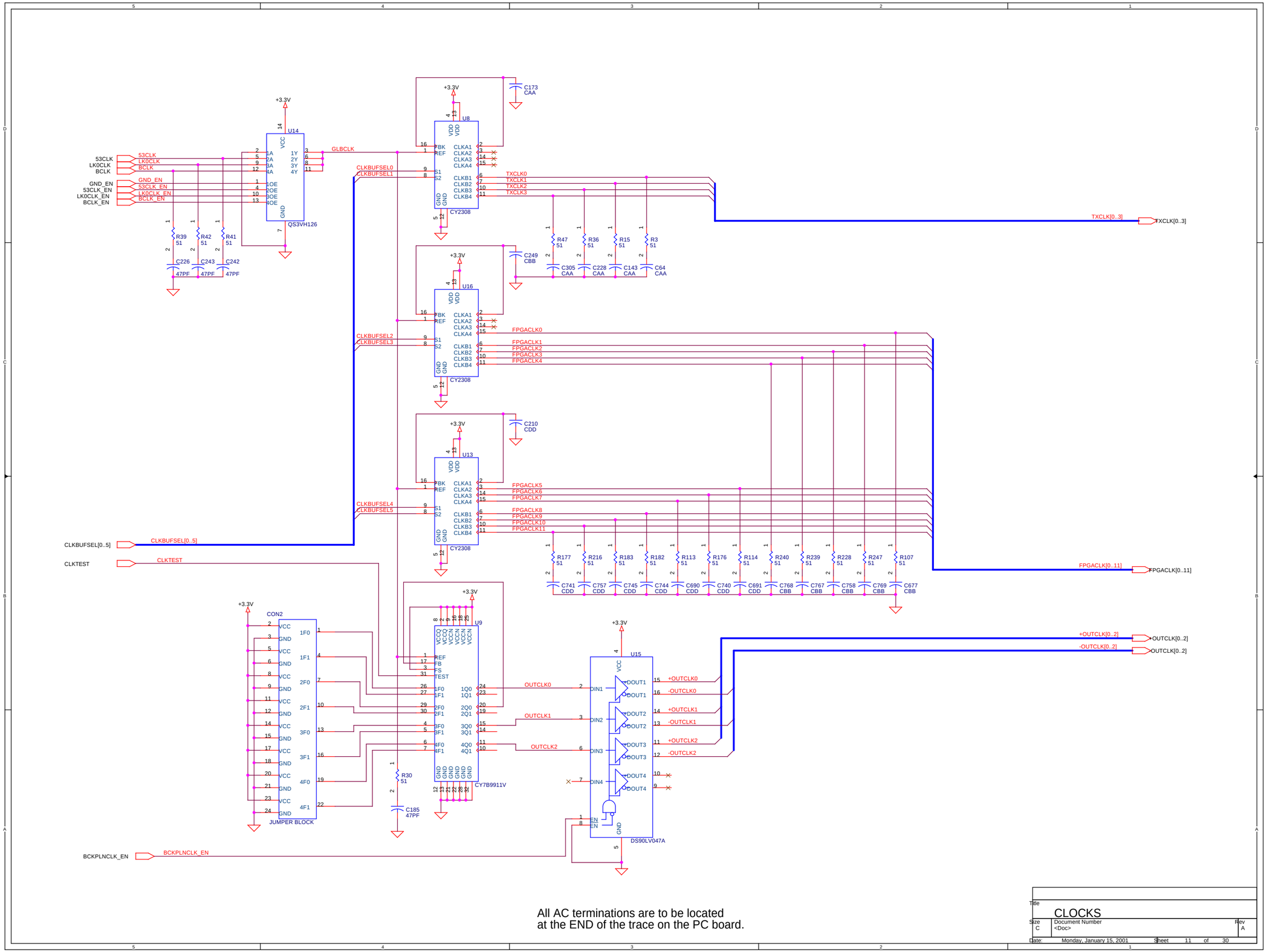

All AC terminations are to be located
at the END of the trace on the PC board.

Title	CLOCKS	
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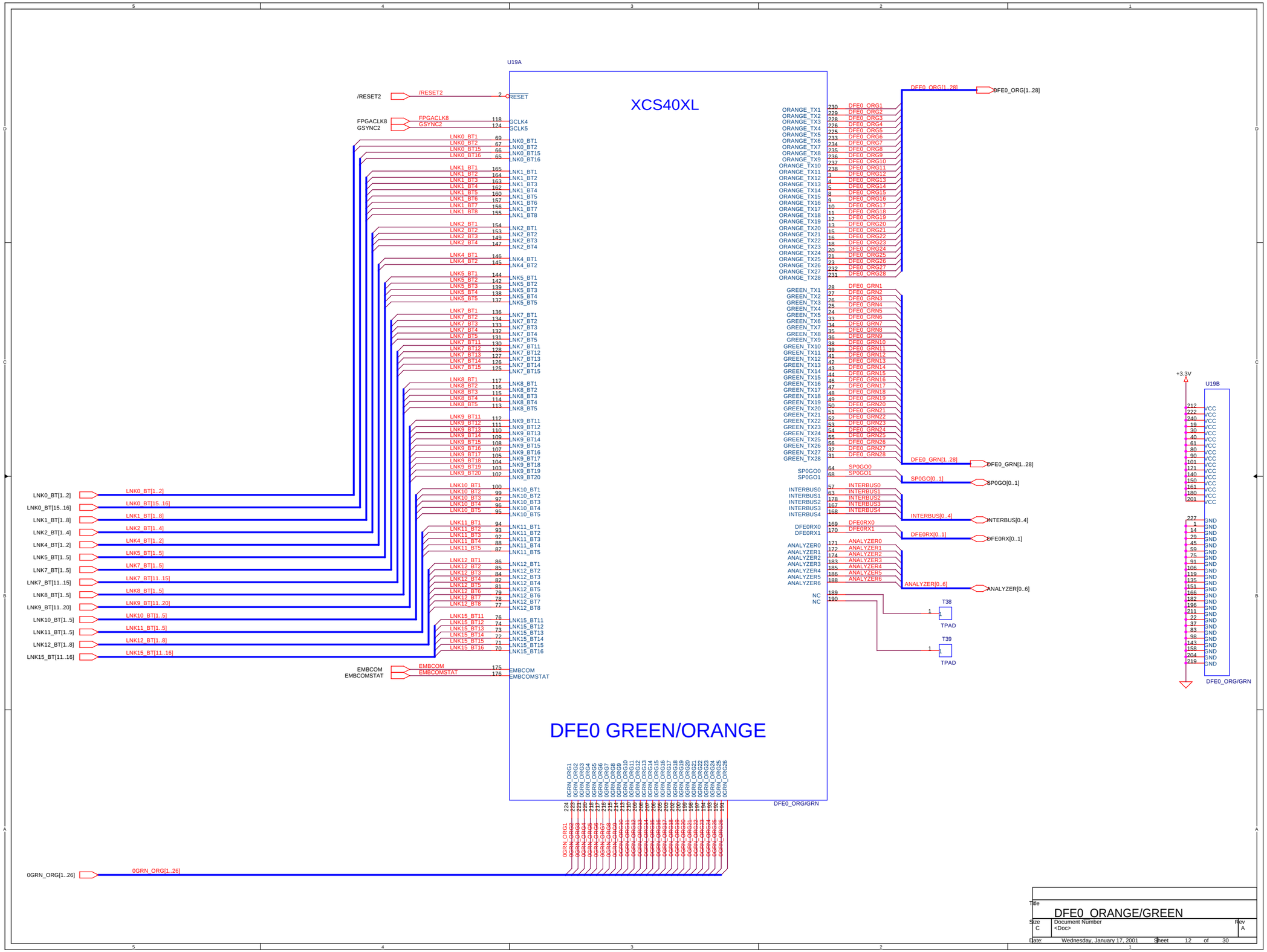

Title
DFE0_ORANGE/GREEN

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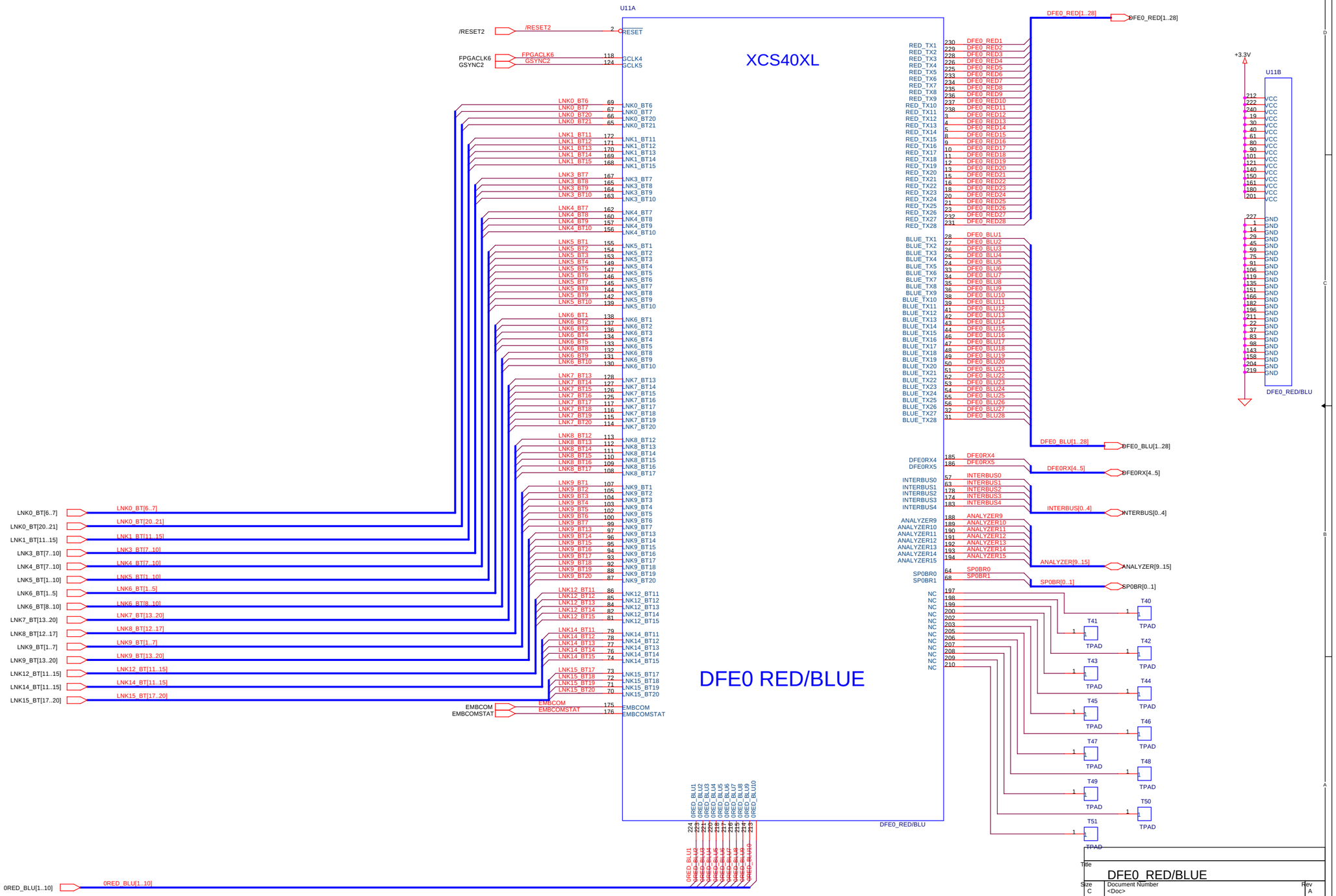
U11A
XCS40XL
/RESET2
FPGACLK6
GSYNC2
DFE0 RED/BLUE
DFE0_RED[1..28]
DFE0_BLU[1..28]
DFE0RX[4..5]
INTERBUS[0..4]
ANALYZER[9..15]
SP0BR[0..1]
+3.3V
U11B
DFE0_RED/BLU
LNK0_BT[6..7]
LNK0_BT[20..21]
LNK1_BT[11..15]
LNK3_BT[7..10]
LNK4_BT[7..10]
LNK5_BT[1..10]
LNK6_BT[1..5]
LNK6_BT[8..10]
LNK7_BT[13..20]
LNK8_BT[12..17]
LNK9_BT[1..7]
LNK9_BT[13..20]
LNK12_BT[11..15]
LNK14_BT[11..15]
LNK15_BT[17..20]
EMBCOM
EMBCOMSTAT
0RED_BLU[1..10]
TPAD
Title
DFE0_RED/BLUE
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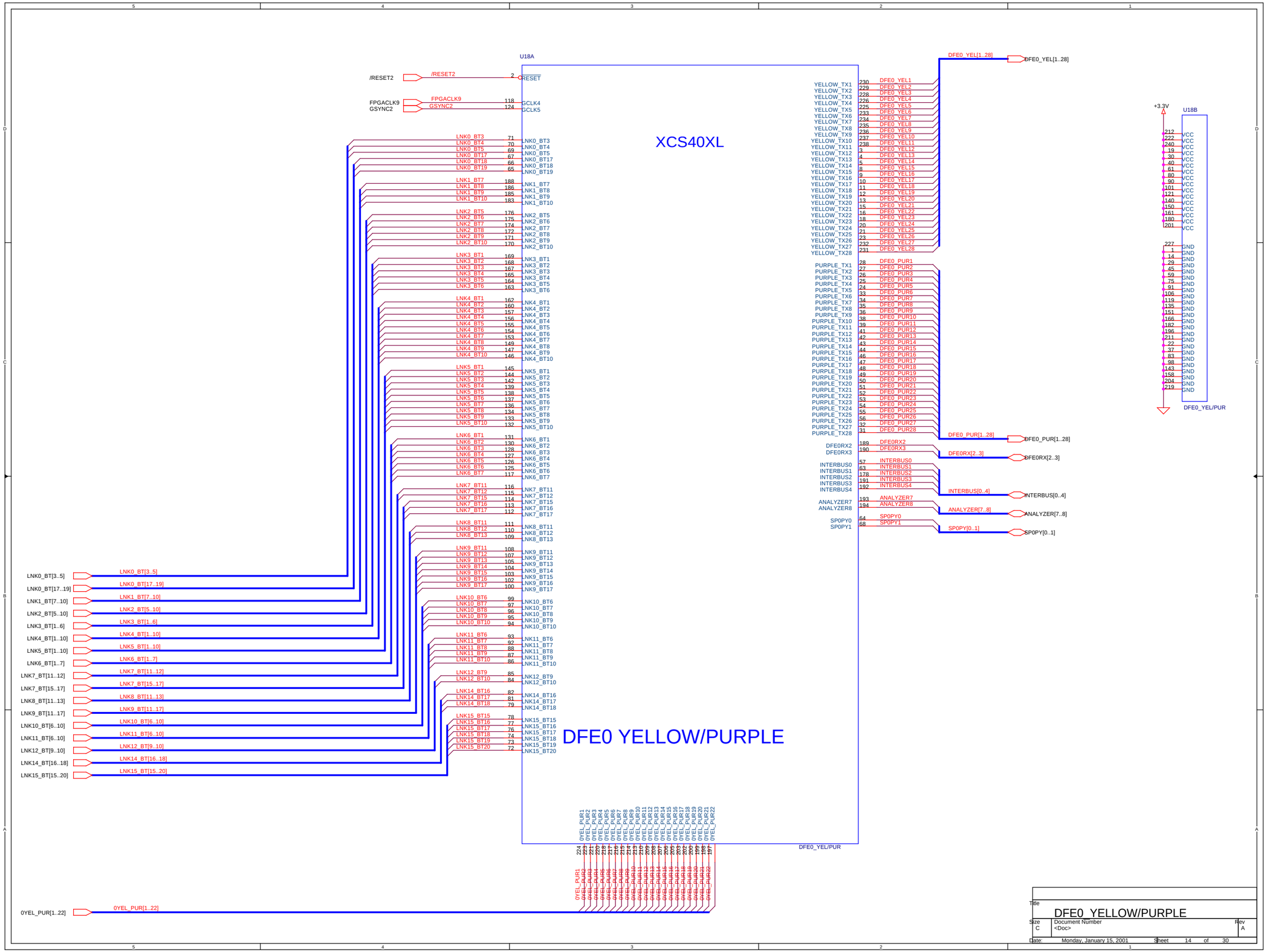

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DFE0_YELLOW/PURPLE

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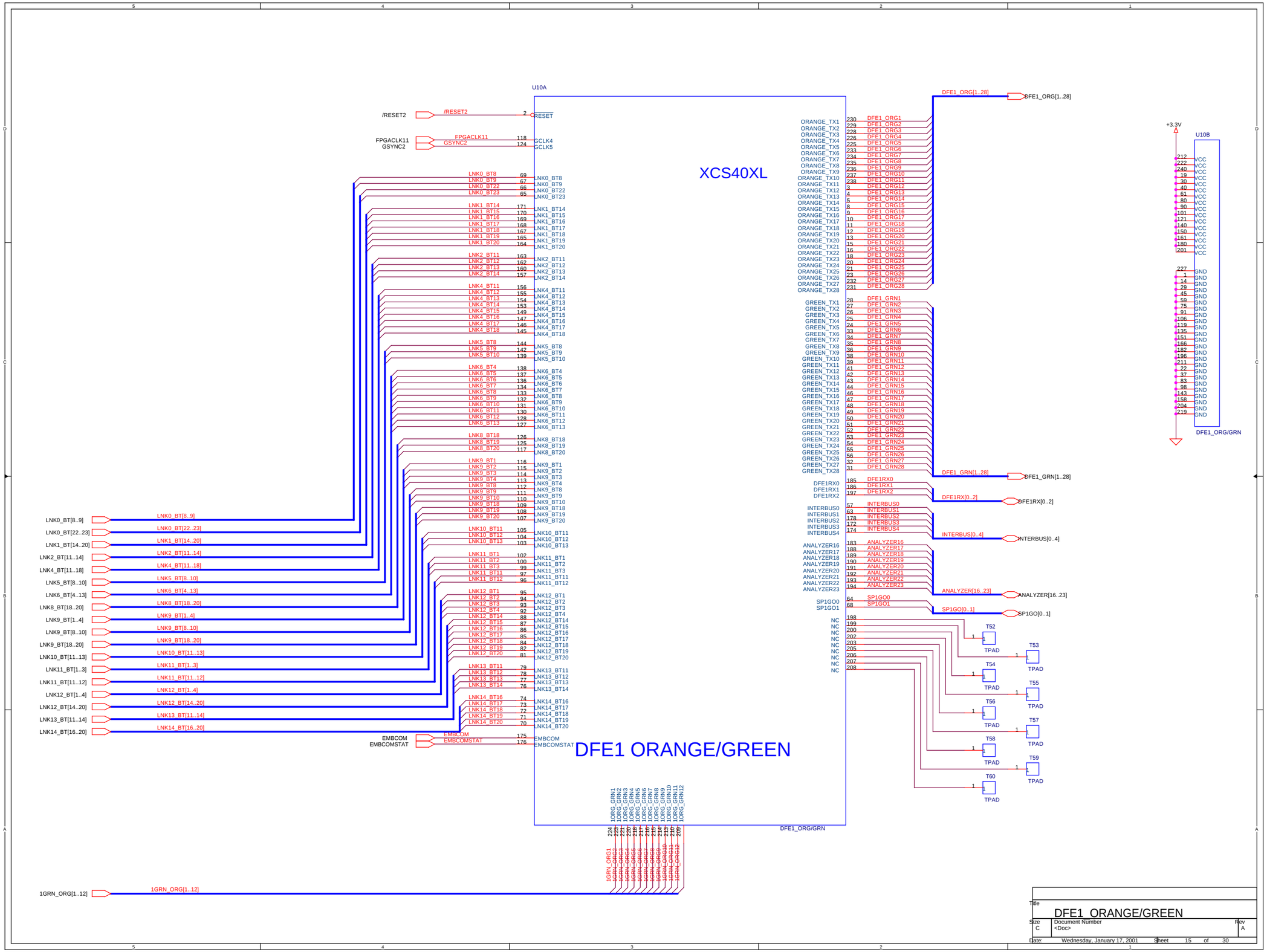
U10A
XCS40XL
DFE1 ORANGE/GREEN
U10B
DFE1_ORG/GRN
/RESET2
FPGACLK11
GSYNC2
EMBCOM
EMBCOMSTAT
1GRN_ORG[1..12]
LNK0_BT[8..9]
LNK0_BT[22..23]
LNK1_BT[14..20]
LNK2_BT[11..14]
LNK4_BT[11..18]
LNK5_BT[8..10]
LNK6_BT[4..13]
LNK8_BT[18..20]
LNK9_BT[1..4]
LNK9_BT[8..10]
LNK9_BT[18..20]
LNK10_BT[11..13]
LNK11_BT[1..3]
LNK11_BT[11..12]
LNK12_BT[1..4]
LNK12_BT[14..20]
LNK13_BT[11..14]
LNK14_BT[16..20]
DFE1_ORG[1..28]
DFE1_GRN[1..28]
DFE1RX[0..2]
INTERBUS[0..4]
ANALYZER[16..23]
SP1GO[0..1]
+3.3V
T52
T53
T54
T55
T56
T57
T58
T59
T60
TPAD
Title
DFE1_ORANGE/GREEN
Size
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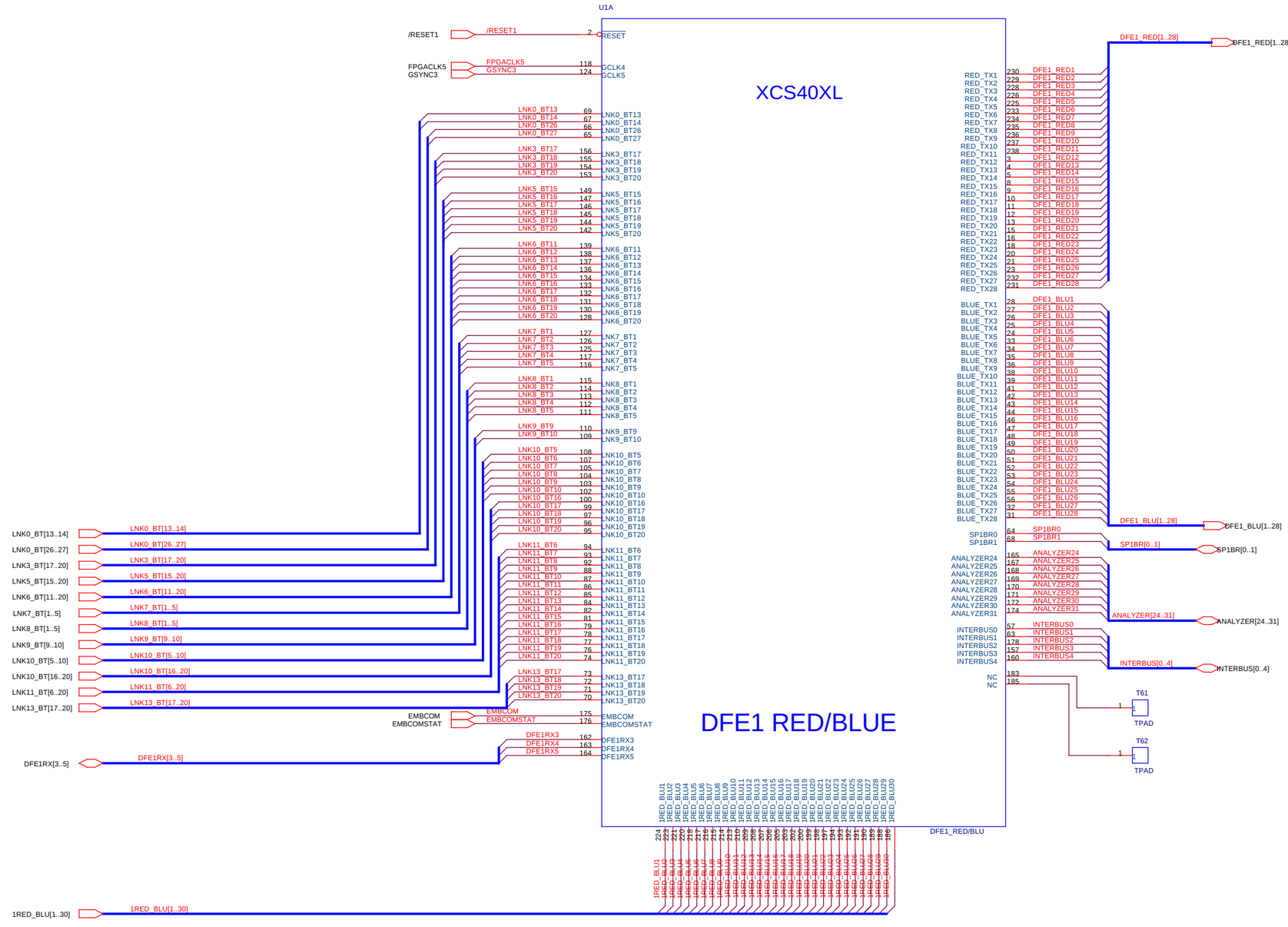

Title
DFE1_RED/BLUE

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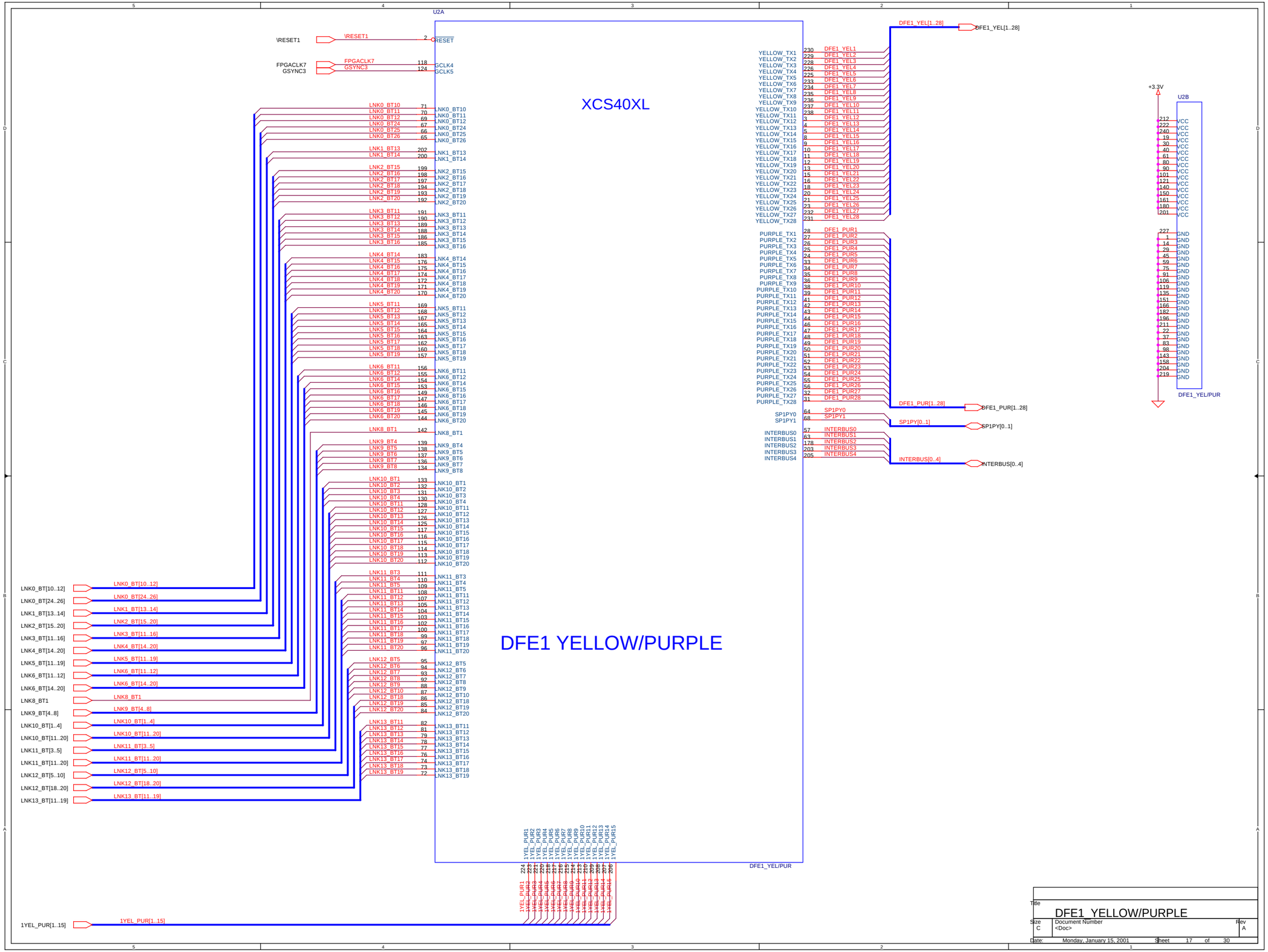

Title: DFE1_YELLOW/PURPLE

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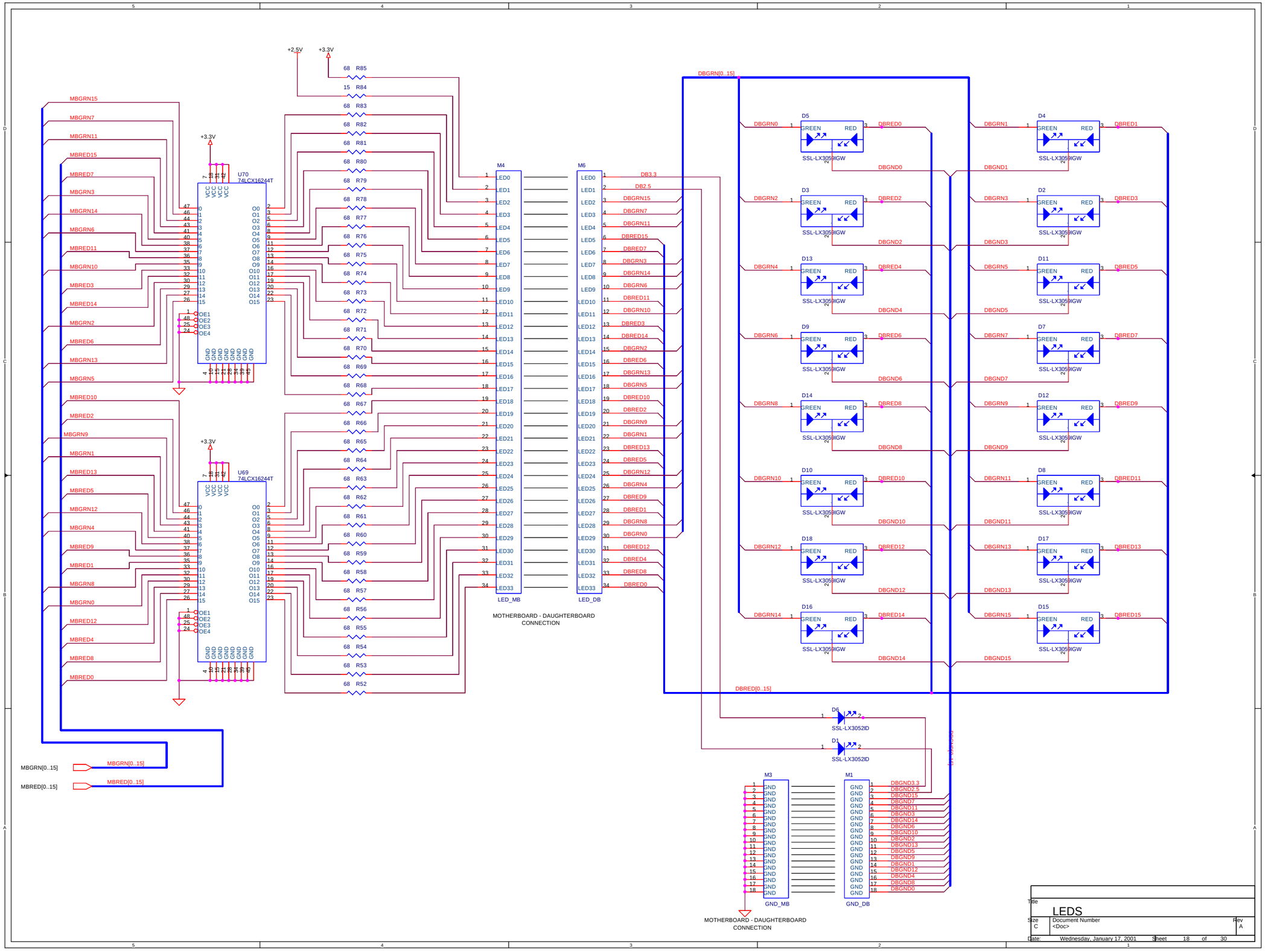
U70
74LCX16244T
U69
74LCX16244T
M4
M6
LED_MB
LED_DB
MOTHERBOARD - DAUGHTERBOARD CONNECTION
M3
M1
GND_MB
GND_DB
MOTHERBOARD - DAUGHTERBOARD CONNECTION
SSL-LX3059IGW
SSL-LX3052ID
MBGRN[0..15]
MBRED[0..15]
DBGRN[0..15]
DBRED[0..15]
DBGND[0..15]
Title
LEDS
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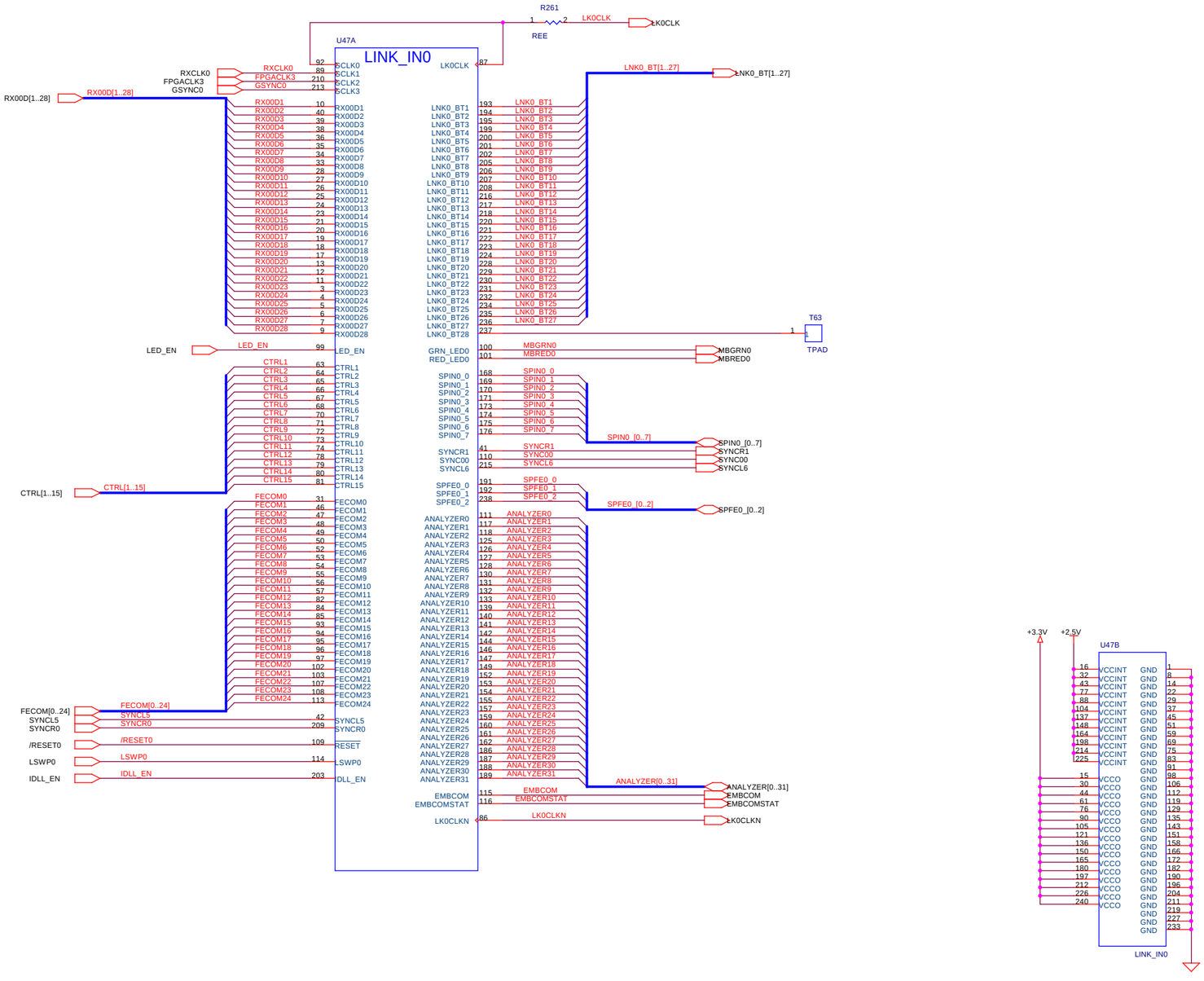

Title
LINK_IN0

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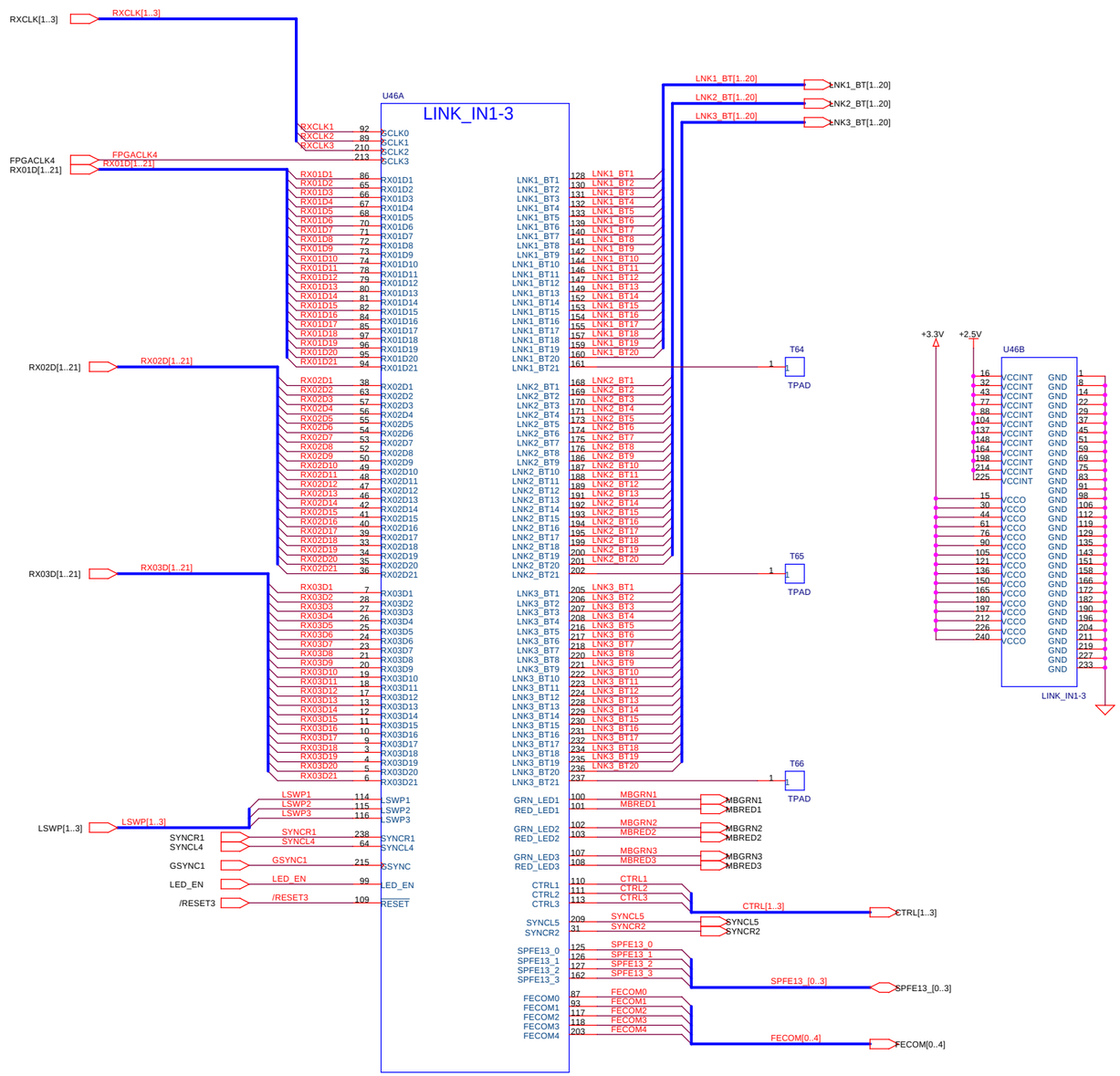

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LINK_IN1-3

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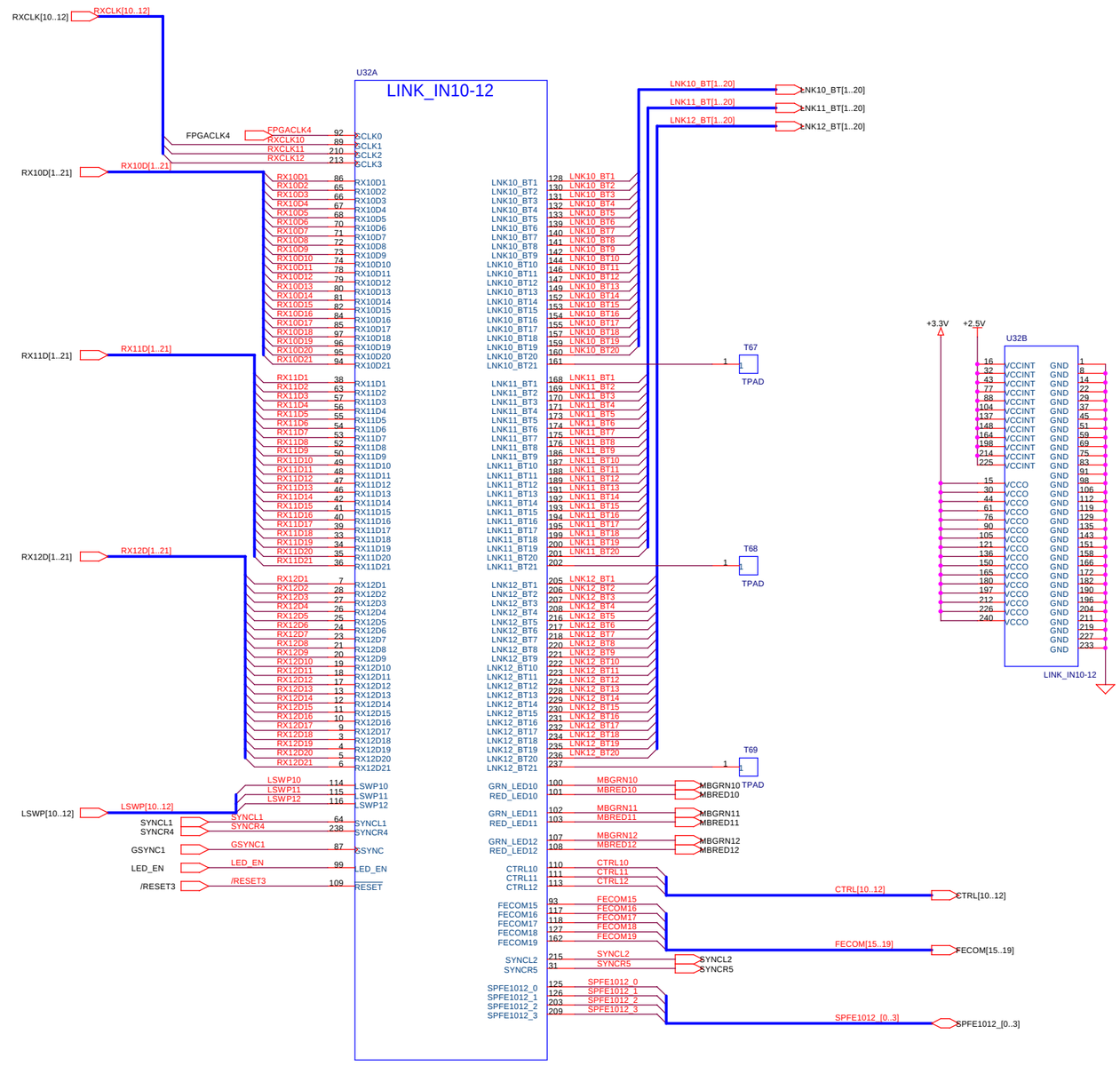

Title
LINK_IN10-12

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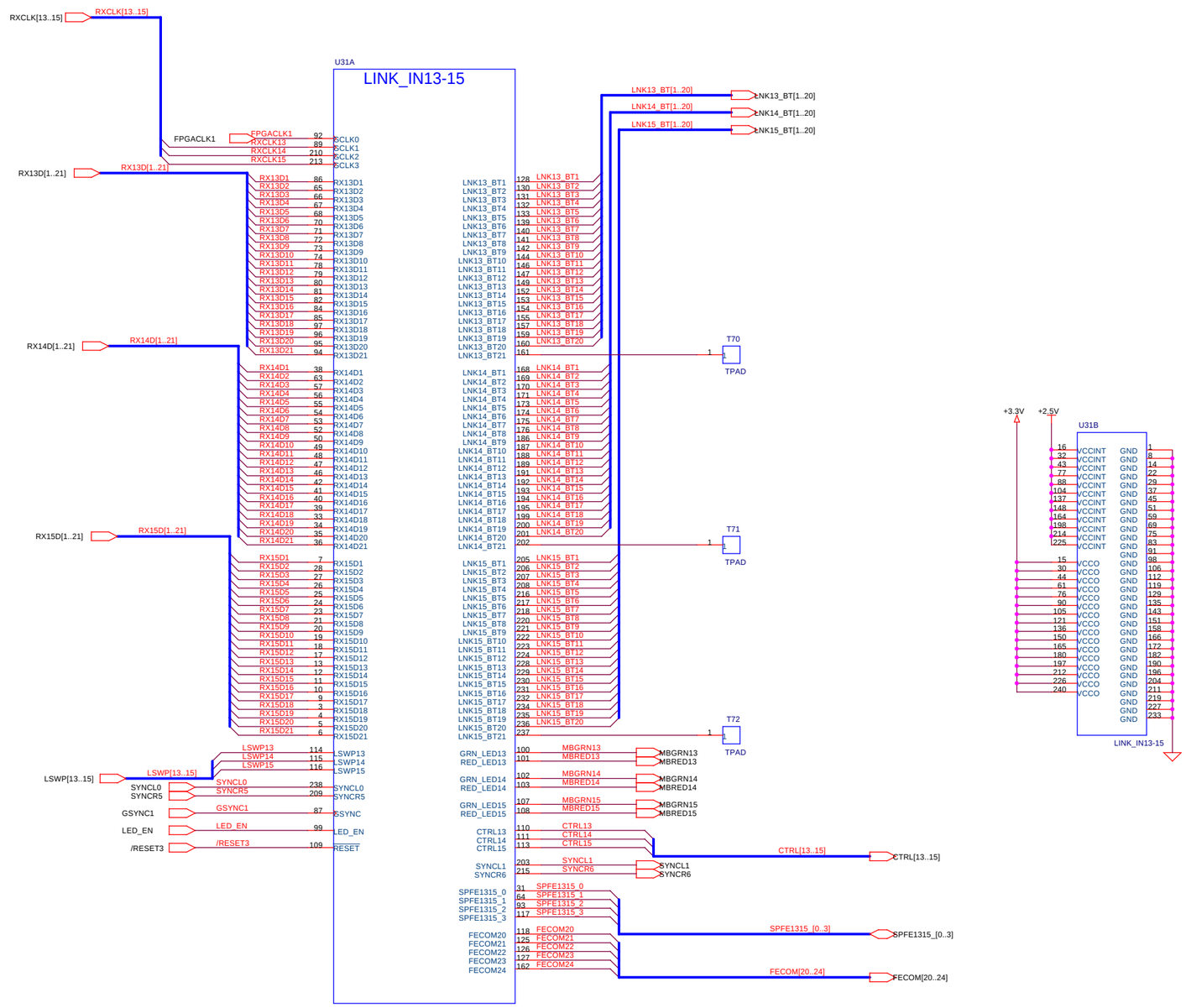

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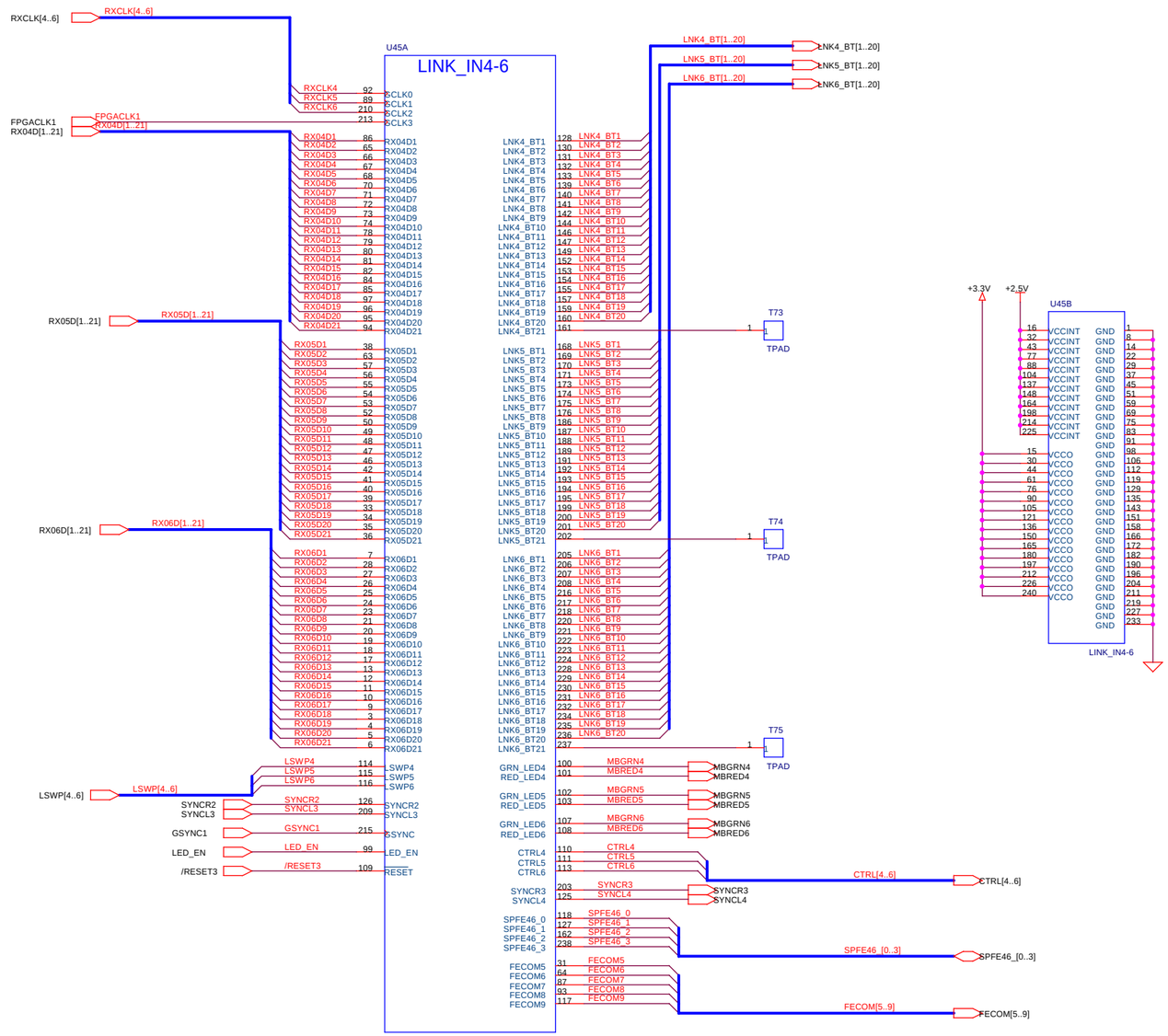

Title
LINK_IN4-6

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C	<Doc>	A

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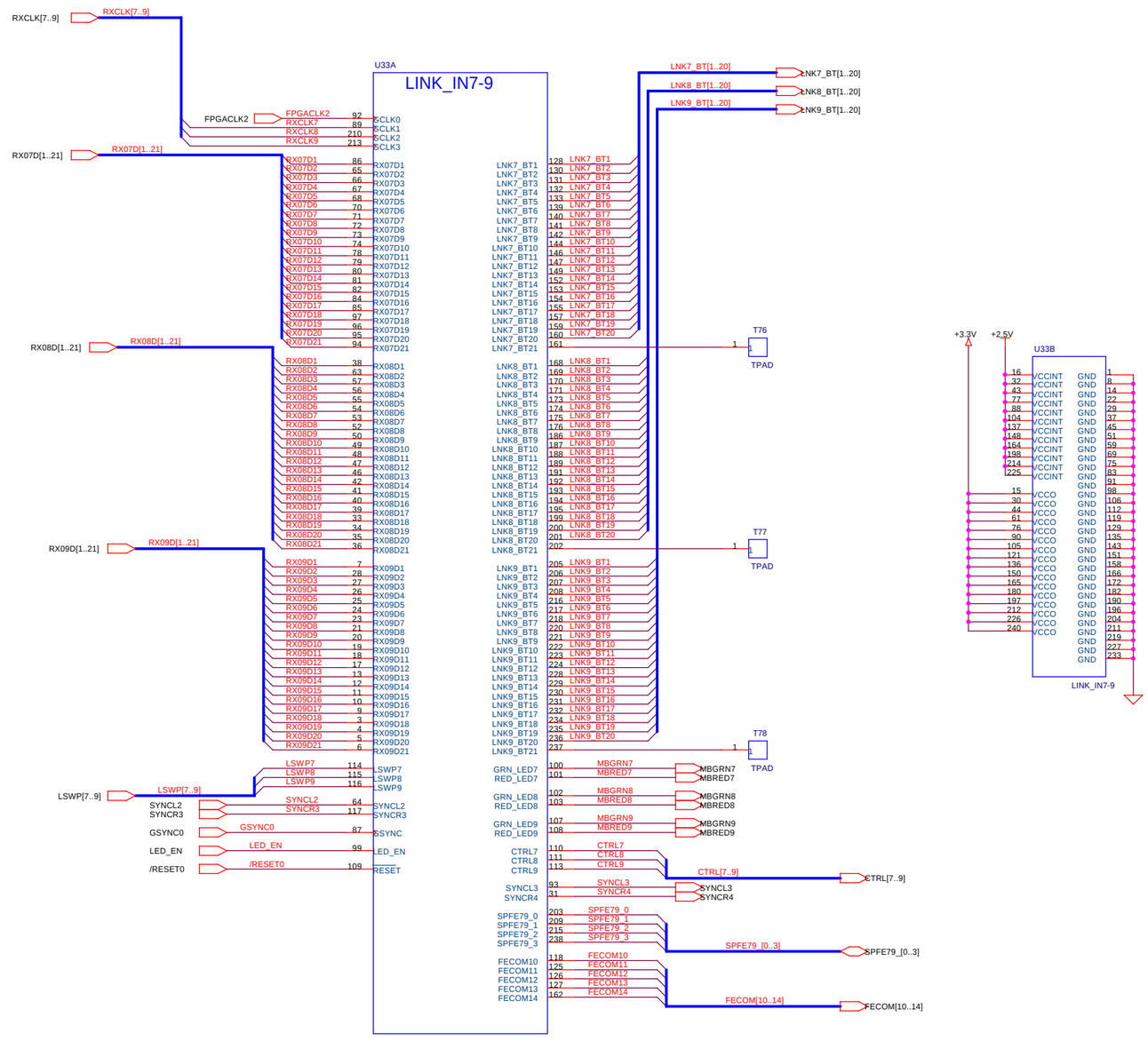

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Size C	Document Number <Doc>
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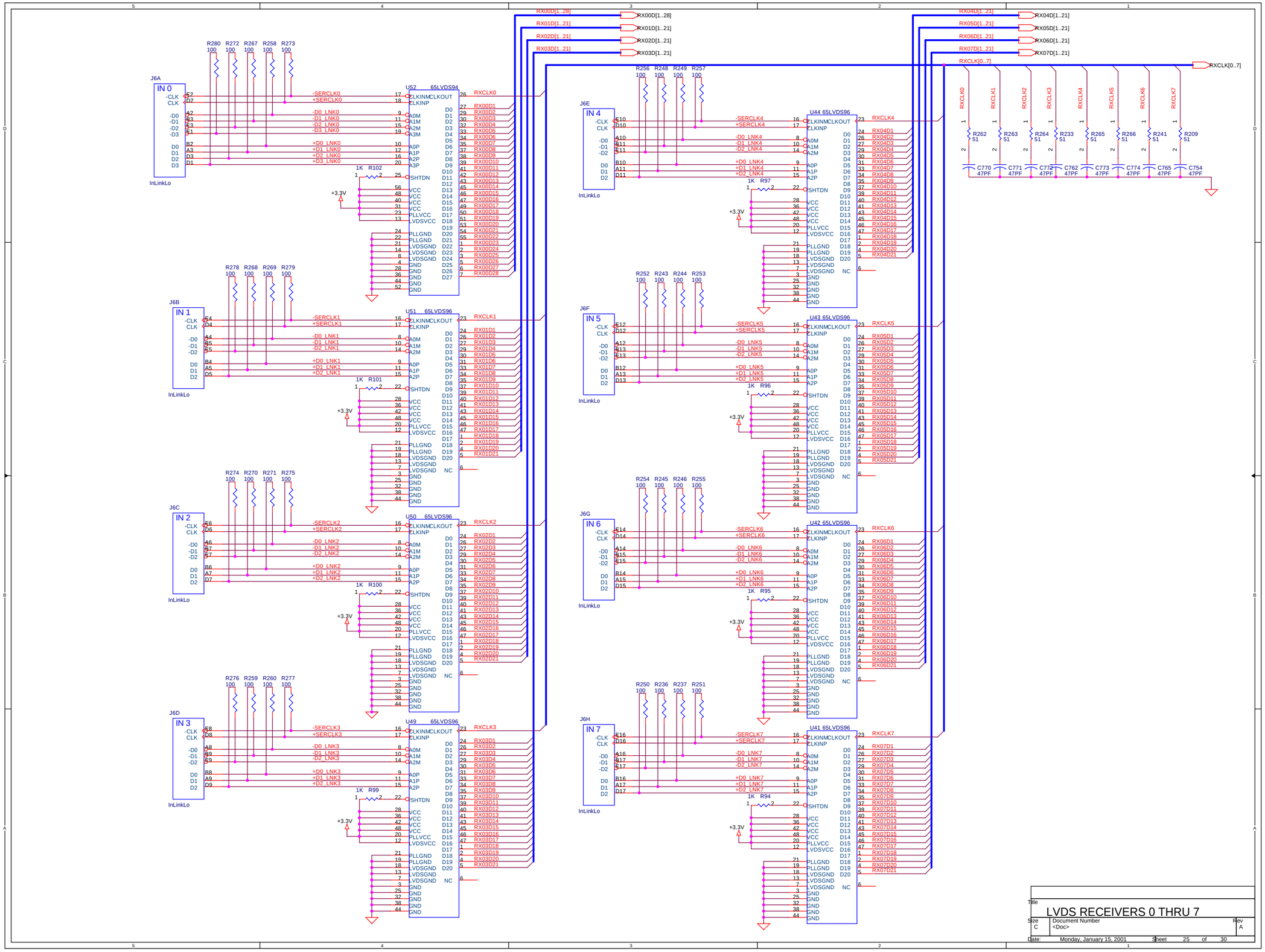

Title
LVDS RECEIVERS 0 THRU 7

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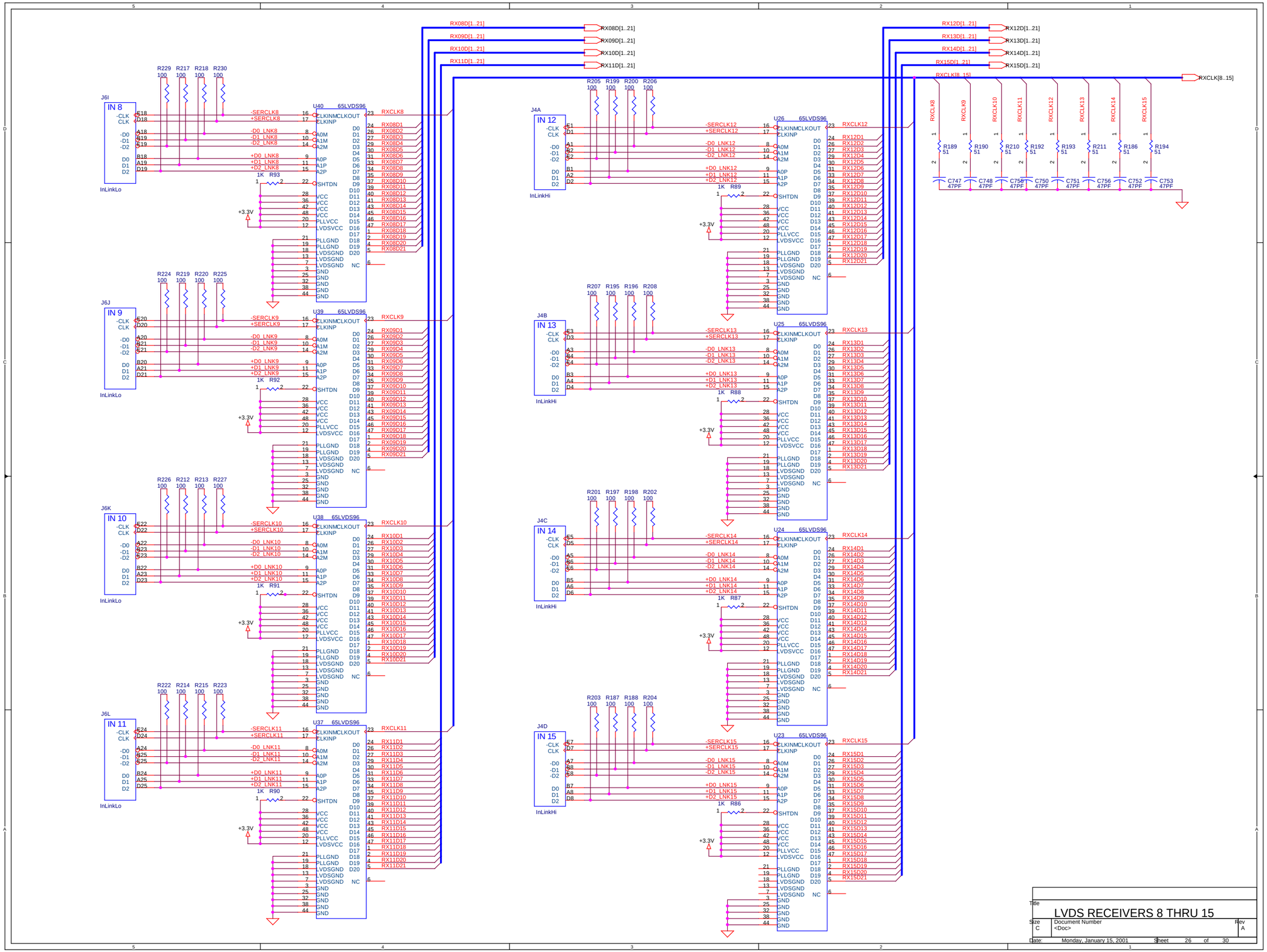
J6I
IN 8
InLinkLo
J6J
IN 9
InLinkLo
J6K
IN 10
InLinkLo
J6L
IN 11
InLinkLo
J4A
IN 12
InLinkHi
J4B
IN 13
InLinkHi
J4C
IN 14
InLinkHi
J4D
IN 15
InLinkHi
U40 65LVDS96
U39 65LVDS96
U38 65LVDS96
U37 65LVDS96
U26 65LVDS96
U25 65LVDS96
U24 65LVDS96
U23 65LVDS96
RX08D[1..21]
RX09D[1..21]
RX10D[1..21]
RX11D[1..21]
RX12D[1..21]
RX13D[1..21]
RX14D[1..21]
RX15D[1..21]
RXCLK[8..15]
RXCLK8
RXCLK9
RXCLK10
RXCLK11
RXCLK12
RXCLK13
RXCLK14
RXCLK15
+3.3V
Title
LVDS RECEIVERS 8 THRU 15
Size
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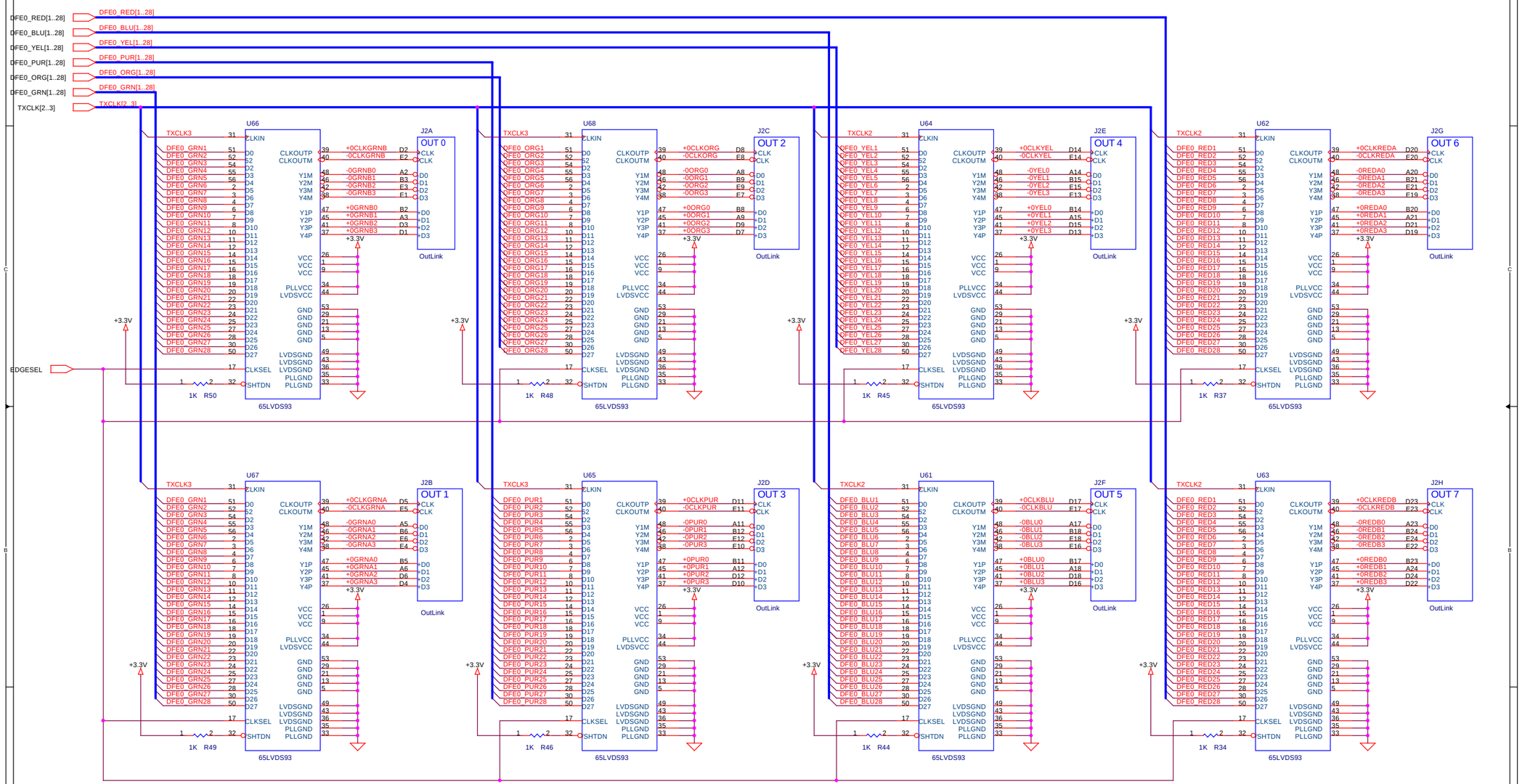

TO DFE0

Title	LVDS TX DFE0
Size C	Document Number <Doc>
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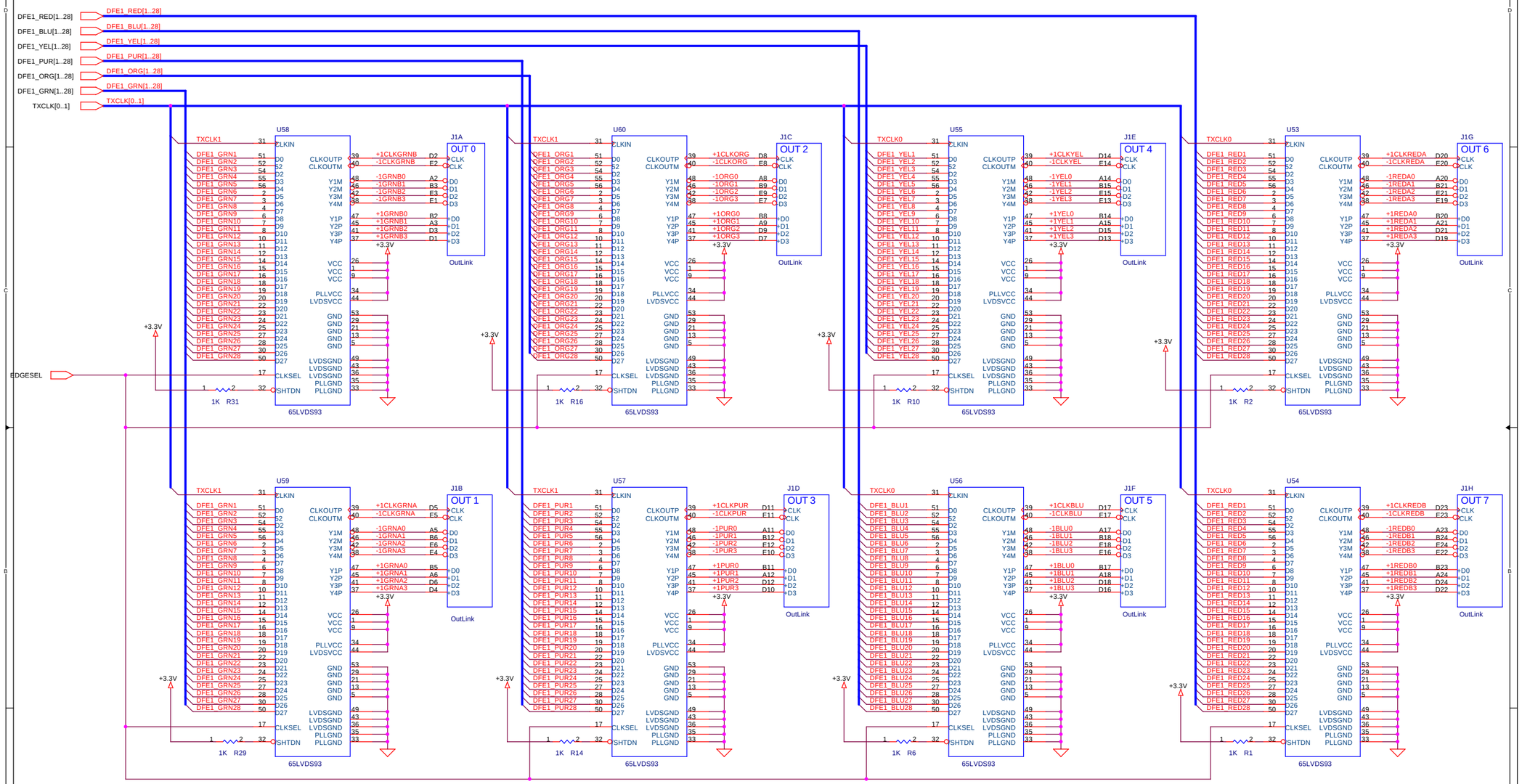

TO DFE1

NOTE: VCC IS +3.3V

Title	LVDS TX DFE1
Size C	Document Number <Doc>
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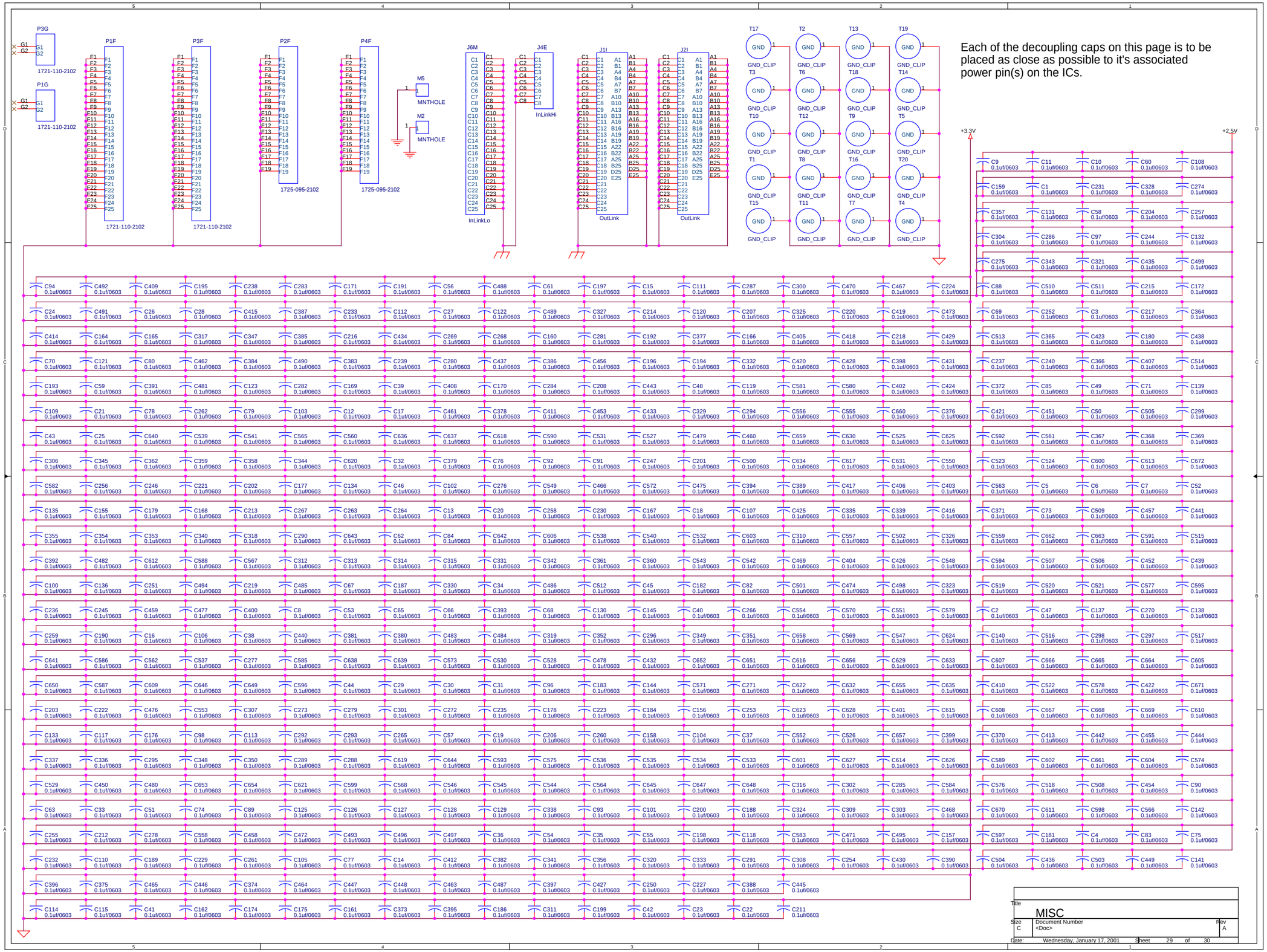
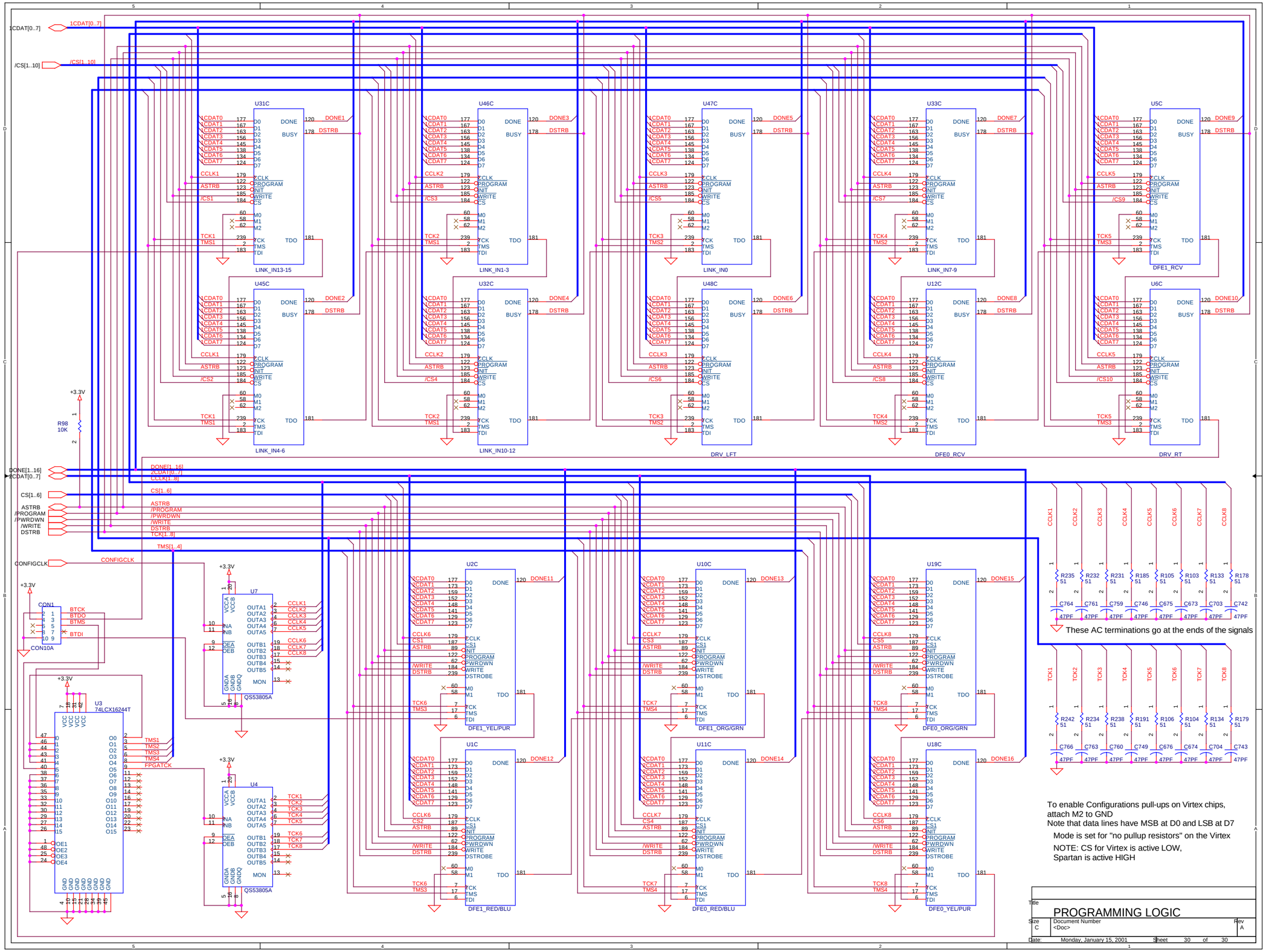


Each of the decoupling caps on this page is to be placed as close as possible to it's associated power pin(s) on the ICs.


1CDAT[0..7]
/CS[1..10]
U31C
U46C
U47C
U33C
U5C
U45C
U32C
U48C
U12C
U6C
LINK_IN13-15
LINK_IN1-3
LINK_IN0
LINK_IN7-9
DFE1_RCV
LINK_IN4-6
LINK_IN10-12
DRV_LFT
DFE0_RCV
DRV_RT
+3.3V
R98
10K
DONE[1..16]
2CDAT[0..7]
CCLK[1..8]
CS[1..6]
ASTRB
/PROGRAM
/PWRDWN
/WRITE
DSTRB
TCK[1..8]
TMS[1..4]
CONFIGCLK
CON1
CON10A
BTCK
BTDO
BTMS
BTDI
U7
U4
QS53805A
U3
74LCX16244T
FPGATCK
U2C
U1C
U10C
U11C
U19C
U18C
DFE1_YEL/PUR
DFE1_RED/BLU
DFE0_ORG/GRN
DFE0_RED/BLU
DFE0_YEL/PUR
R235 51
R232 51
R231 51
R185 51
R105 51
R103 51
R133 51
R178 51
C764 47PF
C761 47PF
C759 47PF
C746 47PF
C675 47PF
C673 47PF
C703 47PF
C742 47PF
These AC terminations go at the ends of the signals
R242 51
R234 51
R238 51
R191 51
R106 51
R104 51
R134 51
R179 51
C766 47PF
C763 47PF
C760 47PF
C749 47PF
C676 47PF
C674 47PF
C704 47PF
C743 47PF
To enable Configurations pull-ups on Virtex chips,
attach M2 to GND
Note that data lines have MSB at D0 and LSB at D7
Mode is set for "no pullup resistors" on the Virtex
NOTE: CS for Virtex is active LOW,
Spartan is active HIGH
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PROGRAMMING LOGIC
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Document Number
<Doc>
Rev A
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