

Real-Time Data Reorganizer for the D0 Central Fiber Tracker Trigger System at Fermilab

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In a few words



THE SYSTEM

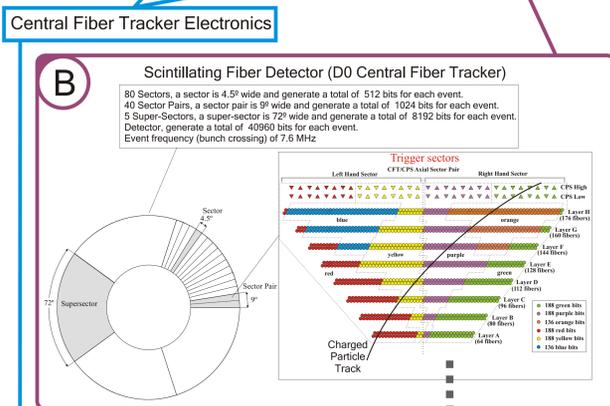
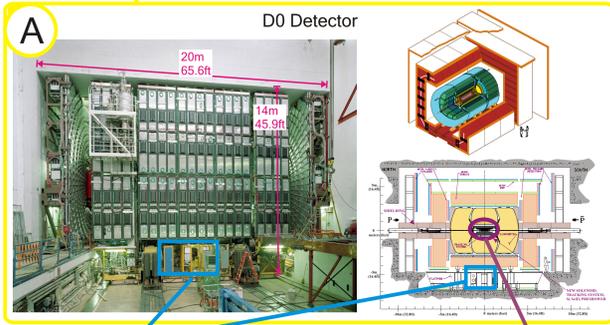
A component of the D0 Detector at Fermilab (A) is the Central Fiber Tracker (CFT) (B). The CFT is constructed of scintillating fibers that are organized together in a very precise array of ribbons, placed onto a structure formed by eight co-axial cylinders. The energy deposited into the scintillating fibers by particle interactions is transformed into visible light. The light travels through the scintillating fiber and through an optical (clear) fiber connected to it (C), reaching a very sensitive light detector, the Visible Light Photon Counter (VLPC) (D), hosted in a liquid helium cryostat. The VLPCs are a derivative of solid-state photomultipliers and are used to convert the scintillation light into electrical signals. These are discriminated and digitized by the Analog Front-End boards (AFE) (E). The Mixer System (F) receives the digitized data from the AFEs, then processes and re-organizes it in real-time with minimal delay from cylindrical geometry into 80 azimuthal wedges or sectors. The restructured data are transmitted to the Digital Front-End (DFE) board system (G). The DFE system uses the data to contribute to level 1 and level 2 trigger decisions (H).

THE MIXER

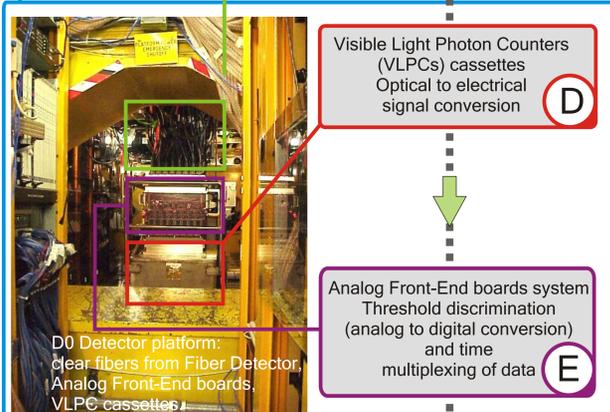
The data Mixer System has been designed to reorganize, in real time, the data produced by the Fermilab D0 Scintillating Fiber Detector. The data is used for the level 1 trigger generation. The Mixer System receives the data from the front-end digitization electronics over 320 Low Voltage Differential Signaling (LVDS) links running at 371 MHz. The input data is de-serialized down to 53 MHz by the LVDS receivers, clock/frame re-synchronized and multiplexed in Field Programmable Gate Arrays (FPGAs). The data is then re-serialized at 371 MHz by LVDS transmitters over 320 LVDS output links and sent to the electronics responsible for level 1 trigger decisions. The Mixer System processes 311 Gigabits per second of data with an input to output delay of 200 nanoseconds.

To find a conceptual design solution that would comply with the design specification a software tool was designed and implemented. The tool allowed us to graphically visualize and analyze the data information and investigate possible design architectures. The tool was also used to generate the portion of VHDL code defining data multiplexing.

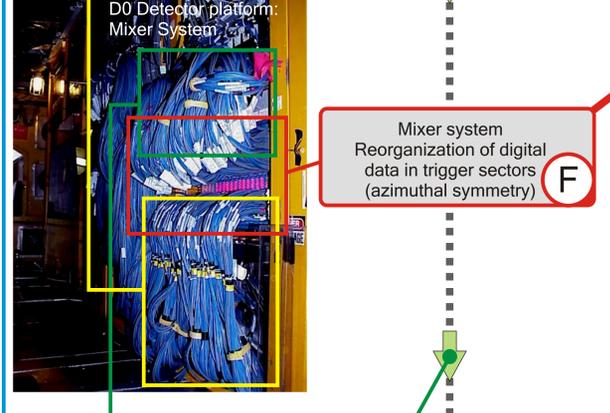
The Mixer System diagnostics allow monitoring input links, clock frequency, frame markers, control bits, clock synchronization, frame realignment and detecting/sending test patterns. The input links test pattern recognition and output links test pattern transmission is used by the trigger system diagnostic to verify the integrity and correctness of the cabling. The Mixer System diagnostic is remotely accessible. A simplified version of the diagnostic using bi-color LEDs on the Mixer board's front panel allow the user to view in real-time the status of signals and flags.



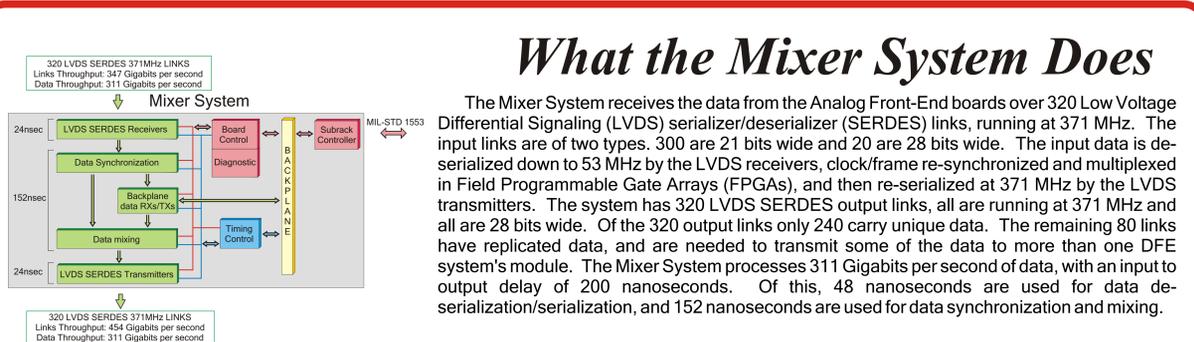
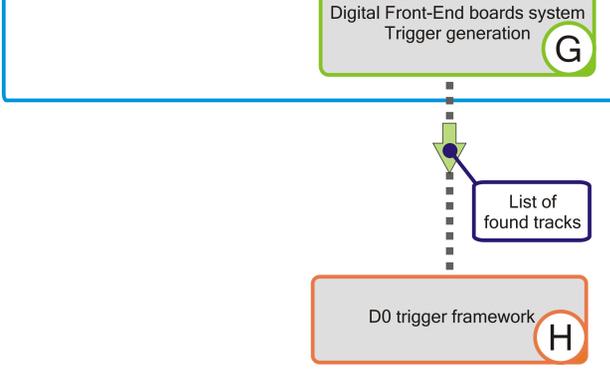
C 40960 clear fibers (data has cylindrical symmetry)



320 LVDS SERDES 371MHz LINKS
Links Throughput: 347 Gigabits per second
Data Throughput: 311 Gigabits per second
Data has cylindrical symmetry



320 LVDS SERDES 371MHz LINKS
Links Throughput: 454 Gigabits per second
Data Throughput: 311 Gigabits per second
Data has azimuthal symmetry



What the Mixer System Does

The Mixer System receives the data from the Analog Front-End boards over 320 Low Voltage Differential Signaling (LVDS) serializer/deserializer (SERDES) links, running at 371 MHz. The input links are of two types. 300 are 21 bits wide and 20 are 28 bits wide. The input data is de-serialized down to 53 MHz by the LVDS receivers, clock/frame re-synchronized and multiplexed in Field Programmable Gate Arrays (FPGAs), and then re-serialized at 371 MHz by the LVDS transmitters. The system has 320 LVDS SERDES output links, all are running at 371 MHz and all are 28 bits wide. Of the 320 output links only 240 carry unique data. The remaining 80 links have replicated data, and are needed to transmit some of the data to more than one DFE system's module. The Mixer System processes 311 Gigabits per second of data, with an input to output delay of 200 nanoseconds. Of this, 48 nanoseconds are used for data deserialization/serialization, and 152 nanoseconds are used for data synchronization and mixing.

Design Constraints

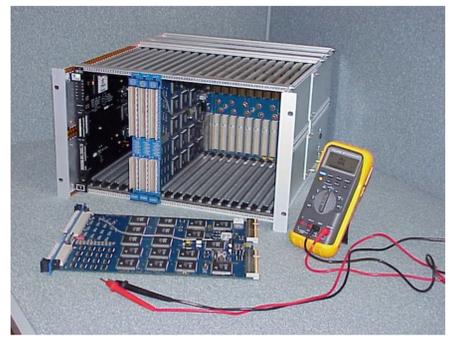
Because the Mixer System was specified as a late addition to a previously designed system, there were many design constraints forced on the system. The most challenging constraints were the limited space available, the restricted access location, the system timing requiring minimal input to output delay, the number of input/output links, the clock/frame resynchronization of the input links data streams. A particular demanding constraint was the already fixed throughput of the Mixer System I/O links, just barely sufficient for the detector's data throughput. Due to limited budget and time available for the project, the specification also called for a custom design with minimal flexibility. Furthermore, the possible flavors of the Mixer board had to be based on the same hardware, so that only one board design would be needed. The fact that the system was to be installed in a limited access area also suggested a need for the capability to remotely run diagnostics and remotely update the system firmware.

Routing 311 Gbit/sec of Data

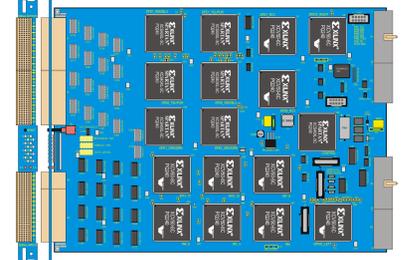
To find a conceptual design solution that would comply with the design specification, a software tool was designed and implemented. The tool is based on Microsoft Excel™ software package and makes extensive use of routines written in Visual Basic™ for Applications (VBA). The tool allows graphical visualization and analysis of the data. It also permits arranging of the data in order to minimize the required number of interconnections between inner elements of the Mixer System to reorganize the data into azimuthal trigger sectors. The tool was also used to decide between possible hardware architectures, and after the architecture was chosen, to generate the portion of VHDL code defining how the system's FPGAs should "mix" data.

The Mixer Subrack

The Mixer System consists of a 21-slot 6U subrack with a custom backplane. The subrack type was an initial constraint resulting from limited rack space available for a new component of the trigger system. The Mixer subrack first slot hosts a custom subrack controller, and the remaining slots host twenty Mixer boards. These twenty Mixer boards can be logically partitioned in five subsystems of four boards. This partitioning matches the fiber detector partitioning in five 72° wide sections or supersectors. This mechanical symmetry allows each supersector to be considered identical from the Mixer System's point of view. Each Mixer subsystem exclusively handles the data of one supersector, and because of detector symmetry, all five subsystems can use the same firmware. A portion of the data received by each of the Mixer boards, needs to be routed to another board in order to be part of the output data stream to which it belongs. The input links to the Mixer System have been arranged in such a way as to limit each Mixer board's data exchange to only the two adjacent boards. Furthermore, the five Mixer subsystems can be considered independent, because no data exchange is needed between them.



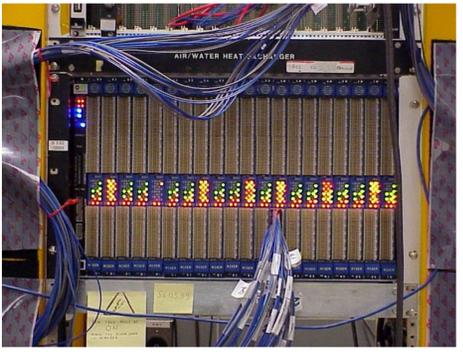
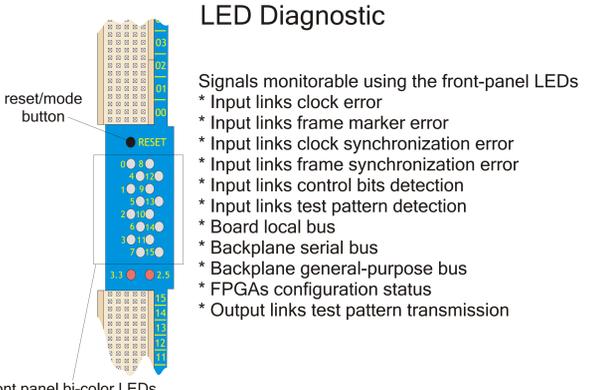
The Mixer Board



The Mixer board uses a total of 17 FPGAs. One FPGA is used as the board controller and is programmed at power-up by an on-board EEPROM. It implements the interface with the custom subrack controller, providing access to board's controls, diagnostics and a means to configure the remaining 16 FPGAs. The FPGA configuration files are stored on a CompactFlash™ memory card hosted by the subrack controller. The system firmware can be updated by replacing the memory card, or when the system is not accessible, downloading the configuration files to the memory card using the subrack controller MIL-STD-1553 interface. Of the 16 remaining FPGAs, 6 are used as the board front-end to perform data clock synchronization and frame realignment, 4 are used to exchange data through the backplane, and 6 as the board back-end to perform the data mixing and drive the output link transmitters. One of the 4 backplane FPGAs is also used as clock controller, and handles the board's clock and frame timing signals. One of the four Mixer boards in each subsystem acts as a timing master, and propagates clock and frame marker signals through the subsystem, allowing synchronous operations.

Onboard Diagnostics

One critical component of a Mixer board is the diagnostic firmware. It allows monitoring input links, clock frequency, frame markers, control bits, clock synchronization, frame alignment and detecting/sending test patterns. The input links test pattern recognition and output links test pattern transmission is used by the trigger system diagnostic to verify the integrity and correctness of the cabling. The Mixer diagnostic is remotely accessible through the MIL-STD-1553 system interface. A simplified version of the diagnostic uses the reset push-button and 16 bi-color LEDs on the Mixer board front panel. This allows the user to view, in real-time, the status of 256 signals and flags, by scrolling through 16 "monitoring modes". The front panel accessible diagnostic has proven to be extremely useful during system testing and installation.



The Mixer System was comprehensively exercised before the commissioning phase using a test system which, aside from a limited data throughput, emulates closely the real data environment.

The system commissioning phase ended in February of 2002, support for system integration is ongoing at D0, and at this time only minor firmware changes are foreseen.

More information about the Mixer System can be found on the web site:
http://www-ese.fnal.gov/D0_CTT_Mixer/
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