

### **Copyright notice**

Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists or to reuse any copyrighted component of this work in other works must be obtained from IEEE (The Institute of Electrical and Electronics Engineers).

IEEE web site: <http://www.ieee.org/>

# Real-Time Data Reorganizer for the D0 Central Fiber Tracker Trigger System at Fermilab

Stefano M. Rapisarda, Neal G. Wilcer, and Jamieson T. Olsen

*Abstract*--A custom digital data Mixer System has been designed to reorganize, in real time, the data produced by the Fermilab D0 Scintillating Fiber Detector. The data are used for the Level 1 and Level 2 trigger decisions. The Mixer System receives the data from the front-end digitization electronics over 320 Low Voltage Differential Signaling (LVDS) links running at 371 MHz. The input data are de-serialized down to 53 MHz by the LVDS receivers, clock/frame re-synchronized and multiplexed in Field Programmable Gate Arrays (FPGAs). The data are then re-serialized at 371 MHz by LVDS transmitters over 320 LVDS output links and sent to the electronics responsible for Level 1 and Level 2 trigger decisions. The Data Mixer System processes 311 Gigabits per second of data with an input to output delay of 200 nanoseconds.

## I. INTRODUCTION

The D0 experiment [1] studies high energy proton anti-proton interactions. The experiment's detector is sited at a high-energy particle accelerator, the Tevatron Collider, at Fermi National Accelerator Laboratory (Fermilab) in Batavia, Illinois, USA. A component of the D0 Detector is the *Central Fiber Tracker (CFT)*. The CFT is constructed of scintillating fibers that are organized together in a very precise array of ribbons, placed onto a structure formed by eight co-axial cylinders. Each cylinder carries an axial doublet layer of fibers parallel to the beam axis and a stereo doublet layer of helically arranged fibers. Only the axial fibers are used for the trigger [3]. The energy deposited into a scintillating fiber by particle interactions is transformed into visible light. The light travels through the scintillating fiber and through an optical (clear) fiber connected to it, reaching a very sensitive light detector, the *Visible Light Photon Counter (VLPC)* [4], hosted in a liquid helium cryostat. The VLPCs are a derivative of solid-state photomultipliers and are used to convert the scintillation light into electrical signals. These are discriminated and digitized by the *Analog Front-End boards (AFEs)* [5]. The Data Mixer System receives the digitized data from the AFEs, then processes and re-organizes it in real-time with minimal delay from cylindrical geometry into 80 azimuthal wedges or

sectors. The restructured data are transmitted to the *Digital Front End board (DFE)* [6, 7] system.

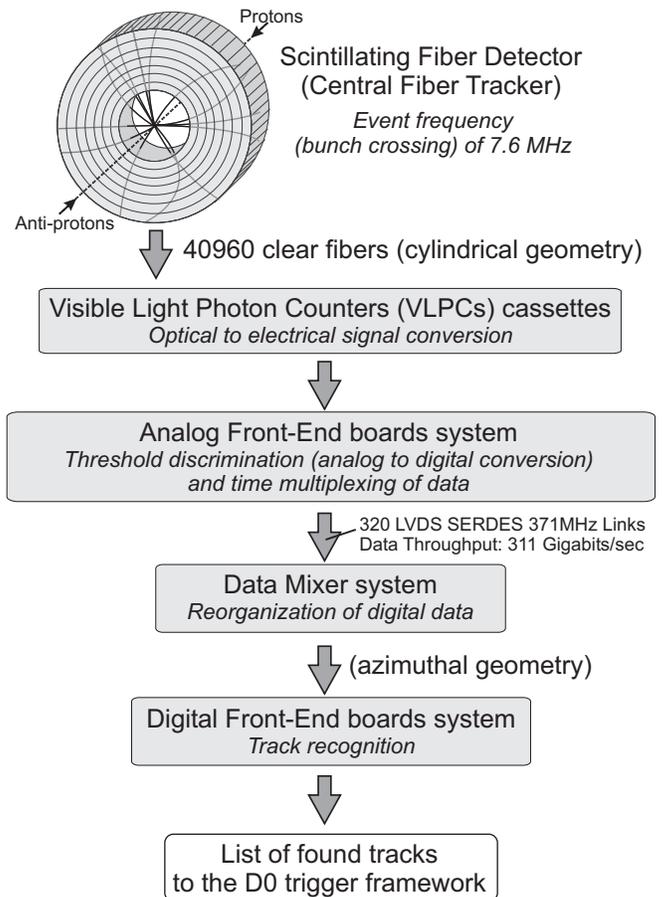


Fig. 1. Block diagram of the D0 Detector Central Fiber Tracker Electronics. Particles generated by proton anti-proton collisions deposit energy on the scintillating fibers where it is transformed into visible light. The light is carried by clear fibers to the Visible Light Photon Counters and converted to electrical signals. These signals are discriminated and digitized by the Analog Front-End boards, reorganized from cylindrical geometry into azimuthal sectors by the Data Mixer System and then used by the Digital Front-End board system for track recognition. Tracks are used for Level 1 and Level 2 trigger decisions.

The DFE system uses the data to detect tracks that are used to contribute to level 1 and level 2 trigger decisions. A block diagram of the D0 Detector CFT electronics is shown in Fig. 1.

Manuscript received December 05, 2002.

S. M. Rapisarda, N. G. Wilcer, and J. T. Olsen are with the Fermi National Accelerator Laboratory, Batavia, IL 60510 USA (e-mail: rapisard@fnal.gov; wilcer@fnal.gov; jamieson@fnal.gov).

The decision to design and build the Data Mixer System was made after all the other Central Fiber Tracker electronics system components were almost in the production phase. The track recognition electronics (Digital Front-End board system) needed to receive the data organized in azimuthal wedges or *trigger sectors*.

One way to address data organization was to physically reorganize the optical fibers prior to the front-end electronics performing the opto-electrical conversion and digitization. The mechanical design of the detector caused unexpected difficulties with this approach. The next best solution was the reorganization of the data after the digitizing process, which led to the design of the Real-Time Data Reorganizer or Data Mixer System [8].

## II. DESIGN REQUIREMENTS

The Data Mixer System was specified as a late addition to a previously designed system, so many design constraints were imposed. The most challenging constraints were the limited space available, the restricted access location, the system timing requiring minimal input to output delay, the number of input/output links, and the clock/frame resynchronization of the input links data streams. A particularly demanding constraint was the already fixed throughput of the Data Mixer System I/O links, just barely sufficient for the detector's data throughput. Due to the limited budget and time available for the project, the specification also called for a custom design with minimal flexibility. Furthermore, the possible flavors of the Mixer board had to be based on the same hardware, so that only one board design would be needed. The fact that the system was to be installed in a limited access area also required the capability to remotely run diagnostics and remotely update the system firmware.

## III. DATA REORGANIZATION

A graphical software tool was designed and written to both find and implement a conceptual solution for reorganizing and transferring data in compliance with the design specification. The tool is based on the Microsoft Excel™ [9] software package and makes extensive use of routines written in Visual Basic™ for Applications (VBA). The tool allows graphical visualization and analysis of the data and its attributes. This capability was used to study the data flow and reorganization. The tool allowed both to reorganize the data into azimuthal trigger sectors and to minimize the required number of interconnections between inner elements of the Data Mixer System. The tool was also used to compare possible hardware architectures, and after the architecture was chosen, to generate the portion of VHDL (Very high speed integrated circuit Hardware Description Language) code defining how the system's FPGAs should operate on the data. This portion of the VHDL code is unique to each FPGA. Due to the large number of data bits (40960 at 7.6 MHz) to be multiplexed, this code is

also the most prone to error, in particular if the code is manually typed. Our automated tool addresses these concerns.

## IV. DATA MIXER SYSTEM DESIGN

The Data Mixer System consists of a 21-slot 6U subrack with a custom backplane [10]. The subrack type was constrained by the limited rack space available for a new component in the Central Fiber Tracker electronics. The first Data Mixer subrack slot hosts a custom controller [7], and the remaining slots host twenty Mixer boards. These twenty Mixer boards can be logically partitioned into five subsystems of four boards each. The partitioning matches the fiber detector partitioning in five 72° wide sections referred to as supersectors. This mechanical symmetry allows each supersector to be considered identical and independent from the Data Mixer System's point of view. Each Mixer subsystem exclusively handles the data from one supersector. Due to the detector symmetry, all five Mixer subsystems can use the same firmware.

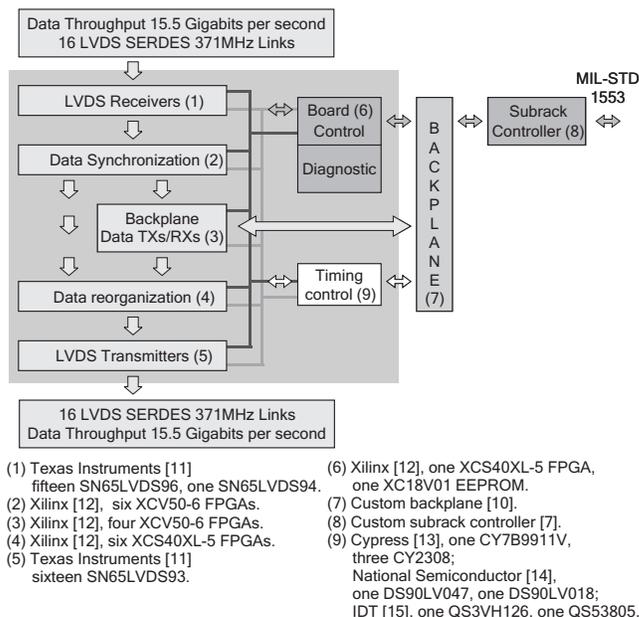


Fig. 2. Block diagram of a Mixer board showing data flow, controls, timing and external communication. A single Xilinx FPGA controls diagnostic and communication with the subrack controller. Timing logic is used to synchronize clocks and frames across an entire Mixer subsystem.

A portion of the data received by each of the Mixer boards needs to be routed to another board in order to be part of the proper output data stream. This is accomplished using point-to-point connections on the custom subrack backplane. The input links to the Data Mixer System have been arranged in such a way as to limit each Mixer board's data exchange to only the two adjacent boards. The backplane design provides for each board to have 41 point-to-point connections to each of the two adjacent boards. These connections are identical for every subrack slot. Furthermore, the five Mixer subsystems can be

considered independent, because no data exchange is needed between them. Therefore, the backplane point-to-point connections crossing supersector boundaries are unused.

### A. Input to output data flow

The Data Mixer System receives the data from the AFE boards over 320 LVDS serializer-deserializer (SERDES) [11] links running at 371 MHz. Each LVDS input link cable is 10 meters [32.8 feet] long. The input links are of two types. 300 are 21 bits wide serialized into four differential pairs (three for the data and one for the clock) and 20 are 28 bits wide serialized into five differential pairs (four for the data and one for the clock). The input data are de-serialized down to 53 MHz by the LVDS receivers, clock/frame re-synchronized and multiplexed in FPGAs, and then re-serialized at 371 MHz by the LVDS transmitters. The system has 320 LVDS SERDES output links, all are running at 371 MHz and all are 28 bits wide. Each LVDS output link cable is 2 meters [6.6 feet] long. Of the 320 output links only 240 carry unique data. The remaining 80 links have replicated data, and are needed to transmit some of the data to more than one DFE module. The replicated data is needed because of track curvature in the magnetic field. This can cause tracks to cross sector boundaries (at most one boundary for tracks above 1.5GeV/c). When this occurs, hits from neighboring sector are needed by a DFE to recognize a track. A block diagram of a Mixer board is shown in Fig. 2. The Data Mixer System processes 311 Gigabits of data per second, with an input to output delay of 200 nanoseconds. Of this, 48 nanoseconds are used for data de-serialization/serialization, and 152 nanoseconds are used for data re-synchronization and mixing.

### B. Data format

At the output of the input links' LVDS receivers the data rate is seven times faster than the D0 detector event frequency (i.e.  $7.6 \text{ MHz} \times 7 = 53 \text{ MHz}$ ).

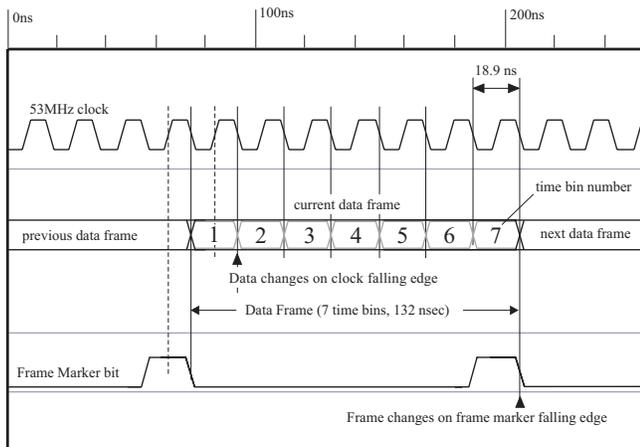


Fig. 3 Timing diagram of the data arriving at the Mixer boards from the AFE boards. The format shown is after the de-serialization process (output of the LVDS receivers).

The data from each event are received in frames that are seven clock periods, or time bins, long as shown in Fig. 3.

Each time bin contains a data word that is 21 or 28 bits wide, depending on the type of link. The Least Significant Bits in each word in a frame are used as the frame marker signal. This signal is set high to specify when a data frame ends separating data belonging to different events. Data bits have the same naming convention used for the detector fibers and each data bit has a specific position assigned in both the input and output data streams. The time bin assigned to any data bit in an input data frame is preserved in the output data frame. The data reorganization process performed by the Data Mixer System is repeated continuously for each set of input frames carrying the 40960 data bits belonging to each event.

### C. Timing and synchronization

In order to correctly handle the data it is essential that every component of a Mixer subsystem operate synchronously using a common clock and frame marker source. In normal operations the Mixer subsystem uses as reference the clock and the frame marker of the first input link (link#0) on the leftmost board.

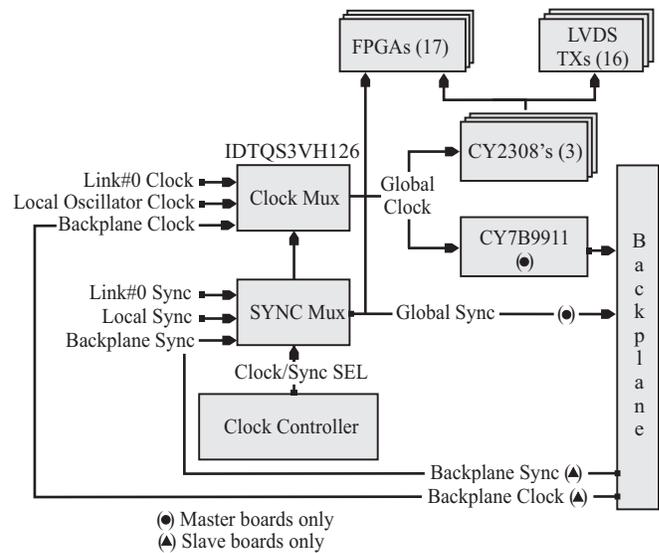


Fig. 4 Mixer board clock and frame marker distribution. Each board has logic to choose from more than one clock source. In normal operations the timing reference for a Mixer subsystem is the input link #0 of the leftmost board (master). The master board propagates the clock and frame marker over the backplane to the other three "slave" boards in the subsystem. The master board uses a Cypress programmable skew clock buffer CY7B9911 to distribute the clock to the slave boards. Three Cypress CY2308 zero delay buffers are used for on-board clock distribution to the seventeen FPGAs and sixteen LVDS transmitters. An IDTQS3VH126 analog switch is used as clock multiplexer.

This leftmost board acts as timing "master" and distributes the clock and frame marker over the backplane to the other three "slave" boards in the subsystem. Each board has logic to verify the validity of the clock and frame marker and the

capability to use a different timing source if the primary source fails. The timing distribution is represented in Fig. 4.

A master board can choose between two possible timing references, input link number 0 or local (on-board oscillator and frame marker generator). A slave board has three choices, in order of priority: backplane timing from master board, input link number 0 and local.

The reasons for multiple timing references are to both facilitate the testing when not all the links are connected and to allow the slave boards to continue operating in case the master board fails. Besides being a backup timing reference, the on-board oscillator is used by the on-board diagnostics and control logic to guarantee continuous operations.

#### D. Data Pipelining

The Data Mixer System operation relies heavily on data pipelining. Each component of the system progressively operates on the data flowing through it without waiting for all the data of an event to be received (see Fig. 5). The data are first synchronized to a common clock reference by the input FPGAs. The data are then routed to the backplane and output FPGAs through the interconnection network hardwired in the printed circuit board. The backplane driver FPGAs multiplex the data to be sent to the adjacent boards where the data are multiplexed again by the backplane receivers and then routed to the output FPGAs. The output FPGAs reorganize the data before sending them to the output links' LVDS transmitters.

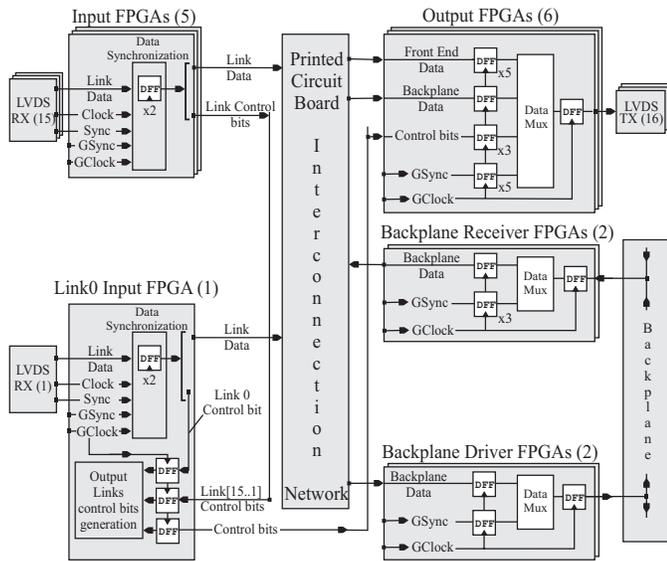


Fig. 5 Block diagram showing data pipelining in a Mixer board. Input data are synchronized in the input FPGAs, routed to output and backplane FPGAs. Backplane FPGAs perform some data multiplexing and are used for data exchange with adjacent boards. Output FPGAs are dedicated to data reorganization before transmission through the LVDS output links.

Each input link also carries control bits that are routed to one of the input FPGA and used to generate the output links

control bits. No control bits are exchanged between boards. Components of the data pipelining chain use the frame marker signal as timing reference to determine how the data should be multiplexed at a particular time (i.e. clock edge).

#### V. EMBEDDED DIAGNOSTICS

Embedded diagnostic firmware proved to be a crucial component of the Data Mixer System [16]. It allows monitoring of the status of several critical parameters of the input links: clock frequency, frame markers, control bits, clock synchronization, frame synchronization, and detection of test patterns. The diagnostic also provides monitoring of the board's local bus, the backplane serial and parallel buses, the FPGAs configuration status, the testing of the front panel LEDs, the transmission of test patterns and simulated events on the output links.

The capability of the Data Mixer System to recognize and transmit test patterns is used by the Central Fiber Tracker electronics diagnostic to verify the integrity and correctness of the cabling. The transmission of user definable events is utilized to test the Digital Front-End board system for track recognition and the D0 Trigger framework for trigger decisions.

The Mixer diagnostic is remotely accessible through the MIL-STD-1553 system interface.

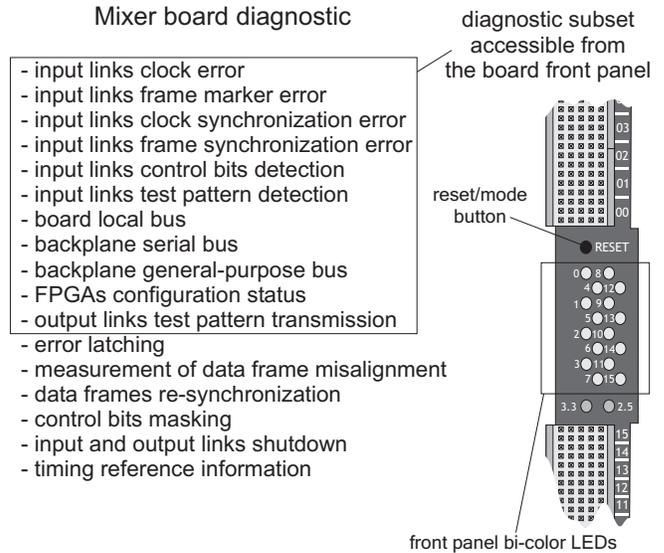


Fig. 6 Mixer Board diagnostic. The diagnostic is accessible through the subrack controller interface. A subset of the diagnostic information is accessible from the Mixer board front panel. A dual function push-button allows the user to reset the board and also to select one of the 16 sets of signals to be displayed via the front panel LEDs.

A simplified version of the diagnostic uses the reset/mode push-button and 16 bi-color LEDs on the Mixer board front panel. This allows the user to view, in real-time, the status of

256 signals and flags by scrolling through 16 sets of signals or "monitoring modes". The reset/mode button has a dual function, when pressed for more than two seconds it resets the board, otherwise it is used to scroll through the monitoring modes selecting which set of signals is to be displayed on the 16 LEDs. When the monitoring mode is changed, only one of the front panel LEDs is briefly turned on to show the active mode number. Each bi-color LED is a red and a green LED in the same package. The red LED is driven by the signal to be monitored and the green LED by the same signal negated. Both of them are stretched to have a minimum duration of 150 msec in order to be visible to the human eye.

The front panel accessible diagnostic uses minimal space/resources, does not require any external interface to check a large number of signals and flags and has proven to be extremely useful during system testing and commissioning.

A list of the diagnostic capabilities of the Mixer System along with the diagnostic subset accessible from the front panel is shown in Fig. 6.

## VI. DATA MIXER SYSTEM CONFIGURATION

One of the 17 FPGAs on each mixer board acts as the board controller and is automatically configured at power-up by an on-board EEPROM. The EEPROM contents are modifiable through a front panel JTAG (IEEE Std 1149.1) interface port. The board controller interacts with the subrack controller and handles the configuration of the remaining 16 FPGAs.

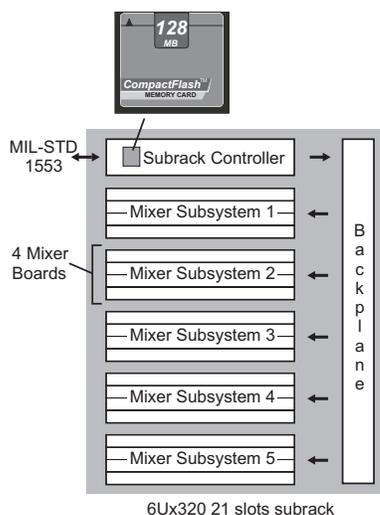


Fig. 7 Data Mixer System configuration. A CompactFlash memory card on the subrack controller stores the configuration files for the Mixer system FPGAs. On power-up, the subrack controller automatically downloads the FPGA configuration files using a "broadcast" mode of communication where each Mixer subsystem is configured simultaneously.

The FPGAs configuration files are stored on a removable CompactFlash™ memory card [17] on the subrack controller. Taking advantage of the fact that each of the five Mixer

subsystems uses the same firmware, the configuration stream is downloaded simultaneously to all subsystems reducing the required configuration time by eighty percent. At power-up the configuration time for the full Data Mixer System is 30 seconds.

## VII. PRINTED CIRCUIT BOARD DESIGN

The Data Mixer System's input and output LVDS links operate at 371 MHz. The data flowing through the board is clocked at 53 MHz. Careful attention has been given to signal layout and layer stackup.

The 371 MHz differential LVDS signals were hand routed on inner layers and kept separate from the 53 MHz signals. Impedance was controlled using the edge coupled symmetrical dual stripline technique where differential signals are routed next to each other with plane layers above and below. The distance between the differential traces was calculated to result in an impedance of 100 Ω. Additionally, 100 Ω terminators were installed at the end of these traces near the LVDS receiver ICs.

The 53 MHz signals were routed using symmetrical striplines on the inner signal layers and microstrips on the outer signal layers. All the signal traces were designed to have an impedance of 50 Ω relative to the plane layers above and below each signal layer. Clocks and other critical signals were hand routed. AC termination was used on all clock signals and bypass capacitors were used throughout the board in accordance with each IC manufacturer's recommendation.

## VIII. TESTING THE DATA MIXER SYSTEM

Data Mixer System testing has been a necessary step to solve assembly problems, verify system performance and timing, and guarantee error free operation. The testing went through three phases.

### A. Intra-board connectivity

The first phase of testing was a connectivity test that verified the trace and solder connections between all of the FPGAs and their auxiliary logic. This portion of the test was done using Corelis™ [18] boundary scan software that allows the user to access and test the I/O interconnects with a JTAG capable device.

### B. Data transfer accuracy

The second phase of testing involved verification of the data paths, the reorganization algorithms, and timing. Because the Data Mixer System can be logically partitioned into five independent and identical subsystems, a subsystem of four adjacent Mixer boards was used for this phase of testing.

A custom test-board called the *Datapump* [7] was used to exercise the Mixer subsystem input links with test patterns and analyze the Mixer subsystem output links. The Datapump test-board was connected to a host computer's parallel port and controlled by a user interface based on MS Excel™ [19]. This test system allowed comparing the data transmitted on the Mixer subsystem output links with the software-generated expected data and to verify Mixer board diagnostic functionality.

### C. In-situ testing

Final testing was done during commissioning at the D0 experiment site in the Data Mixer System subrack installed on the D0 detector platform. Tests included verification of input/output links cabling using the Mixer test pattern detection/transmission capability and frame timing/synchronization using the Data Mixer System diagnostic.

## IX. CONCLUSION

The Data Mixer System was installed in November of 2001. The system has proven reliable and accurate. The Data Mixer System diagnostics have played an important role in solving issues during Central Fiber Tracker electronics integration and are currently used by the D0 experiment online software to continuously monitor CFT system performance.

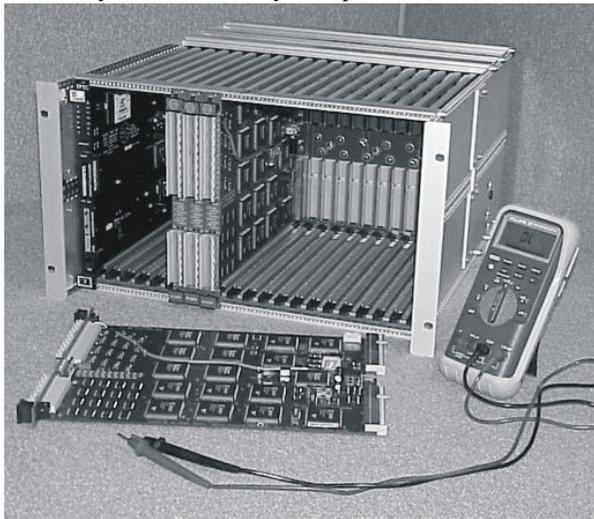


Fig. 8. The Mixer subrack showing the custom backplane, three Mixer boards, and a subrack controller installed. The digital multi-meter is shown for size reference.

## X. ACKNOWLEDGMENT

The authors would like to thank J. Anderson, R. Angstadt, F. Borcharding, B. Haynes, D. Husby, J. Smith, and M. Vaz for major contributions to the design of the Data Mixer System; S. Bledsoe, J. Chromowicz, S. Grünendahl, G. Ginther, S. Lynn, P. Rubinov, and M. Tomoto for their invaluable help in the

assembly, debugging, and commissioning of the Data Mixer System.

## XI. REFERENCES

- [1] D0 Experiment at Fermi National Accelerator Laboratory, Batavia, Illinois. URL: <http://www-d0.fnal.gov/>
- [2] DØ Collaboration, "The DØ Upgrade: The Detector and Its Physics", Fermilab *Pub-96/357-E*, 1996. [Online]. Available: <http://higgs.physics.lsa.umich.edu/dzero/d0doc96/d0doc.html>
- [3] DØ Collaboration, "The DØ Upgrade Central Fiber Tracker, Technical Design Report", Fermilab. [Online]. Available: [http://d0server1.fnal.gov/projects/scifi/cft\\_home.html](http://d0server1.fnal.gov/projects/scifi/cft_home.html)
- [4] M. Adams, N. Amos, D. A. Averill, P. Baringer, Chung M., F. Hsieh et al. "A Detailed Study of Plastic scintillating Strips with Axial Wavelength Shifting Fiber and VLPC Readout", *Nucl. Instrum. And Meth.*, A366, pp.263-277, 1995.
- [5] J.Anderson, "D-Zero Central Fiber Tracker 8-MCM Analog Front-End Board, Design Specification". [Online]. Available: [http://d0server1.fnal.gov/users/janderson/Public\\_Eng\\_Notes/default.html](http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/default.html)
- [6] J.Anderson, F.Borcharding, S.Grünendahl, H.Johnson, J.Olsen, M.Martin, Y.Kin, "A high rate digital processing board for the D0 Upgrade", 11th IEEE NPSS Real Time Conference, Santa Fe, New Mexico, 1999.
- [7] J.T.Olsen, Technical Documentation. [Online]. Available: <http://d0server1.fnal.gov/users/jamieson/www/index.html>
- [8] N.G.Wilcer, S.M.Rapisarda, "Central Tracker Trigger (CTT) Mixer System". [Online]. Available: [http://www-ese.fnal.gov/D0\\_CTT\\_Mixer/](http://www-ese.fnal.gov/D0_CTT_Mixer/)
- [9] Microsoft, Seattle, Washington. URL: <http://www.microsoft.com/>
- [10] N.G.Wilcer, S.M.Rapisarda, "Central Tracker Trigger (CTT) Mixer System, Backplane Description & Power Distribution Specification". [Online]. Available: [http://www-ese.fnal.gov/D0\\_CTT\\_Mixer/](http://www-ese.fnal.gov/D0_CTT_Mixer/)
- [11] Texas Instruments Inc., Dallas, Texas. URL: <http://www.ti.com/>
- [12] Xilinx, San Jose, CA. URL: <http://www.xilinx.com/>
- [13] Cypress, San Jose, California. URL: <http://www.cypress.com/>
- [14] National Semiconductor, Santa Clara, California. URL: <http://www.national.com>
- [15] IDT, Santa Clara, California. URL: <http://www.idt.com/>
- [16] N.G.Wilcer, S.M.Rapisarda, "Central Tracker Trigger (CTT) Mixer System, Diagnostic Procedures". [Online]. Available: [http://www-ese.fnal.gov/D0\\_CTT\\_Mixer/](http://www-ese.fnal.gov/D0_CTT_Mixer/)
- [17] Sandisk, Sunnyvale, California. URL: <http://www.sandisk.com/>
- [18] Corelis Inc., Cerritos, California. URL: <http://www.corelis.com/>
- [19] R.D.Angstadt, F.Borcharding, M.E.Johnson, L.Moreira, "Using Modern Software Tools to Design, Simulate and Test a Level 1 Trigger Sub-System for the DZero Detector". *D0 note 2589*. [Online]. Available: <http://d0server1.fnal.gov/users/angstadt/www/d0notes.htm>