Test Waveform Generator System
Fermilab December 11th, 2003

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TWG Prototype System status

Software:

-) No relevant changes to report.

Hardware:

-) Added SCL interface in order to get the system synchronized for future tests.
   a) Manufactured passive adapter to connect Xilinx Test card and SCL receiver.
   b) Modified Xilinx card firmware to allow for adapter connection.

Work in progress:

-) Modification of Xilinx firmware to use SCL timing for triggering.
-) Implementation of filtering (in the amplification stages) to limit bandwidth of output signals [Report Nov 13 2003].
-) Investigating improvements of the system clock (currently 40 MHz) [Report Oct 30, 2003].
-) Documentation/web page updates.

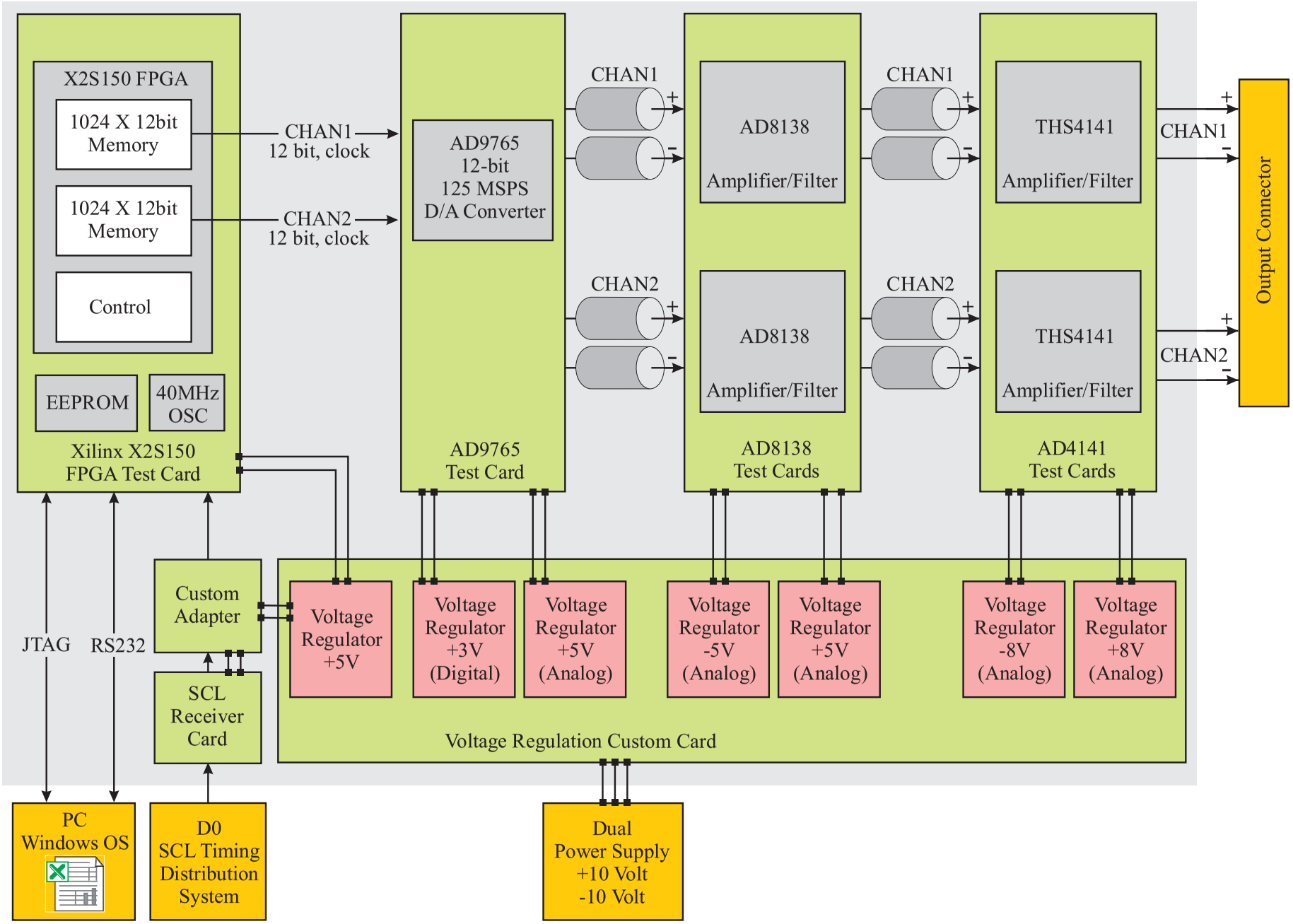
TWG System

Work in progress on:

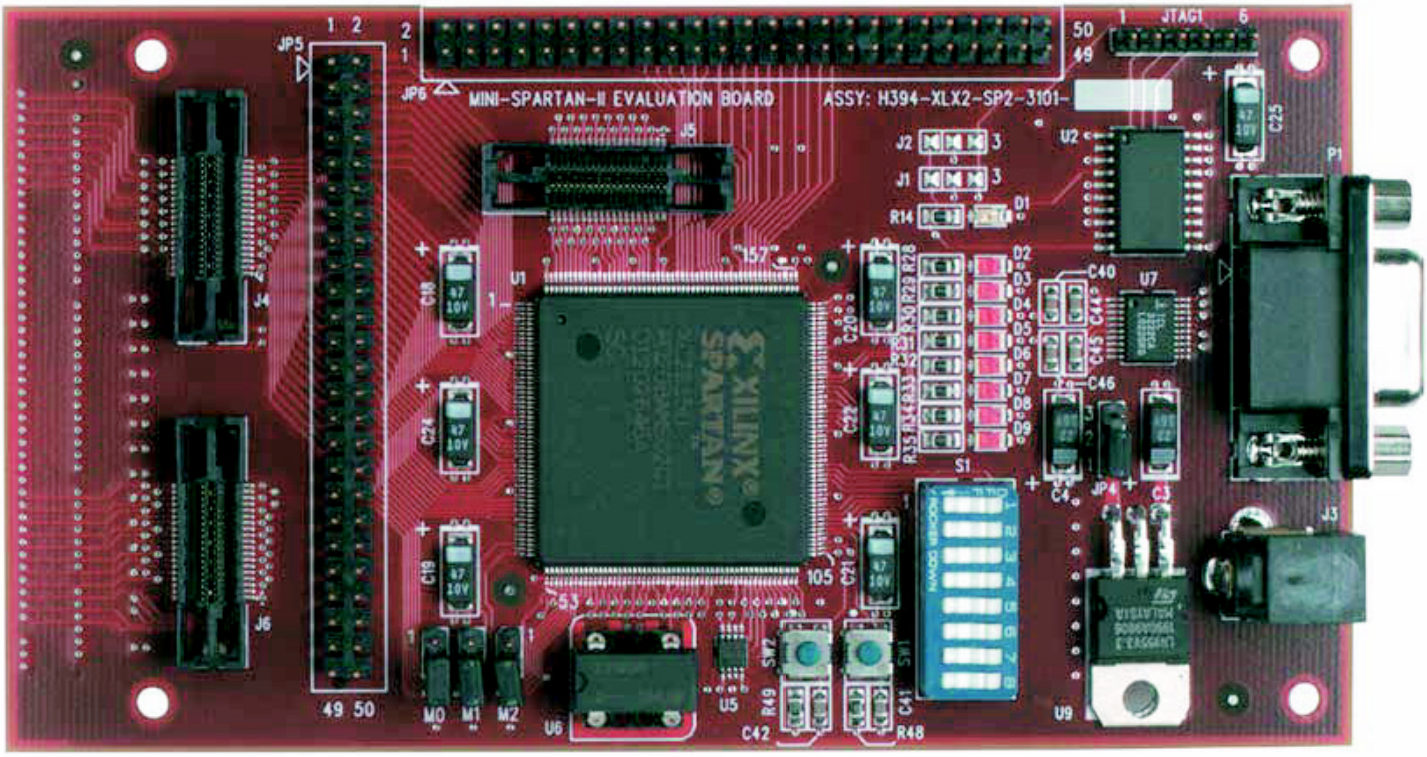
-) Specification proposal.
   Comments and ideas are very welcome [Report Nov 13 2003].

TWG Documentation (including this report):

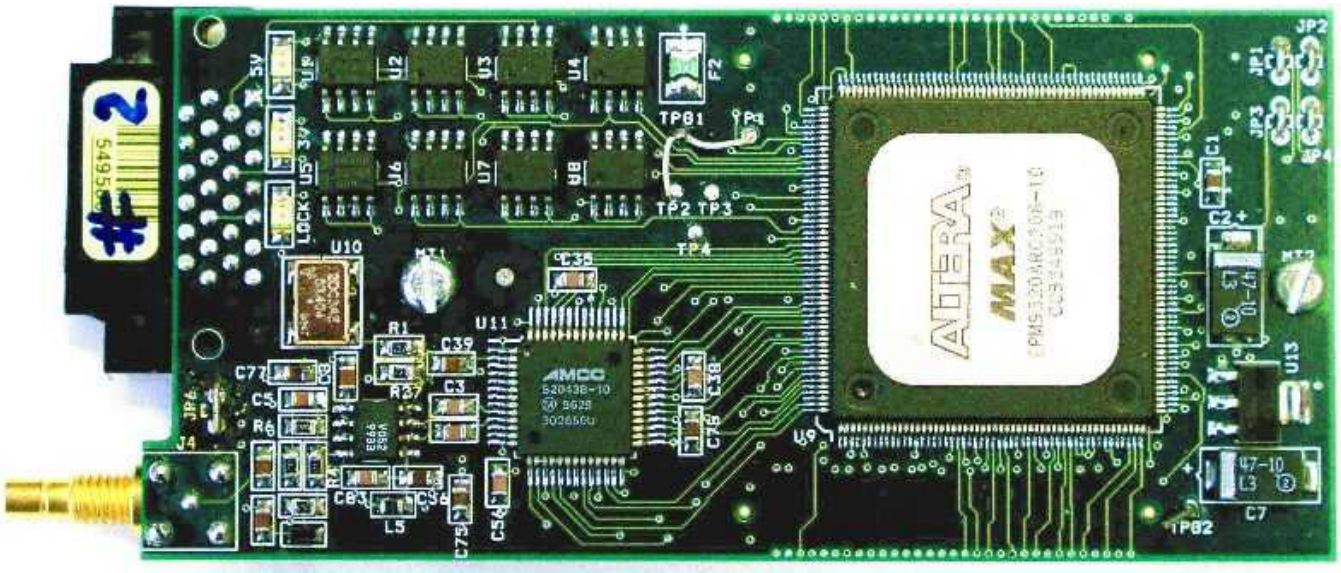
http://www-ese.fnal.gov/D0Cal_TWG/


X2S150 FPGA
1024 X 12bit Memory
1024 X 12bit Memory
Control
EEPROM
40MHz OSC
Xilinx X2S150 FPGA Test Card
CHAN1 12 bit, clock
CHAN2 12 bit, clock
AD9765 12-bit 125 MSPS D/A Converter
AD9765 Test Card
CHAN1
CHAN2
AD8138 Amplifier/Filter
AD8138 Amplifier/Filter
AD8138 Test Cards
THS4141 Amplifier/Filter
THS4141 Amplifier/Filter
AD4141 Test Cards
CHAN1
CHAN2
Output Connector
JTAG
RS232
Custom Adapter
SCL Receiver Card
Voltage Regulator +5V
Voltage Regulator +3V (Digital)
Voltage Regulator +5V (Analog)
Voltage Regulator -5V (Analog)
Voltage Regulator +5V (Analog)
Voltage Regulator -8V (Analog)
Voltage Regulator +8V (Analog)
Voltage Regulation Custom Card
PC Windows OS
D0 SCL Timing Distribution System
Dual Power Supply +10 Volt -10 Volt

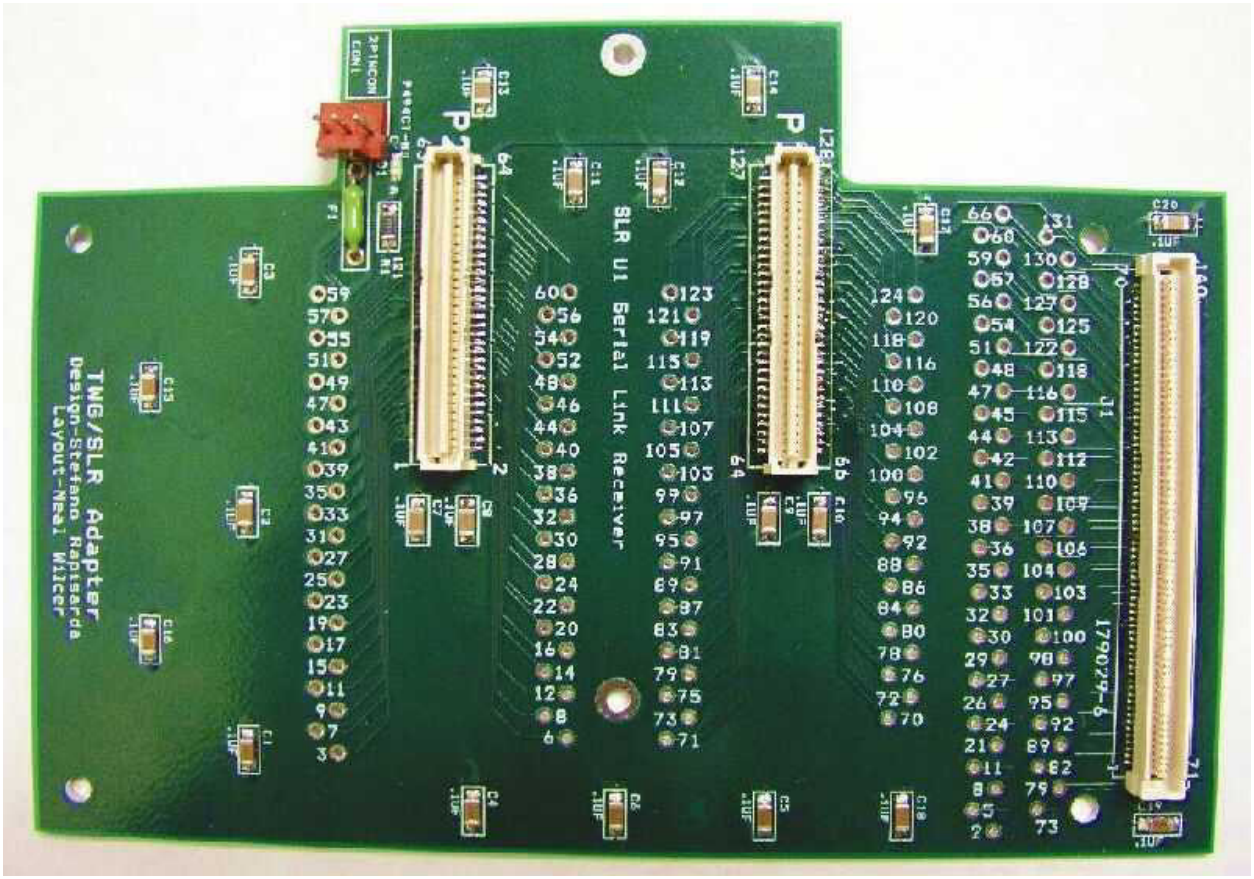
Xilinx Test Card



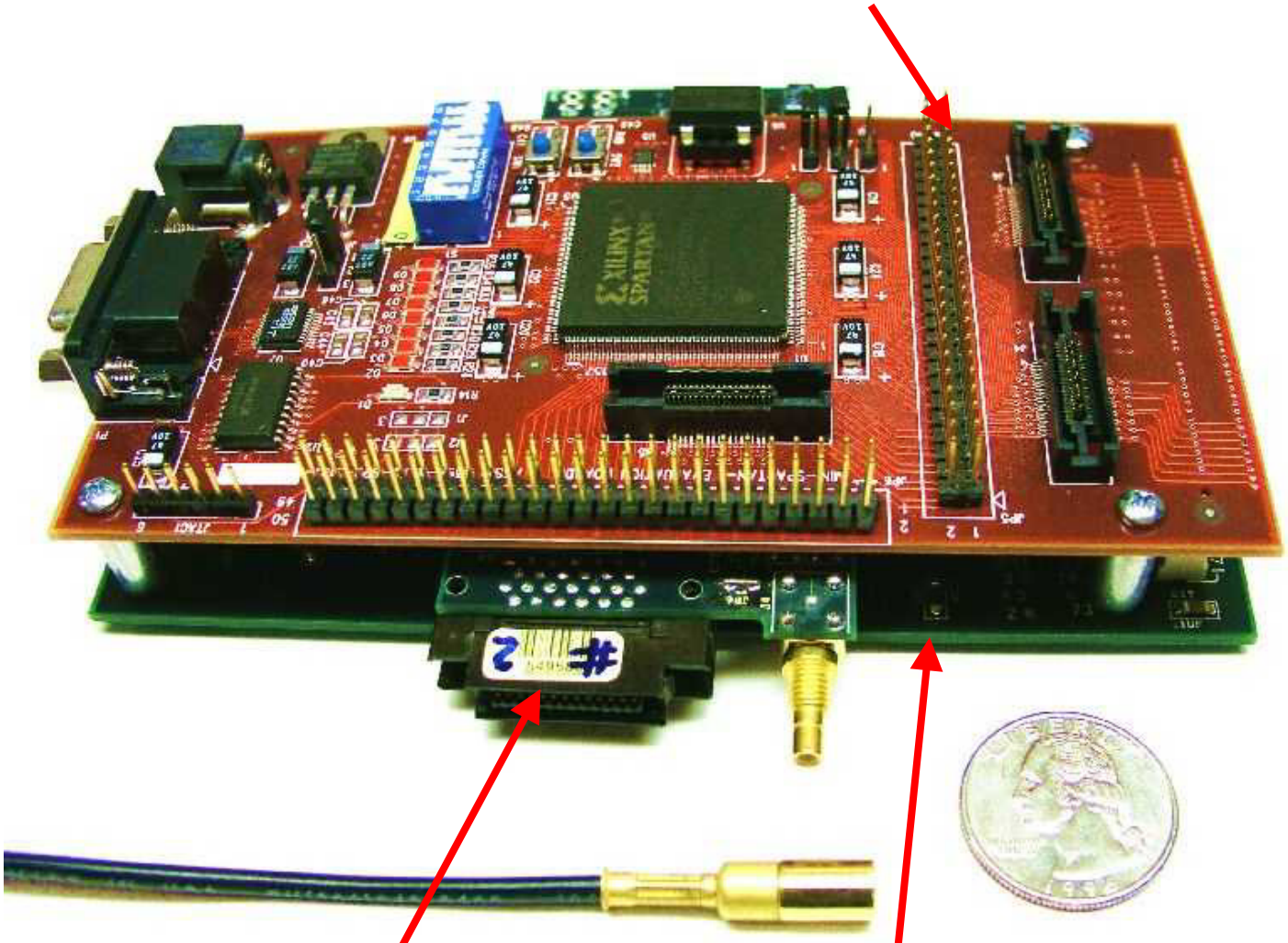
SCL receiver



SCL Passive Adapter



Xilinx Test card



SCL Receiver

SCL Passive Adapter