

**Fermi National Accelerator Laboratory**

**D-Zero Detector Calorimeter Electronics  
Run II b Upgrade Project**

**Test Waveform Generator System  
System Specification**

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## 1 Introduction

This document specifies the Test Waveform Generator System (TWG) [Ref.1]. The TWG is part of the electronics of the D-Zero detector Calorimeter Trigger Test System at Fermilab. More information on the experiments performed at Fermilab is available on the laboratory web page:

<http://www.fnal.gov/>

More information on the D0 Detector is available on:

<http://www-d0.fnal.gov/>

The designers welcome suggestions and corrections [Ref.22], which can be addressed directly to the engineer responsible of the project. Contact information is available on the Electronics System Engineering (ESE) web page:

<http://www-ese.fnal.gov/>

More information and documentation on the Test Waveform Generator Project are available on:

[http://www-ese.fnal.gov/D0Cal\\_TWG/](http://www-ese.fnal.gov/D0Cal_TWG/)

## 2 Overview

The Test Waveform Generator (TWG) [Ref.1] is a system used for testing some components of the D0 Calorimeter Level 1 Trigger electronics (see Paragraph 9, page 29). The TWG has been assembled using a commercial one-channel “arbitrary waveform generator”, a commercial switch (multiplexer) system and a custom VME 64 [Ref.20] transition module.

### 2.1 System Under Test - The D0 calorimeter Level 1 Trigger System

The main purpose of the TWG is to test the ADF cards/system (see Paragraph 9, page 29). Figure 2.1 briefly describes the ADF system and its interfaces. The TWG will not be a part of the D0 Trigger system but will be used only to verify performance and functionality of the ADF cards in a separate test environment. Besides emulating the signals produced by the Baseline Subtractor System (BLS) the TWG is able to generate arbitrary waveforms that can be used to measure the characteristics of the ADF’s analog input stage.

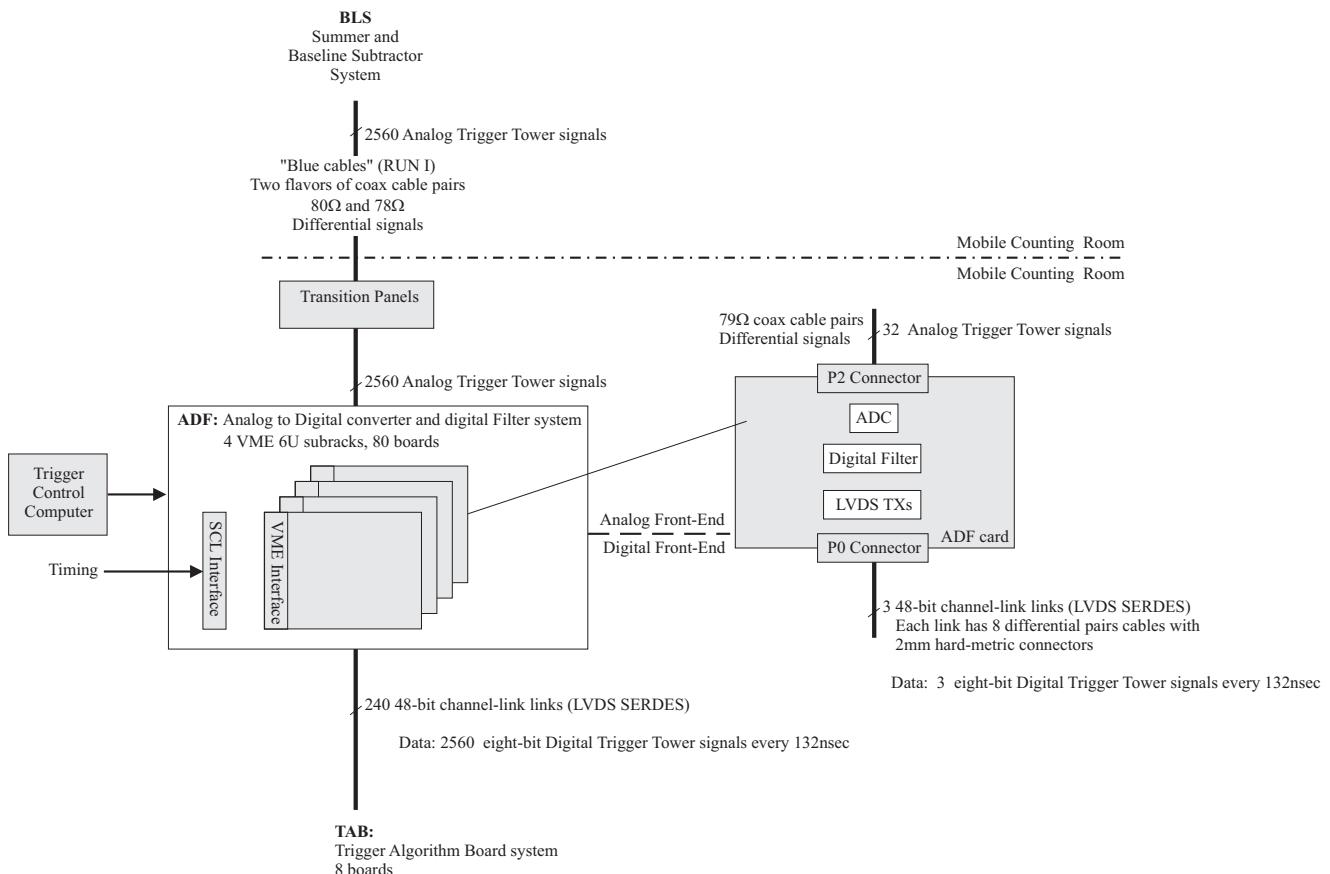


Figure 2.1, Block diagram of the ADF section on the L1 trigger system

The TWG system is used to test only one ADF card at a time. The TWG can be controlled from a PC using RS-232 [Ref.15] and/or IEEE-488 (GPIB, HPIB) [Ref.5].

### 3 Test Waveform Generator system

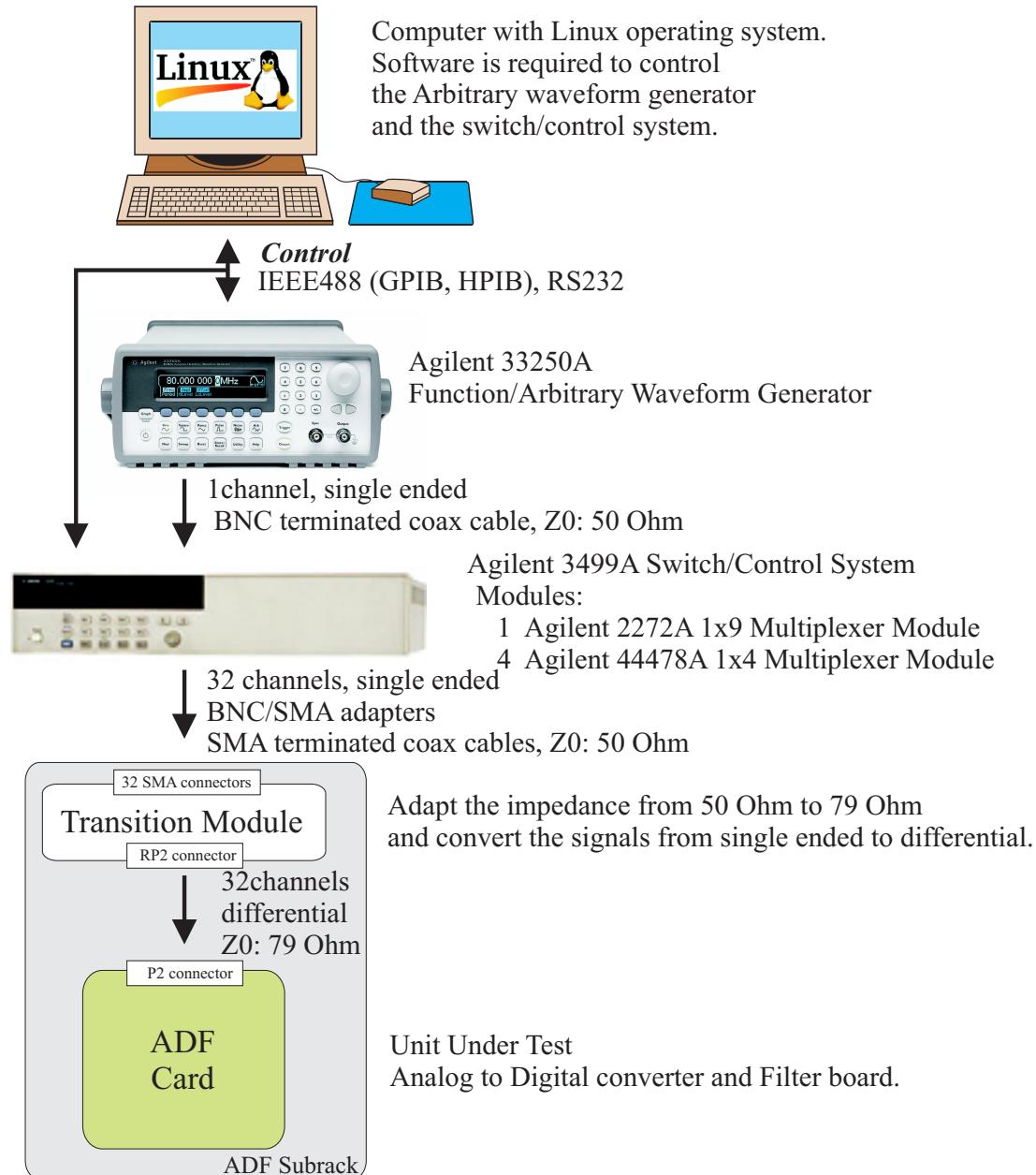


Figure 3.1, Test Waveform Generator system.

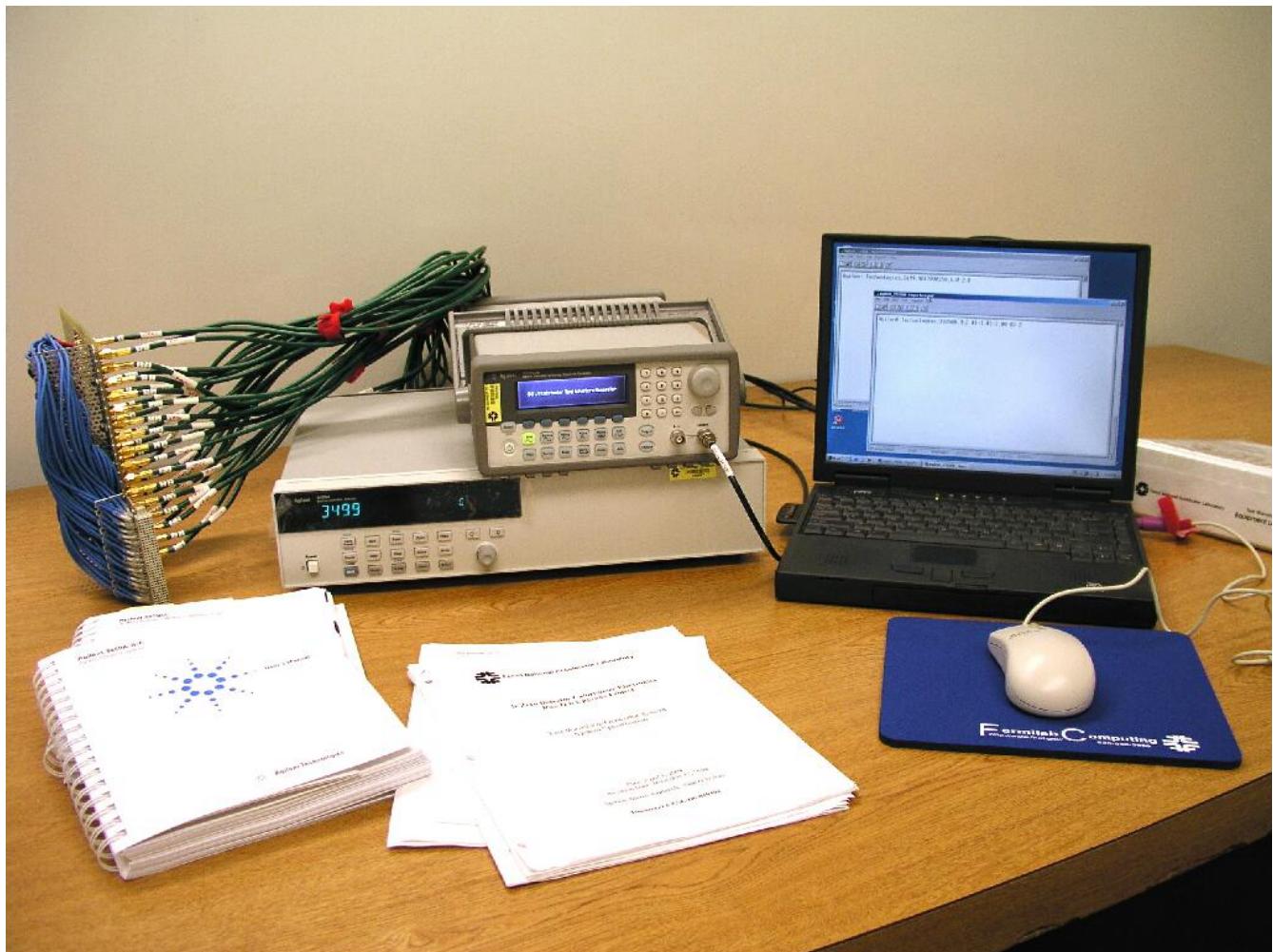


Figure 3.2, Test Waveform Generator system.

### 3.1 Computer

#### 3.1.1 Minimum Requirements

Interface ports to control the TWG system: GPIB I/O or RS-232 (2 ports).

### 3.2 Arbitrary Waveform Generator

One Arbitrary Waveform Source: *Agilent 33250A* [[Ref.3](#)]



Figure 3.3, Agilent 33250A Function/Arbitrary Waveform Generator

The Agilent 33250A Function/Arbitrary Waveform generator uses direct digital synthesis to create output waveform down to 1 uHz frequency resolution.

#### *Waveforms*

80MHz sine and square wave outputs

50MHz pulse waveform with variable rise/fall times

12-bit, 200Msa.s, 64K-point deep arbitrary waveform.

#### *Output characteristics*

Signal source impedance: 50 Ohm

Amplitude (into 50 Ohm): 10 mV<sub>pp</sub> to 10 V<sub>pp</sub>

#### *Interfaces*

IEEE-488 (GPIB, HPIB) [[Ref.6](#)]

RS232 [[Ref.15](#)]

#### *Power Supply*

100-240 VAC, 50-60Hz

100-127 VAC, 50-400Hz

Power consumption: 140 VA

### 3.3 Switch System

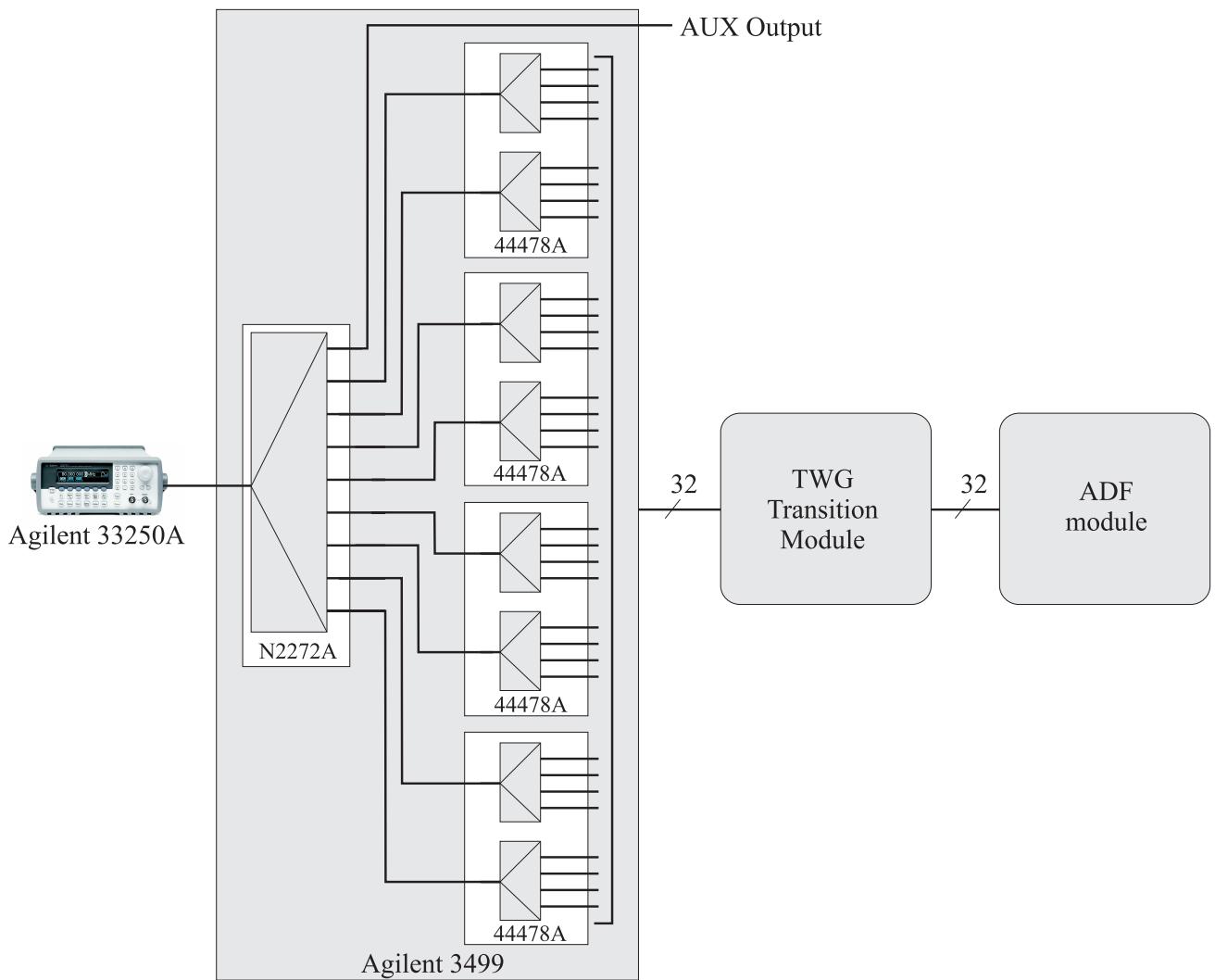


Figure 3.4, Switch system diagram

#### 3.3.1 Mainframe

*Agilent 3499A* [\[Ref.3\]](#) Switch/Control System, 5 slot mainframe



Figure 3.5, Agilent 3499A Switch/Control System

*Interfaces*

IEEE-488 (GPIB, HPIB) [\[Ref.6\]](#)

RS232 [\[Ref.15\]](#)

*Power Supply*

100-240 VAC, 50-60Hz

100-127 VAC, 50-400Hz

Power consumption: 40 VA maximum

**3.3.2 1x9 Multiplexer module*****Agilent N2272A*** [Ref.3], 1 GHz 1x9 RF Multiplexer Module

Insertion loss (100MHz): &lt;0.5 dB

Cross talk (100MHz): &lt;-75dB

SWR (100MHz): &lt;1.20

Bandwidth: 1.0 GHz

Characteristic impedance: 50 Ohm

Signal delay: 2.5 nsec

Initial channel closed resistance: 0.8 Ohm

Connector: BNC

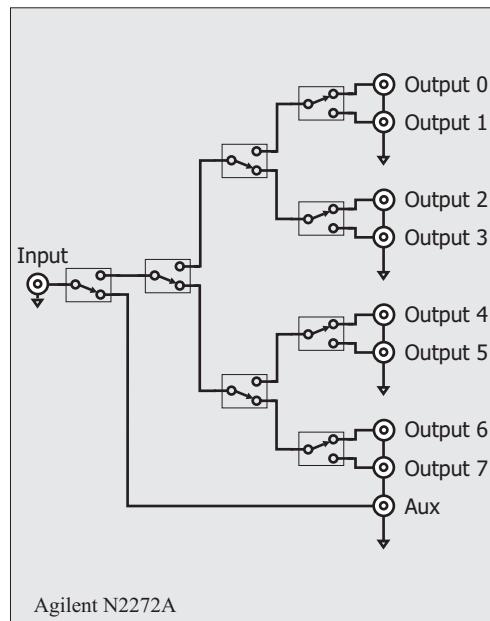


Figure 3.6, N2272A multiplexing diagram

### 3.3.3 1x4 Multiplexer module

**Agilent 44478A** [Ref.3], Dual 1x4 RF Multiplexer(1.3GHz, 50 Ohm)

Insertion loss (100MHz): <0.7 dB

Cross talk (100MHz): <-80dB

SWR (100MHz): <1.25

Bandwidth: 1.3 GHz

Characteristic impedance: 50 Ohm

Signal delay: 3 nsec

Initial channel closed resistance: 1 Ohm

Connector: BNC

Off-channels termination: Yes

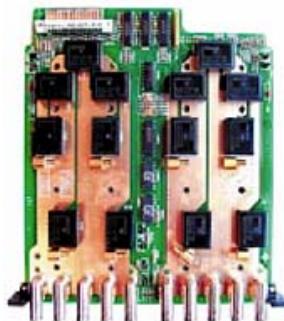


Figure 3.7, Agilent 44478A Dual 1x4 VHF Multiplexer

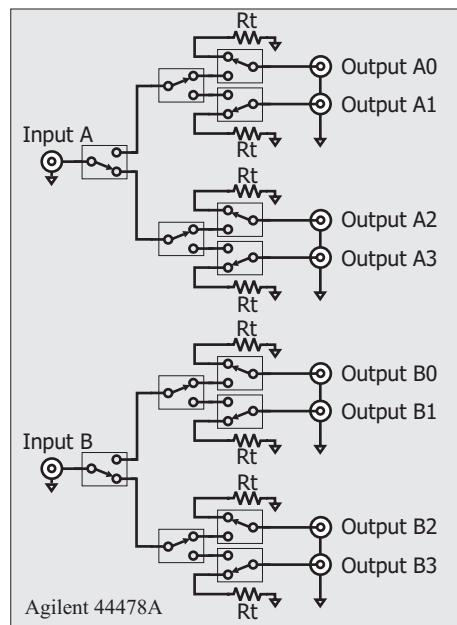


Figure 3.8, 44478A multiplexing diagram

### 3.4 Custom VME 64 Transition Module

A detailed description of the transition module is given in paragraph 4.

## 4 Custom VME 64 Transition Module

A custom VME 64 Transition Module [Ref.10, 20] has been designed to interface the waveform generation and switching components of the TWG system with the ADF system.

### 4.1 Specifications

The module complies with the VME64 [Ref.20] and IEEE 1101.11 [Ref.10] transition module specifications. The module follows the in-line configuration, this means that it will be mechanically coplanar with the front plug-in unit (ADF card).

It has 32 inputs, one for each of the ADF analog input channels.

The module converts single ended signals to differential using transformers; the output impedance is then matched to the input stage of the ADF.

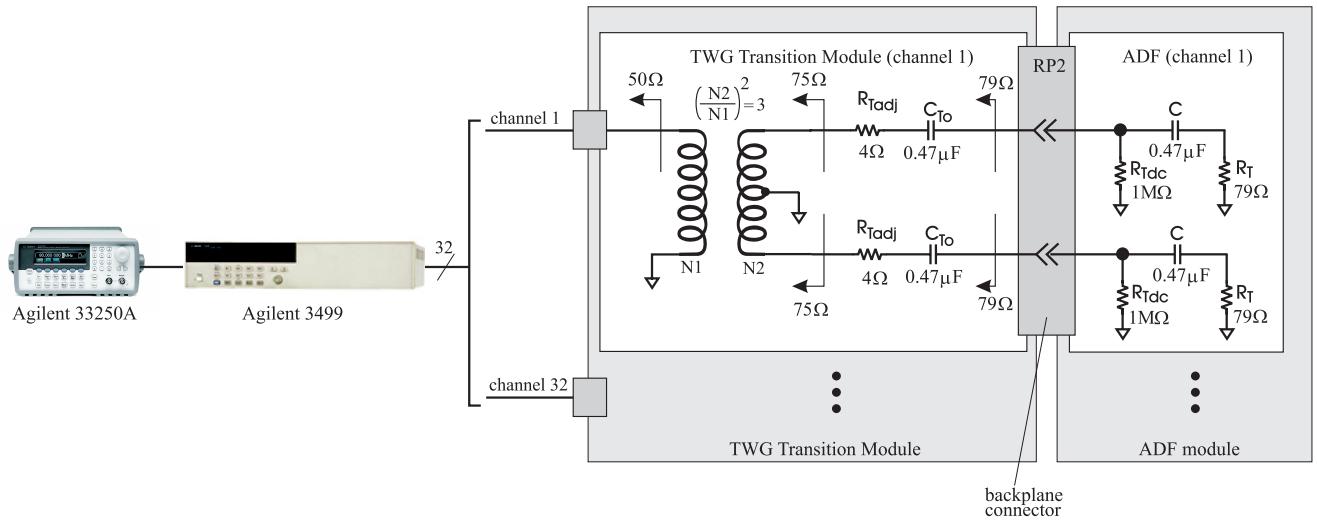


Figure 4.1, ADF Interfacing diagram

### 4.2 Interfaces

Input interface: 32 SMA jack receptacle connectors.

Output interface: VME64 transition module RP2 connector.

### 4.3 Monitoring and diagnostic features

A VME 6U module is provided to allow for verification of TWG system functioning.

#### 4.3.1 Power supply

The TWG transition module is a passive module and no power supply is needed.

#### 4.4 Appendix D - TWG Transition Module Components and Layout

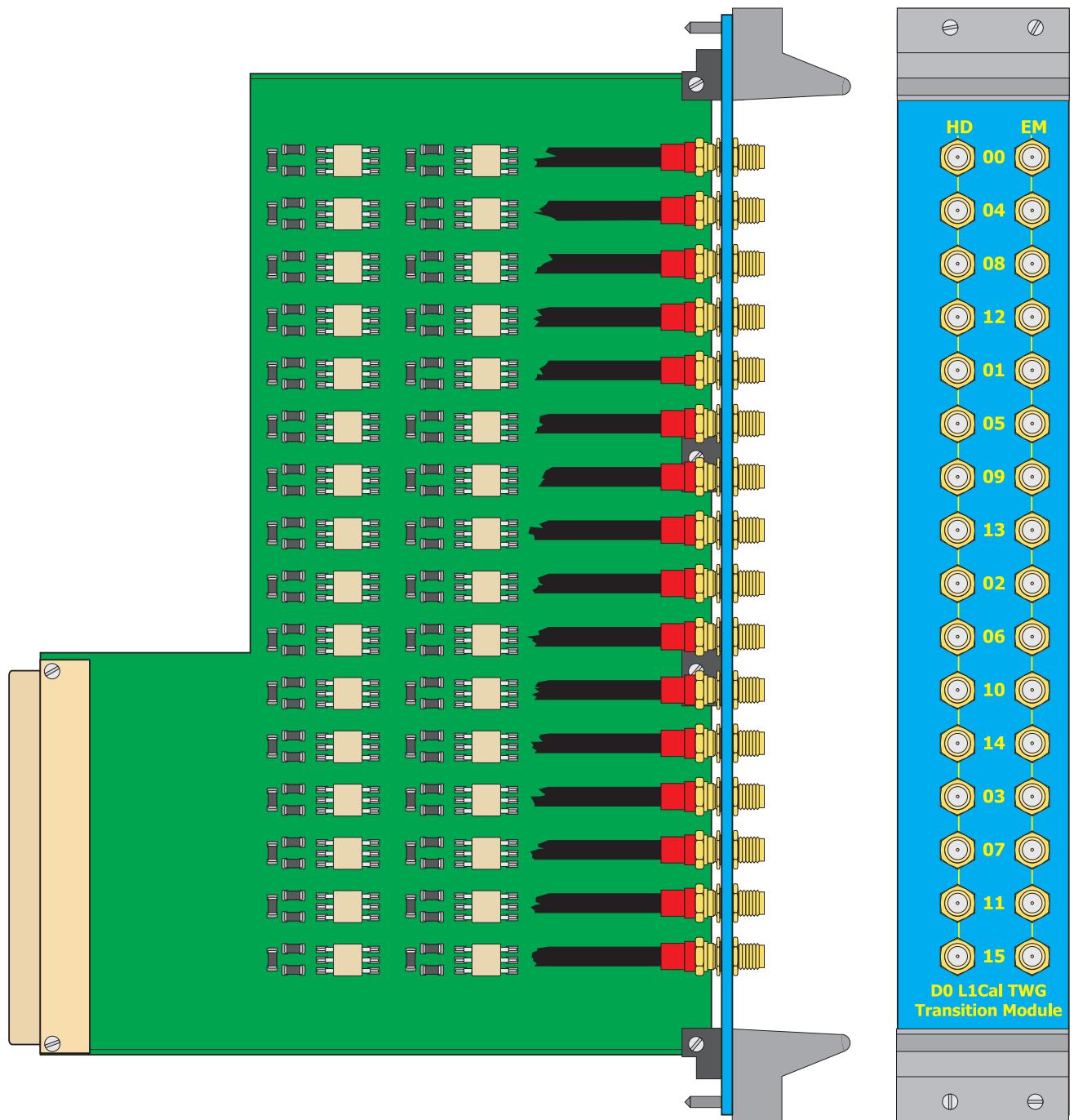


Figure 4.2, TWG transition module

#### 4.4.1 Transformers

Manufacturer: Minicircuits [\[Ref.12\]](#)

Vendor: Surplus Sales of Nebraska [\[Ref.17\]](#)

Model: TT4-1

Impedance ratio: 3

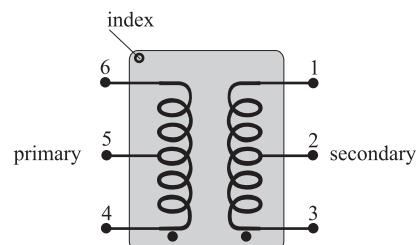
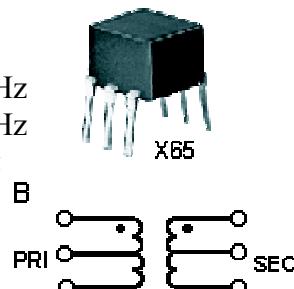
Frequency: 50KHz - 200MHz

3dB Bandwidth: 50KHz - 200MHz

2dB Bandwidth: 200KHz - 50MHz

1dB Bandwidth: 1MHz - 30MHz

Case Style: X65



#### 4.4.2 SMA PCB connectors

Manufacturer: Johnson Components [\[Ref.11\]](#)

Vendor: Newark [\[Ref.14\]](#)

Model: 142-0701-201

Description: SMA jack receptacle connector,

50 Ohm impedance, PCB through hole, straight body style.

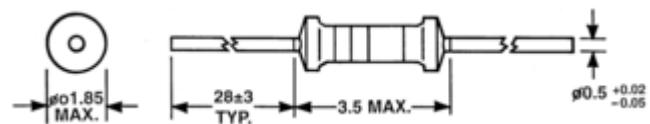
#### 4.4.3 Resistors

Manufacturer: SPC Technology/Multicomp [\[Ref.16\]](#)

Vendor: Newark [\[Ref.14\]](#)

Model: CR1/8W-5%-3R9

Description: Carbon film resistor, power rating 1/8 watt, resistance 3.9 Ohm, tolerance 5%.



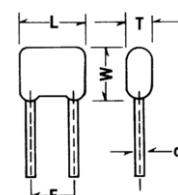
#### 4.4.4 Capacitors

Manufacturer: SPC Technology/Multicomp [\[Ref.16\]](#)

Vendor: Newark [\[Ref.14\]](#)

Model: R30W474K1HL5L

Description: Ceramic multi-layer capacitor, radial lead, dielectric X7R, 0.47 uFarad capacitance, 10% tolerance.



#### 4.4.5 Co-axial cable

Manufacturer: Belden [\[Ref.4\]](#)

Vendor: Mouser Electronics, Inc [\[Ref.13\]](#)

Model: 7500A G7X250

Description: co-axial cable, 30AWG, 75 OHM, stranding: 7x38, conductor diameter: 0.012 inch, overall nominal diameter: 0.110 inch



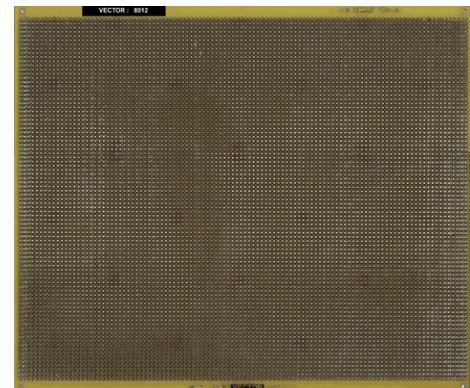
#### 4.4.6 Prototyping board

Manufacturer: Vector Electronics and Technology [\[Ref.18\]](#)

Vendor: Newark [\[Ref.14\]](#)

Manufacturer Part No.: 8012

Description: Prototyping board, .062 in. thickness,  
(HxW) 9.2 x 11 in.



#### 4.4.7 Backplane connector

Manufacturer: Harting [\[Ref.7\]](#)

Part number: 02 04 160 1101

Description: Printed board connector, 160 poles, angled solder pins,  
row pitch 2.54 mm, pin current rating 1 Amp.

## 5 Appendix A - ADF Test Procedure

### 5.1 Agilent 33250A setup

#### 5.1.1 Serial interface setup

For detailed information please refer to the instrument manual [\[Ref.3\]](#).

The interface selection is displayed on the front panel when you turn on the function generator. The interface configuration is accessible from the instrument front panel: Press UTILITY button and then select the RS-232 softkey from the “I/O” menu.

The interface selection is stored in *non-volatile* memory and *does not* change when power has been off or after a remote interface reset.

The suggested settings are those underlined:

Baud Rate: 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200

Parity / Data Bits: None / 8 data bits, Even / 7 data bits, Odd / 7 data bits

Handshake Mode:

None (no handshake mode), DTR/ DSR, Modem, RTS / CTS, XON/ XOFF

Number of Start Bits: 1 bit (fixed)

Number of Stop Bits: 1 bit (fixed)

To connect the function generator to a computer, you must have the proper interface cable. Most computers are DTE (*Data Terminal Equipment*) devices. Since the function generator is also a DTE device, you must use a DTE-to-DTE interface cable. These cables are also called *null-modem*, *modem-eliminator*, or *crossover cables*.

When the interface is working correctly issuing the command \*IDN? should return something like “Agilent Technologies,33250A,0,2.01-1.01-2.00-03-2”.

## 5.2 Agilent 3499A

### 5.2.1 Serial interface setup

For detailed information please refer to the instrument manual [\[Ref.3\]](#).

The suggested settings are:

Baud Rate: 2400, 4800, 9600, 19200, 38400, 57600.

Parity / Data Bits: None / 8 data bits, Even / 7 data bits, Odd / 7 data bits

Handshake Mode:

None (no handshake mode), DTR/ DSR, Modem, RTS / CTS, XON/ XOFF

Number of Start Bits: 1 bit (fixed)

Number of Stop Bits: 1 bit (fixed)

As for the Agilent 33250A function generator, to connect the Agilent 3499A to a computer, you must use a *null-modem* cable.

When the interface is working correctly issuing the command \*IDN? should return something like “Agilent Technologies,3499,SG42000258,4.0 2.0”.

Slot 1: 44478A Dual 1-to-4 Mux Module	Slot 4: 44478A Dual 1-to-4 Mux Module
Slot 2: 44478A Dual 1-to-4 Mux Module	Slot 5: 44478A Dual 1-to-4 Mux Module
Slot 3: N2272A 1-to-9 Mux Module	Slot 0: 3499 Controller

Table 5.1, Agilent 3499A slot configuration

### 5.2.2 Agilent N2272A Multiplexer Module

Channel Addressing (snn, ‘s’= Slot Number, ‘nn’ = Channel Number)  
s00, s01, ....s07, s08.

### 5.2.3 Agilent 44478A Multiplexer Modules

Channel Addressing (snn, ‘s’= Slot Number, ‘nn’ = Channel Number)

Group 0: s00, s01, s02, s03.

Group 1: s10, s11, s12, s13.

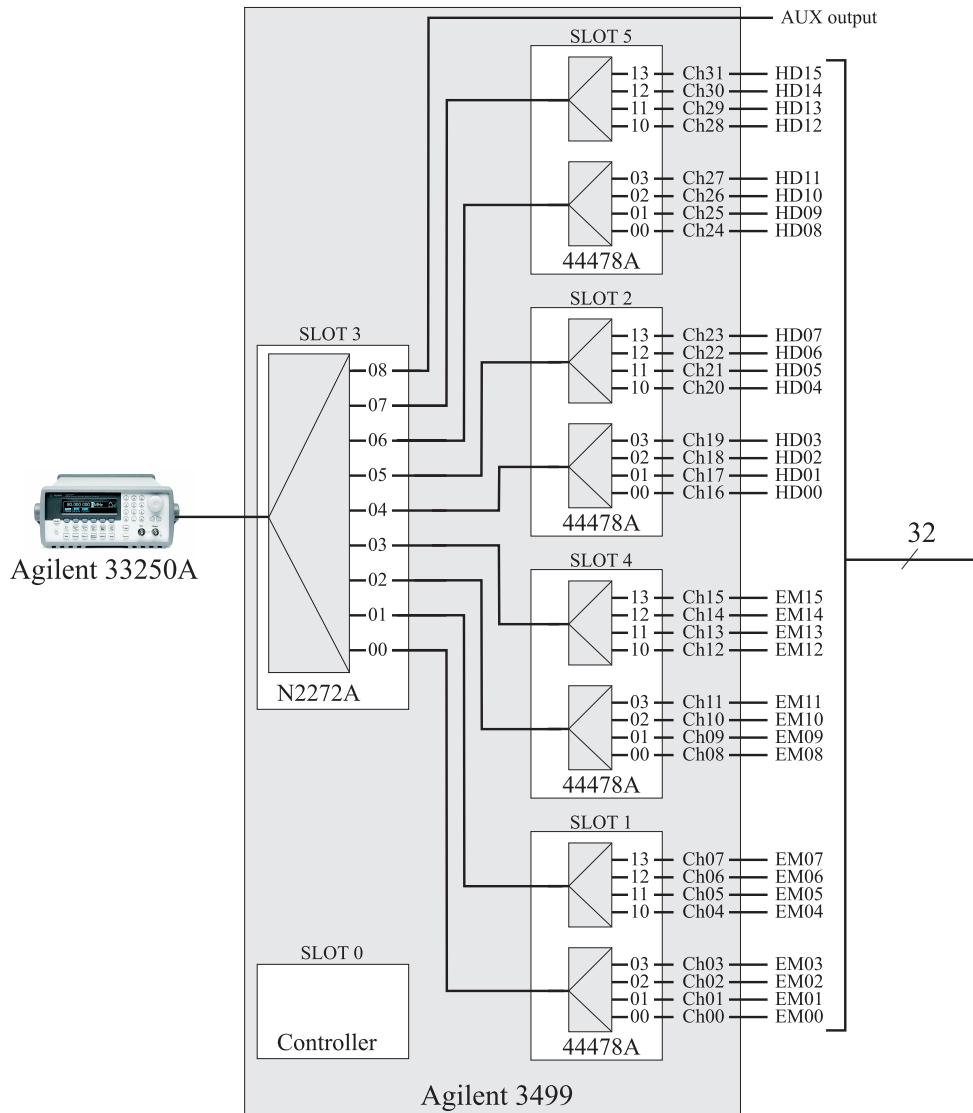


Figure 5.1, Switch System channel/relay numbering and wiring

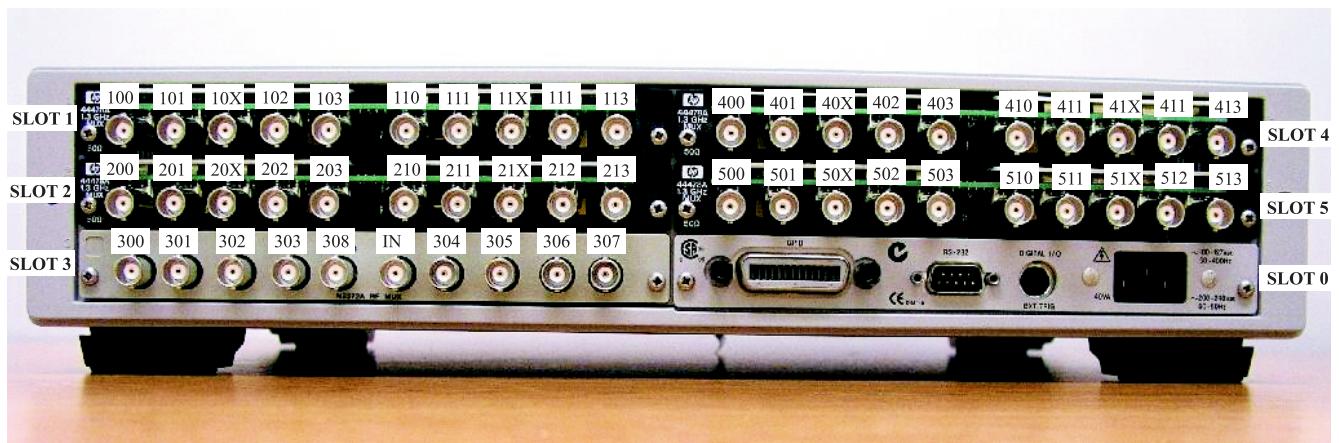


Figure 5.2, Switch System rear view.

Table 5.2 lists the channels relay to be closed in order to activate each output channel.

Output Channel	ADF Channel	N2272A Slot 3	44478A Slot 1		44478A Slot 4		44478A Slot 2		44478A Slot 5	
			Group 0	Group 1						
0	EM00	00	00	=	=	=	=	=	=	=
1	EM01	00	01	=	=	=	=	=	=	=
2	EM02	00	02	=	=	=	=	=	=	=
3	EM03	00	03	=	=	=	=	=	=	=
4	EM04	01	=	10	=	=	=	=	=	=
5	EM05	01	=	11	=	=	=	=	=	=
6	EM06	01	=	12	=	=	=	=	=	=
7	EM07	01	=	13	=	=	=	=	=	=
8	EM08	02	=	=	00	=	=	=	=	=
9	EM09	02	=	=	01	=	=	=	=	=
10	EM10	02	=	=	02	=	=	=	=	=
11	EM11	02	=	=	03	=	=	=	=	=
12	EM12	03	=	=	=	10	=	=	=	=
13	EM13	03	=	=	=	11	=	=	=	=
14	EM14	03	=	=	=	12	=	=	=	=
15	EM15	03	=	=	=	13	=	=	=	=
16	HD00	04	=	=	=	=	00	=	=	=
17	HD01	04	=	=	=	=	01	=	=	=
18	HD02	04	=	=	=	=	02	=	=	=
19	HD03	04	=	=	=	=	03	=	=	=
20	HD04	05	=	=	=	=	=	10	=	=
21	HD05	05	=	=	=	=	=	11	=	=
22	HD06	05	=	=	=	=	=	12	=	=
23	HD07	05	=	=	=	=	=	13	=	=
24	HD08	06	=	=	=	=	=	=	00	=
25	HD09	06	=	=	=	=	=	=	01	=
26	HD10	06	=	=	=	=	=	=	02	=
27	HD11	06	=	=	=	=	=	=	03	=
28	HD12	07	=	=	=	=	=	=	=	10
29	HD13	07	=	=	=	=	=	=	=	11
30	HD14	07	=	=	=	=	=	=	=	12
31	HD15	07	=	=	=	=	=	=	=	13
AUX	HD00	08	=	=	=	=	=	=	=	=

Table 5.2, Switch System Relay/Channel selection table

### 5.3 Example of SCPI commands sequence

Table is an example of SCPI (Standard Commands for Programmable Instruments) sequence meant to control the two instruments part of the TWG system, the Agilent 33250A waveform generator and the Agilent 3499A switch system. The SCPI command sequence was written to setup a waveform and to sequentially send it to the 32 TWG output channels.

The voltage values controlled with the SCPI commands are those at the output of the Agilent 33250A waveform generator when connected to a load of 50 ohm. The voltage values at the output of the TWG system are different due to attenuation introduced by the switch-system/interconnection-cables and by the load impedance change in TWG adapter. Both system attenuation and load characteristics are frequency dependent.

When a sine wave is used an approximation of the output signal peak-to-peak level when a channel is loaded with the series of a .47uF capacitor and a 79 Ohm resistance is obtained multiplying the value selected on the 33250A by the factor  $\sqrt{3}$ .

In the following example the waveform is setup at the beginning of the test and then the Agilent 3499A switch system is used to sequence through the 32 TWG output channels.

Another possible choice is to setup the waveform to different frequencies/amplitudes while a particular channel is selected. This last method will allow performing multiple tests on one channel before switching to a different one and will minimize the use of the switch system relays.

Square brackets ([]) indicate optional keywords, commands or parameters.

It is recommended to turn the output of the waveform generator off before changing waveform settings (Agilent 33250A) or channel selection (Agilent 3499A).

SCPI command	33250A	3499A	Notes
Instruments Setup			
*RST		•	Reset the 3499A to its factory default state
*TST?		•	Self Test, returns 0 if successful
*RST	•		Reset the 33250A to its factory default state
*TST?	•		Self Test, returns 0 if successful
FUNCTION SINusoid	•		Set waveform to sine wave
[FUNCtion?]	•		Verify waveform
FREQuency 50.0E03 FREQuency 2.00E06 FREQuency 25.0E06	•		Set Waveform Frequency to 50 KHz 2 MHz 25 MHz
[FREQuency?]	•		Verify frequency
VOLTage 1.0E-01 VOLTage 1.0E00 VOLTage 5.0E00	•		Set the output waveform peak-to-peak voltage to 100 mVolt 1 Volt 5 Volt Note: the voltage set is at the output of the 33250A waveform generator, the peak to peak voltage at the output of the TWG system is approximately increased by a factor of $\sqrt{3}$ when connected to a 79 ohm load.
[VOLTage?]	•		Verify output waveform peak-to-peak voltage

SCPI command	33250A	3499A	Notes
[DISPlay:TEXT 'SINEWAVE ffMHz vvVolt pp - Output OFF']	•		Display information message
ROUTe:CLOSE (@308)		•	Aux output selected
[DIAGnostic:DISPlay "Channel AUX"]		•	Display "Channel AUX"
OUTPut ON	•		33250A Output ON
[OUTPut?]	•		Verify output status, returns "0" (OFF) or "1" (ON)
[DISPlay:TEXT 'SINEWAVE ffMHz vvVolt pp - Output ON']	•		Display information message
			Verify waveform using oscilloscope connected to the AUX channel.
OUTPut OFF	•		33250A Output OFF
[OUTPut?]	•		Verify output status, returns "0" (OFF) or "1" (ON)
[DISPlay:TEXT 'SINEWAVE ffMHz vvVolt pp - Output OFF']	•		Display information message
Channel 0			
ROUTe:CLOSE (@300, 100)		•	Output channel 0 selected
[DIAGnostic:DISPlay "Channel 0"]		•	Display "Channel 0"
OUTPut ON	•		33250A Output ON
[OUTPut?]	•		Verify output status, returns "0" (OFF) or "1" (ON)
[DISPlay:TEXT 'SINEWAVE ffMHz vvVolt pp - Output ON']	•		Display information message
			Perform tests on ADF input channel 0
OUTPut OFF	•		33250A Output OFF
[OUTPut?]	•		Verify output status, returns "0" (OFF) or "1" (ON)
[DISPlay:TEXT 'SINEWAVE ffMHz vvVolt pp - Output OFF']	•		Display information message
Channel 1			
ROUTe:CLOSE (@300, 101)		•	Output channel 1 selected
[DIAGnostic:DISPlay "Channel 1"]		•	Display "Channel 1"
OUTPut ON	•		33250A Output ON
[OUTPut?]	•		Verify output status, returns "0" (OFF) or "1" (ON)
			Perform tests on ADF input channel 1
OUTPut OFF	•		33250A Output OFF
[OUTPut?]	•		Verify output status, returns "0" (OFF) or "1" (ON)
[DISPlay:TEXT 'SINEWAVE ffMHz vvVolt pp - Output OFF']	•		Display information message
Channel 2			

SCPI command	33250A	3499A	Notes
ROUTe:CLOSe (@300, 102)		●	Output channel 2 selected
[DIAGnostic:DISPlay “Channel 2”]		●	Display “Channel 2”
OUTPut ON	●		33250A Output ON
[OUTPut?]	●		Verify output status, returns “0” (OFF) or “1” (ON)
			Perform tests on ADF input channel 2
OUTPut OFF	●		33250A Output OFF
[OUTPut?]	●		Verify output status, returns “0” (OFF) or “1” (ON)
[DISPlay:TEXT ‘SINEWAVE ffMHz vvVolt pp - Output OFF’]	●		Display information message
Channel 3			
ROUTe:CLOSe (@300, 103)		●	Output channel 3 selected
[DIAGnostic:DISPlay “Channel 3”]		●	Display “Channel 3”
OUTPut ON	●		33250A Output ON
[OUTPut?]	●		Verify output status, returns “0” (OFF) or “1” (ON)
			Perform tests on ADF input channel 3
OUTPut OFF	●		33250A Output OFF
[OUTPut?]	●		Verify output status, returns “0” (OFF) or “1” (ON)
[DISPlay:TEXT ‘SINEWAVE ffMHz vvVolt pp - Output OFF’]	●		Display information message
Channel 4			
ROUTe:CLOSe (@301, 110)		●	Output channel 4 selected
[DIAGnostic:DISPlay “Channel 4”]		●	Display “Channel 4”
OUTPut ON	●		33250A Output ON
[OUTPut?]	●		Verify output status, returns “0” (OFF) or “1” (ON)
			Perform tests on ADF input channel 3
OUTPut OFF	●		33250A Output OFF
[OUTPut?]	●		Verify output status, returns “0” (OFF) or “1” (ON)
[DISPlay:TEXT ‘SINEWAVE ffMHz vvVolt pp - Output OFF’]	●		Display information message
Channel 31			
ROUTe:CLOSe (@307, 513)		●	Output channel 31 selected
[DIAGnostic:DISPlay “Channel 31”]		●	Display “Channel 31”
OUTPut ON	●		33250A Output ON
[OUTPut?]	●		Verify output status, returns “0” (OFF) or “1” (ON)
			Perform tests on ADF input channel 31

SCPI command	33250A	3499A	Notes
OUTPut OFF	•		33250A Output OFF
[OUTPut?]	•		Verify output status, returns "0" (OFF) or "1" (ON)
[DISPlay:TEXT 'SINEWAVE ffMHz vvVolt pp - Output OFF']	•		Display information message
After-Test			
[DISPlay:TEXT:CLEAR]	•		Clear display information message
ROUTE:CLOSe (@308)		•	Aux output selected
[DIAGnostic:DISPlay "Channel AUX"]		•	Display "Channel AUX"
SYSTem:ERRor?		•	Reads errors form the error queue. Returns +0,"No error" if no errors have occurred.
*CLS		•	Clear Status (clear error queue)
SYSTem:ERRor?	•		Reads errors form the error queue. Returns +0,"No error" if no errors have occurred.
*CLS	•		Clear Status (clear error queue)

## 6 Appendix B - VME64x Backplane - connectors pinout

Pin#	Row Z	Row A	Row B	Row C	Row D
1	MPR (Bus Pause Request)	D00 (Data Bus)	BBSY* (Bus Busy)	D08 (Data Bus)	VPC (Voltage Pre-Charge)
2	GND (Ground)	D01 (Data Bus)	BCLR* (Bus Clear)	D09 (Data Bus)	GND (Ground)
3	MCLK (Module Clock)	D02 (Data Bus)	ACFAIL* (AC Power Fail)	D10 (Data Bus)	+V1 (auxiliary power)
4	GND (Ground)	D03 (Data Bus)	BG0IN* (Bus Grant daisy-chain)	D11 (Data Bus)	+V2 (auxiliary power)
5	MSD (Slave Data)	D04 (Data Bus)	BG0OUT* (Bus Grant daisy-chain)	D12 (Data Bus)	ResvU (reserved Unbussed)
6	GND (Ground)	D05 (Data Bus)	BG1IN* (Bus Grant daisy-chain)	D13 (Data Bus)	-V1 (auxiliary power)
7	MMD (Module Data)	D06 (Data Bus)	BG1OUT* (Bus Grant daisy-chain)	D14 (Data Bus)	-V2 (auxiliary power)
8	GND (Ground)	D07 (Data Bus)	BG2IN* (Bus Grant daisy-chain)	D15 (Data Bus)	ResvU (reserved Unbussed)
9	MCTL (Module Control)	GND (Ground)	BG2OUT* (Bus Grant daisy-chain)	GND (Ground)	GAP* (Geographical Address Parity)
10	GND (Ground)	SYSCLK	BG3IN* (Bus Grant daisy-chain)	SYSFAIL* (System Fail)	GA0* (Geographical Address)
11	RESP* (Response)	GND (Ground)	BG3OUT* (Bus Grant daisy-chain)	BERR* (Bus Error)	GA1* (Geographical Address)
12	GND (Ground)	DS1* (Data Strobe)	BR0* (Bus Request)	SYSRESET* (System Reset)	Power:+3.3V
13	ResBus (Reserved Bussed)	DS0* (Data Strobe)	BR1* (Bus Request)	LWORD* (Long Word)	GA2* (Geographical Address)
14	GND (Ground)	WRITE* (Read/Write)	BR2* (Bus Request)	AM5 (Address Modifier)	Power:+3.3V
15	ResBus (Reserved Bussed)	GND (Ground)	BR3* (Bus Request)	A23 (Address Bus)	GA3* (Geographical Address)
16	GND (Ground)	DTACK* (Data Transfer Acknowledge)	AM0 (Address Modifier)	A22 (Address Bus)	Power:+3.3V
17	ResBus (Reserved Bussed)	GND (Ground)	AM1 (Address Modifier)	A21 (Address Bus)	GA4* (Geographical Address)
18	GND (Ground)	AS* (Address Strobe)	AM2 (Address Modifier)	A20 (Address Bus)	Power:+3.3V
19	ResBus (Reserved Bussed)	GND (Ground)	AM3 (Address Modifier)	A19 (Address Bus)	ResBus (Reserved Bussed)
20	GND (Ground)	IACK* (Interrupt Acknowledge)	GND (Ground)	A18 (Address Bus)	Power:+3.3V
21	ResBus (Reserved Bussed)	IACKIN* (Interrupt Acknowledge daisy-chain)	SERA (Serial Bus)	A17 (Address Bus)	ResBus (Reserved Bussed)
22	GND (Ground)	IACKOUT* (Interrupt Acknowledge daisy-chain)	SERB (Serial Bus)	A16 (Address Bus)	Power:+3.3V
23	ResBus (Reserved Bussed)	AM4 (Address Modifier)	GND (Ground)	A15 (Address Bus)	ResBus (Reserved Bussed)
24	GND (Ground)	A07 (Address Bus)	IRQ7* (priority Interrupt request)	A14 (Address Bus)	Power:+3.3V
25	ResBus (Reserved Bussed)	A06 (Address Bus)	IRQ6* (priority Interrupt request)	A13 (Address Bus)	ResBus (Reserved Bussed)
26	GND (Ground)	A05 (Address Bus)	IRQ5* (priority Interrupt request)	A12 (Address Bus)	Power:+3.3V
27	ResBus (Reserved Bussed)	A04 (Address Bus)	IRQ4* (priority Interrupt request)	A11 (Address Bus)	LI/I*
28	GND (Ground)	A03 (Address Bus)	IRQ3* (priority Interrupt request)	A10 (Address Bus)	Power:+3.3V
29	ResBus (Reserved Bussed)	A02 (Address Bus)	IRQ2* (priority Interrupt request)	A09 (Address Bus)	LI/O*
30	GND (Ground)	A01 (Address Bus)	IRQ1* (priority Interrupt request)	A08 (Address Bus)	Power:+3.3V
31	ResBus (Reserved Bussed)	Power: -12V	Power: +5VSTDBY	Power: +12V	GND (Ground)
32	GND (Ground)	Power: +5V	Power: +5V	Power: +5V	VPC (Voltage Pre-Charge)

Table 6.1. VME64x J1 Pin Assignments

Pin#	Row Z	Row A	Row B	Row C	Row D
1	UD (User Defined)	UD (User Defined)	Power: +5V	UD (User Defined)	UD (User Defined)
2	GND (Ground)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)
3	UD (User Defined)	UD (User Defined)	RETRY*	UD (User Defined)	UD (User Defined)
4	GND (Ground)	UD (User Defined)	A24 (Address Bus)	UD (User Defined)	UD (User Defined)
5	UD (User Defined)	UD (User Defined)	A25 (Address Bus)	UD (User Defined)	UD (User Defined)
6	GND (Ground)	UD (User Defined)	A26 (Address Bus)	UD (User Defined)	UD (User Defined)
7	UD (User Defined)	UD (User Defined)	A27 (Address Bus)	UD (User Defined)	UD (User Defined)
8	GND (Ground)	UD (User Defined)	A28 (Address Bus)	UD (User Defined)	UD (User Defined)
9	UD (User Defined)	UD (User Defined)	A29 (Address Bus)	UD (User Defined)	UD (User Defined)
10	GND (Ground)	UD (User Defined)	A30 (Address Bus)	UD (User Defined)	UD (User Defined)
11	UD (User Defined)	UD (User Defined)	A31 (Address Bus)	UD (User Defined)	UD (User Defined)
12	GND (Ground)	UD (User Defined)	Ground	UD (User Defined)	UD (User Defined)
13	UD (User Defined)	UD (User Defined)	Power: +5V	UD (User Defined)	UD (User Defined)
14	GND (Ground)	UD (User Defined)	D16 (Data Bus)	UD (User Defined)	UD (User Defined)
15	UD (User Defined)	UD (User Defined)	D17 (Data Bus)	UD (User Defined)	UD (User Defined)
16	GND (Ground)	UD (User Defined)	D18 (Data Bus)	UD (User Defined)	UD (User Defined)
17	UD (User Defined)	UD (User Defined)	D19 (Data Bus)	UD (User Defined)	UD (User Defined)
18	GND (Ground)	UD (User Defined)	D20 (Data Bus)	UD (User Defined)	UD (User Defined)
19	UD (User Defined)	UD (User Defined)	D21 (Data Bus)	UD (User Defined)	UD (User Defined)
20	GND (Ground)	UD (User Defined)	D22 (Data Bus)	UD (User Defined)	UD (User Defined)
21	UD (User Defined)	UD (User Defined)	D23 (Data Bus)	UD (User Defined)	UD (User Defined)
22	GND (Ground)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)
23	UD (User Defined)	UD (User Defined)	D24 (Data Bus)	UD (User Defined)	UD (User Defined)
24	GND (Ground)	UD (User Defined)	D25 (Data Bus)	UD (User Defined)	UD (User Defined)
25	UD (User Defined)	UD (User Defined)	D26 (Data Bus)	UD (User Defined)	UD (User Defined)
26	GND (Ground)	UD (User Defined)	D27 (Data Bus)	UD (User Defined)	UD (User Defined)
27	UD (User Defined)	UD (User Defined)	D28 (Data Bus)	UD (User Defined)	UD (User Defined)
28	GND (Ground)	UD (User Defined)	D29 (Data Bus)	UD (User Defined)	UD (User Defined)
29	UD (User Defined)	UD (User Defined)	D30 (Data Bus)	UD (User Defined)	UD (User Defined)
30	GND (Ground)	UD (User Defined)	D31 (Data Bus)	UD (User Defined)	UD (User Defined)
31	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	GND (Ground)
32	GND (Ground)	UD (User Defined)	Power: +5V	UD (User Defined)	VPC

Table 6.2. VME64x J2 Pin Assignments

<b>Pin#</b>	<b>Row E</b>	<b>Row E</b>	<b>Row D</b>	<b>Row C</b>	<b>Row B</b>	<b>Row A</b>	<b>Row Z</b>
<b>1</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>2</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>3</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>4</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>5</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>6</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>7</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>8</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>9</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>10</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>11</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>12</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>13</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>14</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>15</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>16</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>17</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>18</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
<b>19</b>	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)

Table 6.3. VME64x P0 Pin Assignments

## 7 Appendix C - ADF System - backplane connectors pinout

Pin#	Row Z	Row A	Row B	Row C	Row D
1	N.C.	VME_DATA(0)	N.C.	VME_DATA(8)	N.C.
2	GROUND	VME_DATA(1)	N.C.	VME_DATA(9)	GROUND
3	N.C.	VME_DATA(2)	N.C.	VME_DATA(10)	N.C.
4	GROUND	VME_DATA(3)	BUS_GRANT_0	VME_DATA(11)	N.C.
5	N.C.	VME_DATA(4)	BUS_GRANT_0	VME_DATA(12)	N.C.
6	GROUND	VME_DATA(5)	VME_BUS_GRANT_1_IN_B	VME_DATA(13)	N.C.
7	N.C.	VME_DATA(6)	VME_BUS_GRANT_1_OUT_B	VME_DATA(14)	N.C.
8	GROUND	VME_DATA(7)	BUS_GRANT_2	VME_DATA(15)	N.C.
9	N.C.	GROUND	BUS_GRANT_2	GROUND	N.C.
10	GROUND	N.C.	BUS_GRANT_3	N.C.	VME_GEO_B(0)
11	N.C.	GROUND	BUS_GRANT_3	N.C.	VME_GEO_B(1)
12	GROUND	VME_DS1_B	N.C.	VME_SYSRESET_B	VME_3V3
13	BKPLN_BEGIN_TURN_B	VME_DS0_B	N.C.	VME_LWORD_B	VME_GEO_B(2)
14	GROUND	VME_WRITE_B	N.C.	VME_AM5	VME_3V3
15	BKPLN_LIVE_BX_B	GROUND	N.C.	VME_ADDR(23)	VME_GEO_B(3)
16	GROUND	VME_DTACK_B	VME_AM0	VME_ADDR(22)	VME_3V3
17	BKPLN_SAVE_MONIT_DATA_B	GROUND	VME_AM1	VME_ADDR(21)	VME_GEO_B(4)
18	GROUND	VME_AS_B	VME_AM2	VME_ADDR(20)	VME_3V3
19	BKPLN_SCL_INIT_B	GROUND	VME_AM3	VME_ADDR(19)	CRATE_STATUS_B(0)
20	GROUND	VME_IACK_B	GROUND	VME_ADDR(18)	VME_3V3
21	BKPLN_BX_CLOCK	VME_IACKIN_B	N.C.	VME_ADDR(17)	CRATE_STATUS_B(1)
22	GROUND	VME_IACKOUT_B	N.C.	VME_ADDR(16)	VME_3V3
23	BKPLN_BX_CLOCK_B	VME_AM4	GROUND	VME_ADDR(15)	CRATE_STATUS_B(2)
24	GROUND	VME_ADD(7)	N.C.	VME_ADDR(14)	VME_3V3
25	BKPLN_SCLD_SPARE_B	VME_ADD(6)	N.C.	VME_ADDR(13)	CRATE_STATUS_B(3)
26	GROUND	VME_ADD(5)	N.C.	VME_ADDR(12)	VME_3V3
27	VME_RSVBUS(7)	VME_ADD(4)	N.C.	VME_ADDR(11)	N.C.
28	GROUND	VME_ADD(3)	N.C.	VME_ADDR(10)	VME_3V3
29	VME_RSVBUS(8)	VME_ADD(2)	VME_IRQ_B(2)	VME_ADDR(9)	N.C.
30	GROUND	VME_ADD(1)	N.C.	VME_ADDR(8)	VME_3V3
31	VME_RSVBUS(9)	VME_N12V	N.C.	VME_P12V	GROUND
32	GROUND	VME_5V	VME_5V	VME_5V	N.C.

Table 7.1. P1 Pin Assignments

Pin#	Row Z	Row A	Row B	Row C	Row D
1	N.C.	Ch_00_HD_P	VME_5V	Ch_00_EM_P	N.C.
2	GROUND	Ch_00_HD_N	GROUND	Ch_00_EM_N	N.C.
3	N.C.	Ch_04_HD_P	N.C.	Ch_04_EM_P	N.C.
4	GROUND	Ch_04_HD_N	N.C.	Ch_04_EM_N	N.C.
5	N.C.	Ch_08_HD_P	N.C.	Ch_08_EM_P	N.C.
6	GROUND	Ch_08_HD_N	N.C.	Ch_08_EM_N	N.C.
7	N.C.	Ch_12_HD_P	N.C.	Ch_12_EM_P	N.C.
8	GROUND	Ch_12_HD_N	N.C.	Ch_12_EM_N	N.C.
9	N.C.	Ch_01_HD_P	N.C.	Ch_01_EM_P	N.C.
10	GROUND	Ch_01_HD_N	N.C.	Ch_01_EM_N	N.C.
11	N.C.	Ch_05_HD_P	N.C.	Ch_05_EM_P	N.C.
12	GROUND	Ch_05_HD_N	GROUND	Ch_05_EM_N	N.C.
13	N.C.	Ch_09_HD_P	VME_5V	Ch_09_EM_P	N.C.
14	GROUND	Ch_09_HD_N	N.C.	Ch_09_EM_N	N.C.
15	N.C.	Ch_13_HD_P	N.C.	Ch_13_EM_P	N.C.
16	GROUND	Ch_13_HD_N	N.C.	Ch_13_EM_N	N.C.
17	N.C.	Ch_02_HD_P	N.C.	Ch_02_EM_P	N.C.
18	GROUND	Ch_02_HD_N	N.C.	Ch_02_EM_N	N.C.
19	N.C.	Ch_06_HD_P	N.C.	Ch_06_EM_P	N.C.
20	GROUND	Ch_06_HD_N	N.C.	Ch_06_EM_N	N.C.
21	N.C.	Ch_10_HD_P	N.C.	Ch_10_EM_P	N.C.
22	GROUND	Ch_10_HD_N	GROUND	Ch_10_EM_N	N.C.
23	N.C.	Ch_14_HD_P	N.C.	Ch_14_EM_P	N.C.
24	GROUND	Ch_14_HD_N	N.C.	Ch_14_EM_N	N.C.
25	N.C.	Ch_03_HD_P	N.C.	Ch_03_EM_P	N.C.
26	GROUND	Ch_03_HD_N	N.C.	Ch_03_EM_N	N.C.
27	N.C.	Ch_07_HD_P	N.C.	Ch_07_EM_P	N.C.
28	GROUND	Ch_07_HD_N	N.C.	Ch_07_EM_N	N.C.
29	N.C.	Ch_11_HD_P	N.C.	Ch_11_EM_P	N.C.
30	GROUND	Ch_11_HD_N	N.C.	Ch_11_EM_N	N.C.
31	N.C.	Ch_15_HD_P	GROUND	Ch_15_EM_P	GROUND
32	GROUND	Ch_15_HD_N	VME_5V	Ch_15_EM_N	N.C.

Table 7.2. P2 Pin Assignments

Pin#	Row E	Row E	Row D	Row C	Row B	Row A	Row Z
1	GROUND	LX0_T1_N (Link 0 Serial Data 1)	LX0_T1_P (Link 0 Serial Data 1)	GROUND	LX0_T0_N (Link 0 Serial Data 0)	LX0_T0_P (Link 0 Serial Data 0)	GROUND
2	GROUND	LX0_TC_N (Link 0 Serial Data Clock)	LX0_TC_P (Link 0 Serial Data Clock)	GROUND	LX0_T2_N (Link 0 Serial Data 2)	LX0_T2_P (Link 0 Serial Data 2)	GROUND
3	GROUND	LX0_T4_N (Link 0 Serial Data 4)	LX0_T4_P (Link 0 Serial Data 4)	GROUND	LX0_T3_N (Link 0 Serial Data 3)	LX0_T3_P (Link 0 Serial Data 3)	GROUND
4	GROUND	LX0_T6_N (Link 0 Serial Data 6)	LX0_T6_P (Link 0 Serial Data 6)	GROUND	LX0_T5_N (Link 0 Serial Data 5)	LX0_T5_P (Link 0 Serial Data 5)	GROUND
5	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND
6	GROUND	LX1_T1_N (Link 0 Serial Data 1)	LX1_T1_P (Link 0 Serial Data 1)	GROUND	LX1_T0_N (Link 1 Serial Data 0)	LX1_T0_P (Link 1 Serial Data 0)	GROUND
7	GROUND	LX1_TC_N (Link 0 Serial Data Clock)	LX1_TC_P (Link 0 Serial Data Clock)	GROUND	LX1_T2_N (Link 1 Serial Data 2)	LX1_T2_P (Link 1 Serial Data 2)	GROUND
8	GROUND	LX1_T4_N (Link 0 Serial Data 4)	LX1_T4_P (Link 0 Serial Data 4)	GROUND	LX1_T3_N (Link 1 Serial Data 3)	LX1_T3_P (Link 1 Serial Data 3)	GROUND
9	GROUND	LX1_T6_N (Link 0 Serial Data 6)	LX1_T6_P (Link 0 Serial Data 6)	GROUND	LX1_T5_N (Link 1 Serial Data 5)	LX1_T5_P (Link 1 Serial Data 5)	GROUND
10	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND
11	GROUND	LX2_T1_N (Link 0 Serial Data 1)	LX2_T1_P (Link 0 Serial Data 1)	GROUND	LX2_T0_N (Link 2 Serial Data 0)	LX2_T0_P (Link 2 Serial Data 0)	GROUND
12	GROUND	LX2_TC_N (Link 0 Serial Data Clock)	LX2_TC_P (Link 0 Serial Data Clock)	GROUND	LX2_T2_N (Link 2 Serial Data 2)	LX2_T2_P (Link 2 Serial Data 2)	GROUND
13	GROUND	LX2_T4_N (Link 0 Serial Data 4)	LX2_T4_P (Link 0 Serial Data 4)	GROUND	LX2_T3_N (Link 2 Serial Data 3)	LX2_T3_P (Link 2 Serial Data 3)	GROUND
14	GROUND	LX2_T6_N (Link 0 Serial Data 6)	LX2_T6_P (Link 0 Serial Data 6)	GROUND	LX2_T5_N (Link 2 Serial Data 5)	LX2_T5_P (Link 2 Serial Data 5)	GROUND
15	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND
16	GROUND	SCL_LIVE_BX_N (SCL Live Beam Crossing)	SCL_LIVE_BX_P (SCL Live Beam Crossing)	GROUND	CREATE_TO_SCLD_0_N (Create to SCLD signal #0)	CREATE_TO_SCLD_0_P (Create to SCLD signal #0)	GROUND
17	GROUND	CREATE_TO_SCLD_1_N (Create to SCLD signal #1)	CREATE_TO_SCLD_1_P (Create to SCLD signal #1)	GROUND	SCL_INIT_N (SCL Initialization)	SCL_INIT_P (SCL Initialization)	GROUND
18	GROUND	SCL_BEGIN_TURN_N (SCL Begin of Turn Marker)	SCL_BEGIN_TURN_P (SCL Begin of Turn Marker)	GROUND	SCL_BX_CLOCK_N (7.57MHz Beam Cross Clock)	SCL_BX_CLOCK_P (7.57MHz Beam Cross Clock)	GROUND
19	GROUND	SCLD_SPARE_P (Spare Signal)	SCLD_SPARE_P (Spare Signal)	GROUND	SAVE_MONIT_DATA_N (Save Monitoring Data)	SAVE_MONIT_DATA_P (Save Monitoring Data)	GROUND

Table 7.3. J0 Pin Assignments

## 8 Appendix E - Serial Interface

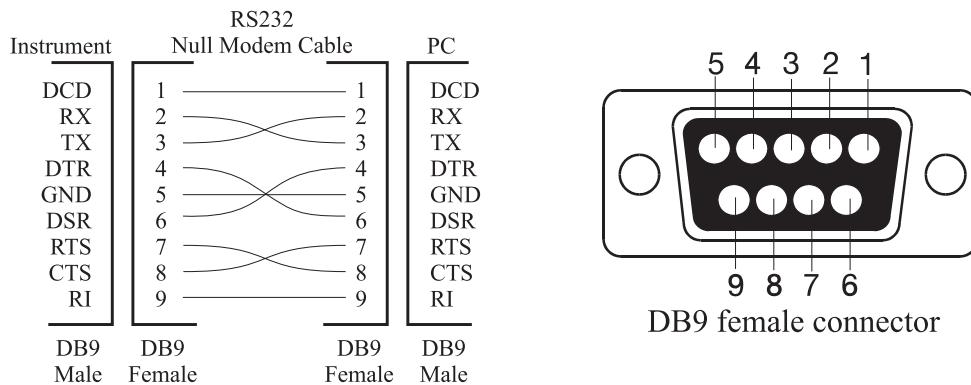


Figure 8.1, RS-232 Null-Modem cable wiring.

Signal name	Description
DCD	Data Carrier Detect
RX	Receive Data (a.k.a RD, RxD)
TX	Transmit Data (a.k.a TD, Tx)
DTR	Data Terminal Ready
GND	Ground
DSR	Data Set Ready
RTS	Request To Send
CTS	Clear To Send
RI	Ring Indicator

Table 8.1, RS232 signals

## 9 Appendix E - D0 Level 1 Trigger System

For detailed information please refer to the D0 Calorimeter RunIIb Level 1 Trigger documentation [\[Ref.2\]](#).

### Calorimeter

A component of the D0 detector experiment is a liquid argon calorimeter. The calorimeter is made by 55296 cells and consists of three units, the Center Calorimeter (CC), and the two End-cap Calorimeters (EC). The calorimeter readout system is being upgraded to improve its performance and the quality of the measurements.

### Preamplifiers:

The charge from the calorimeter cells is integrated in the charge sensitive preamplifiers located on the calorimeter. The preamplifier input impedance is matched to the 30 Ohm coaxial cables from the detector and the preamplifiers have compensated to match the varying detector capacitances.

**BLS:** Summer and Baseline Subtractor card.

The voltage signal generated by the preamplifier are then transmitted single ended on twisted-pair cable to the shaper and baseline subtractor (BLS) cards. The BLS process shapes the signal and removes slowly varying voltage offsets.

The signals from different depths in the electromagnetic and hadronic sections of the calorimeter are added with appropriate weights to form the “analog trigger tower sums”.

The BLS cards take care of the signal conditioning from pre-amplification to weighted sums. The cards are located in a limited access area directly beneath the detector (detector platform).

**ADF:** Analog to Digital converter and digital Filter board.

The 2560 “trigger tower sums” generated by the BLS cards are sent differentially over long ribbons of 80 Ohm coaxial cables to the ADF (ADC and Digital Filter) boards. The Level 1 calorimeter trigger system, including the ADF sub-system, is located on the first floor of the moving counting house.

The ADF board performs the following functions:

Analog-to-Digital conversion of trigger pickoff signals, digital filtering, peak-detector, conversion from energy to transverse energy.

The Level 1 trigger system has 80 ADF boards distributed in 4 VME crates. An ADF board serializes the data and transmits it to the TAB (Trigger Algorithm Board) system over three 48-bit LVDS SER/DES links. These three links transmit exactly the same data to three different TAB boards.

Each ADF crate includes an interface to the Trigger Control Computer (TCC). This slow path is used for downloading, calibration and monitoring.

A timing distribution card connected to a Serial Control Link (SCL) receiver is in charge of distributing the necessary clocks, synchronization and control signals within the ADF system.

In order to perform preliminary test of the new L1 Calorimeter trigger system analog signal splitter cards have been designed. These cards duplicate the analog signals of several BLS's and connect to the CTFEs and the ADF cards being tested.

**TAB:** Trigger Algorithm Board. Each TAB connects to 30 LVDS input links from the ADF system. A TAB board runs the physics selection (sliding window) algorithms on one eighth of the data produced by the ADF system. Results are transmitted to the Level 1 Global Algorithm Board (GAB), Level 2 / Level 3 and to the Calorimeter Track Match system.

**GAB:** Global Algorithm Board. Gathers results and computes global quantities such as missing transverse energy.

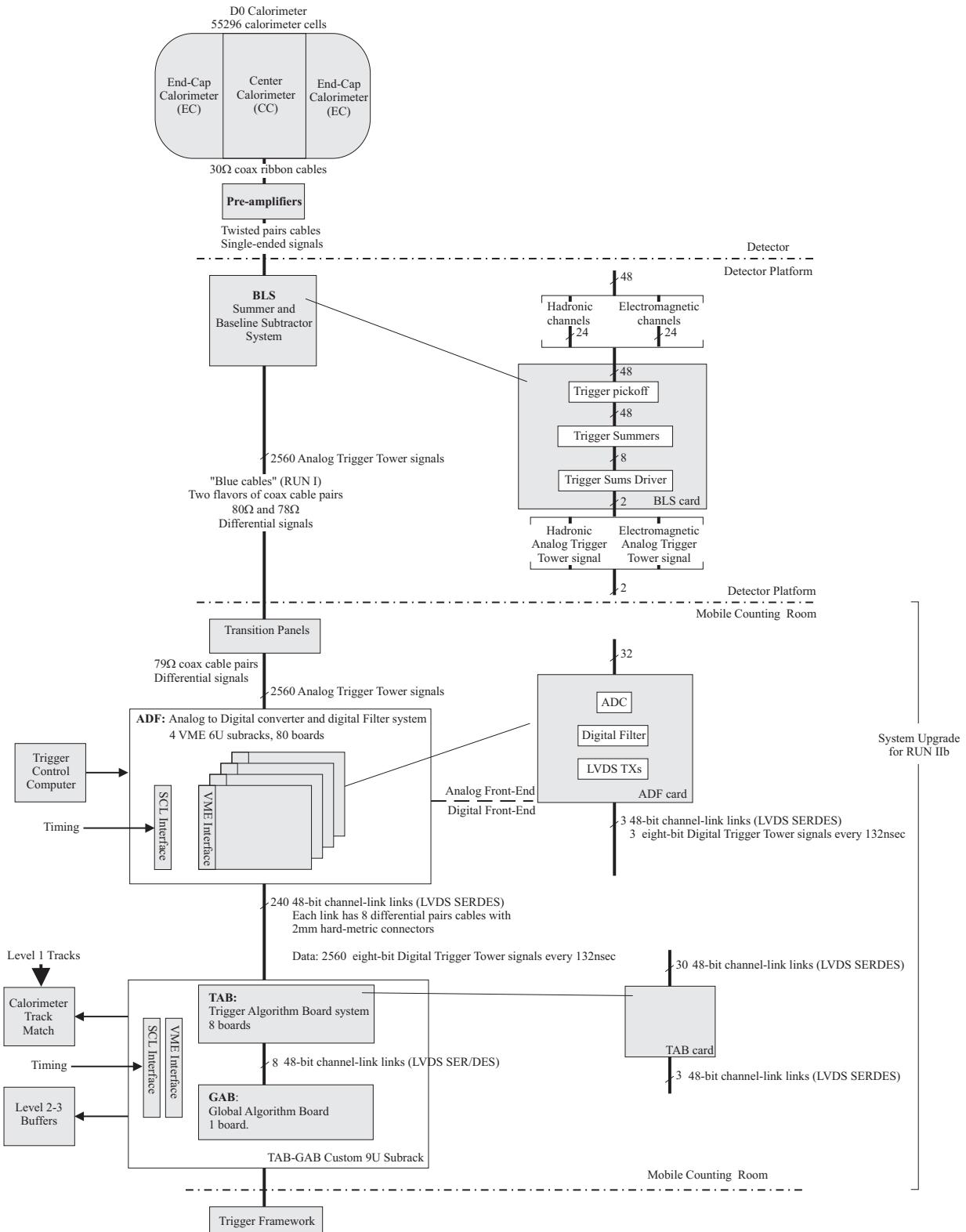


Figure 9.1, Calorimeter Level 1 Trigger block diagram

## 10 Glossary

**ADF:** Analog to Digital converter and Filter board. Component of the Run IIb D0 Level 1 Calorimeter System. See system diagram () .

**BLS:** Summer and Baseline Subtractor card. BLSs are a component of the Run IIb D0 Level 1 Calorimeter System. See system diagram () .

**EM:** Electromagnetic (calorimeter).

**GAB:** Global Algorithm Board. GABs are a component of the Run IIb D0 Level 1 Calorimeter System. See system diagram () .

**HD:** hadronic (calorimeter).

**IEEE:** Institute of Electrical and Electronics Engineers, Inc. [\[Ref.9\]](#).

**IEEE488/HPIB/GPIB:** IEEE-488 bus was developed to connect and control programmable instruments, and to provide a standard interface for communication between instruments. Hewlett-Packard [\[Ref.8\]](#) originally developed the interfacing technique, and called it HP-IB. The interface gained popularity in the computer industry. The IEEE [\[Ref.9\]](#) renamed it GPIB (General Purpose interface Bus).

**Jitter:** The JEDEC Standard No. 65 (EIA/JESD65) defines jitter as the magnitude of the time deviation of a controlled edge from its nominal position.

**RS232/EIA232:** An equipment interconnection standard introduced in the early 1960s by what today is known as the Electronic Industries Association [\[Ref.5\]](#). The standard specifies signal voltages, signal timing, signal function, a protocol for information exchange, and mechanical connectors.

**SCPI:** Standard Commands for Programmable Instruments.

**SCL:** Serial Command Link.

**Skew:** The JEDEC Standard No. 65 (EIA/JESD65) defines skew as The magnitude of the time difference between two events that ideally would occur simultaneously.

**TAB:** Trigger Algorithm Board. TABs are a component of the Run IIb D0 Level 1 Calorimeter System. A TAB run the physics selection algorithms on one eighth of the data produced by the ADF (Analog to Digital converter and Filter) boards. See system diagram () .

**TWG:** Test Waveform Generator System [\[Ref.1\]](#).

**VME/VME64X:** [\[Ref.20\]](#) The VME (VERSAmodule Eurocard) standard was first defined in 1979 by Motorola Corporation. The VMEbus is an asynchronous bus that utilizes a *Master/Slave* architecture. The leftmost slot is the *Master*, and the remaining slots are *Slaves*. The VMEbus is composed of four sub-buses called the *Data Transfer Bus*, the *Data Transfer Arbitration Bus*, the *Priority Interrupt Bus*, and the *Utility Bus*. The original VMEbus standard maximum transfer speed is 40 Mbytes/sec. With the features of the newer VME64X standard described below, that transfer speed has quadrupled to 160 Mbytes/sec. Other features of VMEbus are:

- ) 16, 24, or 32-bit addressing
- ) 8, 16, 24, or 32-bit data path width
- ) Allows unaligned data transfers
- ) Error detection through \*BERR signal
- ) 7 levels of interrupts
- ) System diagnostic capability using the \*SYSFAIL signal
- ) Mechanical standard allows 3U, 6U, or 9U printed circuit boards

The VME64X standard is a superset of the VME standard. Some of the added abilities for VME64X are:

- ) Larger 64-bit data and address paths for 6U boards
- ) 4 times the bandwidth (160 Mbytes/sec)
- ) Cycle retry capability
- ) Bus LOCK cycles
- ) First slot detector
- ) Automatic ‘plug and play’ features
- ) A new 160-pin connector family
- ) A 95-pin J0 connector
- ) 3.3V supply pins
- ) Geographical addressing
- ) 141 more user-defined I/O pins

The VME64X standard utilizes 3 sets of connectors that plug into the backplane. They are a 95-pin connector J0/P0, and two 160-pin connectors, J1/P1 and J2/P2.

## 11 Attachment 1 - Purchase Proposal

### 11.1 Commercial equipment

One Arbitrary Waveform Source: *Agilent 33250A* [\[Ref.3\]](#)

Listed Price: US\$ 4,552. Lead time: 3 weeks.



Figure 11.1, Agilent 33250A Function/Arbitrary Waveform Generator

Switch/Control System:

One *Agilent 3499A* [\[Ref.3\]](#) Switch/Control System, 5 slot mainframe

Listed Price: US\$ 2,300. Lead time: 2 weeks.



Figure 11.2, Agilent 3499A Switch/Control System Mainframe

One *Agilent N2272A* [\[Ref.3\]](#) 1 GHz 1x9 RF Multiplexer Module

Listed Price: US\$ 1,296. Lead time: 2 weeks.

Four *Agilent 44478A* [\[Ref.3\]](#) Dual 1x4 RF Multiplexer Module (1.3GHz, 50 Ohm)

Listed Price: US\$ 1,322. Lead time: 2 weeks.



Figure 11.3, Agilent 44478A Dual 1x4 RF Multiplexer Module

Equipment Cost (list): US\$ 13,406

Approximate discounted (GS) cost: **US\$ 12,065**

## 12 TWG System Equipment list

Agilent 33250A Box:

- 1) Agilent 33250A
- 2) Power cable
- 3) 10 feet RS-232 cable
- 4) 8 feet RS-232 cable
- 4) User's Guide
- 5) 33250A Quick Reference Guide
- 6) Service Guide
- 7) CD Agilent Intuiflink for the 33250A

Agilent 3499A Box:

- 1) Agilent 3499A pre-assembled with one Agilent N2272A and four Agilent 44478A.
- 2) Power cable
- 3) 10 feet RS-232 cable
- 4) User's Manual
- 5) 3499A Quick Reference Guide
- 6) 32 BNC-SMA cables
- 7) 1 BNC-SMA cable (AUX)
- 8) 2 BNC-SMA cable (spares)
- 9) 9 BNC-BNC 3nsec cables
- 10) 1 black BNC-BNC cable (33250A OUT to N2272A Input)
- 11) 10 SMB 50 Ohm terminations.

TWG Transition Module Box:

- 1) TWG transition Module
- 2) TWG System Document
- 3) Binder: TWG Equipment List and System Documents

## 13 References

[1] Test Waveform Generator System documentation

[http://www-ese.fnal.gov/D0Cal\\_TWG/](http://www-ese.fnal.gov/D0Cal_TWG/)

[2] D0 Calorimeter RunIIb Level 1 Trigger documentation:

<http://www.nevis.columbia.edu/~evans/l1cal/index.html>

[3] Agilent (formerly Hewlett-Packard) documentation:

- a) Agilent 33250A User's Guide.
  - b) Agilent 3499A/B/C User's Manual
- Information available on Internet:

<http://www.agilent.com/>

- [4] Belden CDT  
7701 Forsyth Boulevard, Suite 800, St. Louis, MO 63105  
<http://www.belden.com/>
- [5] Electronic Industries Alliance  
2500 Wilson Blvd. Arlington, VA 22201  
<http://www.eia.org/>
- [6] GPIB: see glossary (Chapter 10).
- [7] Harting:  
Harting Inc. of North America  
1370 Bowes Road, Elgin, IL 60123  
<http://www.harkis.harting.com/>
- [8] Hewlett-Packard  
3000 Hanover Street, Palo Alto, CA 94304-1185 USA  
<http://www.hp.com/>
- [9] IEEE: Institute of Electrical and Electronics Engineers, Inc.  
<http://www.ieee.org/>
- [10] IEEE 1101.11-1998 Standard for Mechanical Rear Plug-In Unit Specifications for Microcomputers Using IEEE 1101.1 and IEEE 1101.10 Equipment Practice.  
ISBN 0-7381-0179-6  
The Institute of Electrical and Electronics Engineers, Inc.  
<http://www.ieee.org/>
- [11] Johnson Components  
299 Johnson Ave S.W., Suite 100, Waseca MN 56093  
<http://www.johnsoncomponents.com/>
- [12] Minicircuits:  
Branson, MO 65615  
<http://www.minicircuits.com/>
- [13] Mouser Electronics, Inc.  
1000 North Main Street, Mansfield, Texas 76063  
<http://www.mouser.com/>
- [14] Newark InOne  
4801 N. Ravenswood, Chicago, IL 60640-4496  
<http://www.newark.com/>
- [15] RS-232: see glossary (Chapter 10).

[16] SPC Technology:  
4801 N. Ravenswood Ave.  
Chicago, IL 60640-4496  
<http://www.spctechnology.com/>

[17] Surplus Sales of Nebraska  
1502 Jones Street, Omaha, NE 68102-3112  
<http://www.surplussales.com/>

[18] Vector Electronics and Technology:  
11115 Vanowen St., North Hollywood, CA 91605, US  
<http://www.vectorelect.com/>

[19] VITA, VMEbus International Trade Association  
PO Box 19658, Fountain Hills, AZ 85269  
<http://www.vita.com/>

[20] The VMEbus Handbook, Wade D. Peterson, 4<sup>th</sup> Edition 1997. ISBN 1-885731-08-6.

[21] The VMEbus Specification, VMEbus International Trade Association [Ref.VITA]

[22] Feedback is very welcome.

