



Fermi National Accelerator Laboratory

**D-Zero Detector Calorimeter Electronics
Run II b Upgrade Project**

Test Waveform Generator System
Custom System Specification

SUPERSEDED

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TABLE OF CONTENTS

1	INTRODUCTION	3
2	OVERVIEW	4
3	TWG CARD AND SYSTEM.....	4
3.1	INTERFACES.....	4
3.2	HOW THE TWG FITS INTO THE TESTING OF THE D0 CALORIMETER LEVEL 1 TRIGGER SYSTEM	6
	Figure 3.1, Block diagram of the ADF section on the L1 trigger system.....	6
3.2.1	<i>TWG single card system</i>	7
	Figure 3.2, Test Waveform Generator single card system.	7
3.2.2	<i>TWG 10 cards system</i>	7
	Figure 3.3, Test Waveform Generator system.....	7
3.3	TWG CARD BLOCK DIAGRAM	8
	Figure 3.4, TWG Card block diagram.....	8
4	INTERFACES	9
4.1	BACKPLANE INTERFACE	9
4.2	POWER SUPPLY	9
4.3	DATA INTERFACE	9
4.3.1	<i>DAC Daughter card</i>	10
4.3.2	<i>Interface with ADF card</i>	10
	Figure 4.1, Electrical diagram of TWG-ADF interface.....	10
4.4	GENERAL PURPOSE INTERFACE	11
4.4.1	<i>Serial Command Link daughter card</i>	11
	Figure 4.2, Serial Link Receiver (SLR) daughter card.....	11
4.5	RS-232 INTERFACE	12
4.6	USB INTERFACE.....	12
4.7	JTAG INTERFACE.....	12
	Table 4.1, JTAG Chain Devices	12
4.8	LOGIC ANALYZER CONNECTORS	12
4.9	MEMORY MAP.....	13
5	BOARD CONFIGURATION.....	13
5.1	CONFIGURATION THROUGH JTAG	13
5.2	CONFIGURATION THROUGH VME.....	13
6	MONITORING AND DIAGNOSTIC FEATURES	13
6.1	LED DIAGNOSTICS	13
7	APPENDIX A - BACKPLANE INTERFACE - CONNECTORS PINOUT	14
	Table 7.1, J1/P1 Pin Assignments.....	14
	Table 7.2, J2/P2 Pin Assignments.....	15
	Table 7.3, J0/P0 Pin Assignments.....	16
8	APPENDIX B - MAIN BOARD COMPONENTS AND LAYOUT	17
8.1	FRONT PANEL LAYOUT.....	17
	Figure 8.1, TWG front panel layout.....	17
9	APPENDIX C - D0 LEVEL 1 TRIGGER SYSTEM.....	18
	Figure 9.1, Calorimeter Level 1 Trigger block diagram.....	20
10	GLOSSARY	21
	Figure 10.1, Switching standards.....	24
	Figure 10.2, Comparison of switching standards.....	24

11 REFERENCES26

1 Introduction

This document specifies the Test Waveform Generator System. The Test Waveform Generator System is part of the electronics of the D-Zero detector Calorimeter Trigger Test System at Fermilab. More information on the experiments performed at Fermilab is available on the laboratory web page: <http://www.fnal.gov/>

More information on the D0 Detector is available on: <http://www-d0.fnal.gov/>

The designers welcome suggestions and corrections [Ref. 13], which can be addressed directly to the engineer responsible of the project. Contact information is available on the Electronics System Engineering (ESE) web page: <http://www-eese.fnal.gov/>

More information and documentation on the Test Waveform Generator Project are available on: http://www-eese.fnal.gov/D0Cal_TWG/

2 Overview

The Test Waveform Generator (TWG) is a VME64 [Ref.16] double wide 6U board used for testing the D0 Calorimeter Level 1 Trigger electronics [Ref. Par. 9]. The board is a custom “arbitrary waveform generator” with 32 analog outputs and can be operated stand-alone with minimal additional hardware.

The current testing needs require only a 32 channel TWG. The design allows for system expansions to a 10 boards 320 channel arbitrary waveform generator system.

This expanded system will consist of a 21 slots VME 64X subrack. In a TWG system slot 1 can be occupied by a VME subrack controller, even slots between slot 2 to slot 20 can host up to ten TWG boards.

3 TWG card and system

3.1 Interfaces

The TWG board supports the following interfaces:

Backplane Interface

VME bus

Used for configuration download and for remote access (controls and diagnostic). The VME [Ref.16] interface conforms to VME64X (VITA 1.1 - 1997) standard.

Timing

The TWG is able to use the same timing interface used by the system under test (ADF system, [Ref. Par. 9]). The Timing interface is implemented on backplane connector J0.

Board-to-board

In order to allow for a set of boards to operate synchronously without outside timing references, one of the boards can be operated as timing master and the other boards are operated as timing slaves. Some of the user-defined pins on the backplane connector J2 can be used for board-to-board connections and for distribution of clock and timing information.

Power supply

A TWG board is powered through the backplane connection to the subrack power supply. For stand-alone operations the board can be powered through an auxiliary connector. Each TWG board has its own over-current/over-voltage protection.

Analog Data Output Interface daughter-card

Each TWG board host two data output interface daughter cards. Each of the daughter cards implements a 16 channels arbitrary waveform generator.

General-Purpose Interface daughter-card

Each TWG board can host one general-purpose interface daughter card. The general-purpose interface daughter cards can provide additional functionalities depending on the test environment the TWG is used in. The interface consists of two connectors; one follows the footprint and pinout

form of the Serial Command Link Receiver daughter card [Ref.15] the other connector allows for future system expansions/interfaces.

Serial Link Receiver (SLR) daughter card

The SLR daughter card receives serial trigger and timing information at about 1Gbit/sec over coaxial cable. The SCL card decodes and de-multiplexes this information and provides it to the TWG board at a 7.59MHz rate. The TWG board returns status information to the SCL card, which translates these signals to ANSI TIA/EIA 485 standard.

This card allow for the TWG to operate synchronously to the D0 timing distribution system.

JTAG (IEEE 1149.1) interface

A four pin Test Access Port (TAP) provides access to the TWG board JTAG chain. The JTAG port is used for board FPGAs/EEPROMs configuration, diagnostic, and boundary scan.

USB interface

A USB interface can be used for the board standalone operation removing the need of a VME subrack and controller.

Serial (RS232) interface

The serial interface can be used for the board standalone operation removing the need of a VME subrack and controller.

Logic Analyzer interface

For debugging/diagnostic purposes, the TWG board and the Data Output daughter card will have a few connectors to fit the high-density adapter cables for Agilent 16550A logic analyzers.

3.2 How the TWG fits into the testing of the D0 calorimeter Level 1 Trigger System

The main purpose of the TWG is to test the ADF cards/system [Paragraph 9]. Figure 3.1 briefly describes the ADF system and its interfaces. The TWG will not be a part of the D0 Trigger system but will be used only to verify performance and functionality of the ADF cards in a separate test environment. Besides emulating the signals produced by the Baseline Subtractor System (BLS) the TWG is able to generate arbitrary waveforms that can be used to measure the characteristics of the ADF's analog input stage.

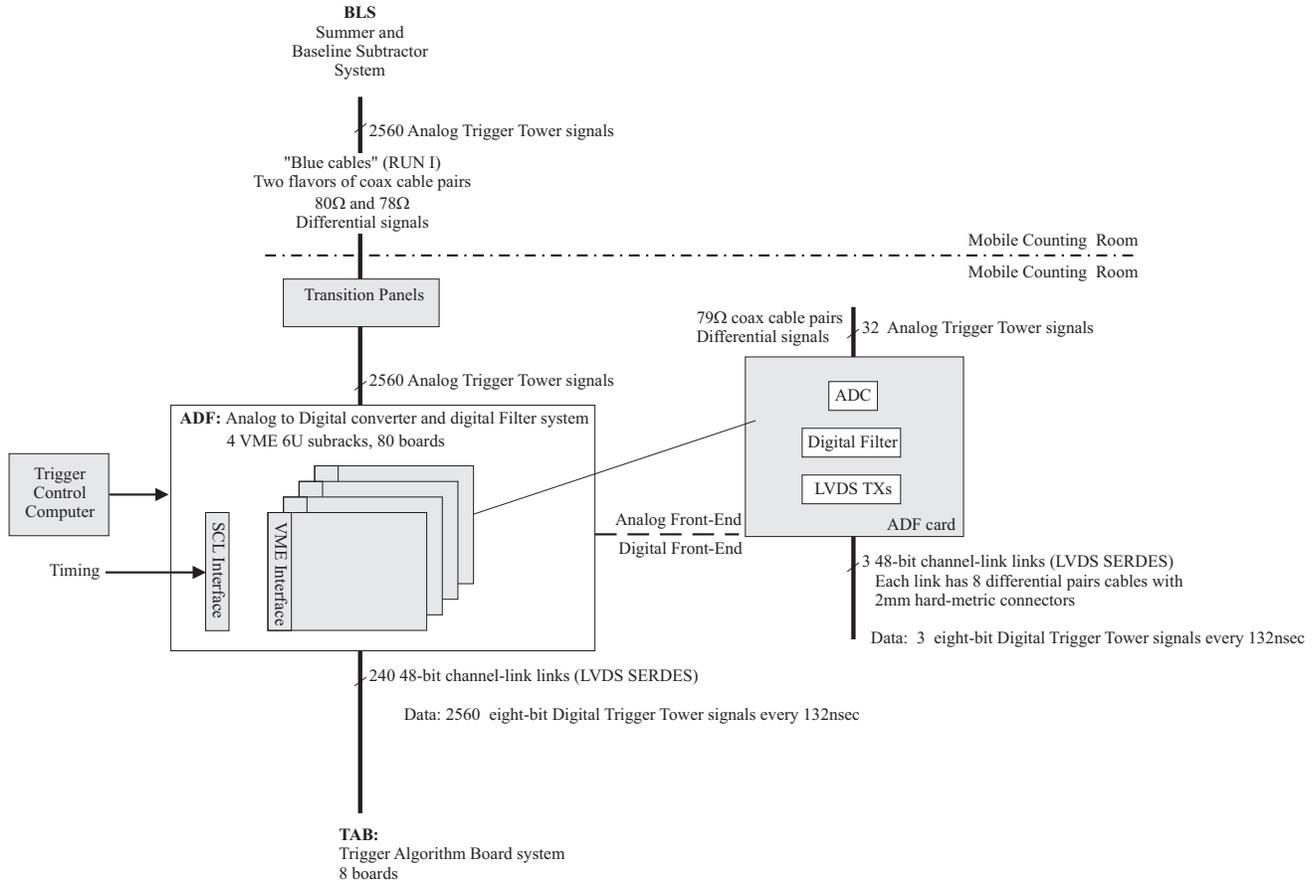


Figure 3.1, Block diagram of the ADF section on the L1 trigger system

3.2.1 TWG single card system

When the TWG system is used to test only one ADF card at a time only one TWG card is needed and the card can be operated in standalone mode. In this mode the card can be positioned on a bench or in a 6 U VME subrack. The card can be controlled from PC using the RS-232 or the USB interfaces. If timing synchronization to the D0 timing distribution is required the TWG card can host a Serial Command Link Receiver (SLR) on its general-purpose interface. In standalone operation the TWG card is powered through an on-board connector by an external power supply.

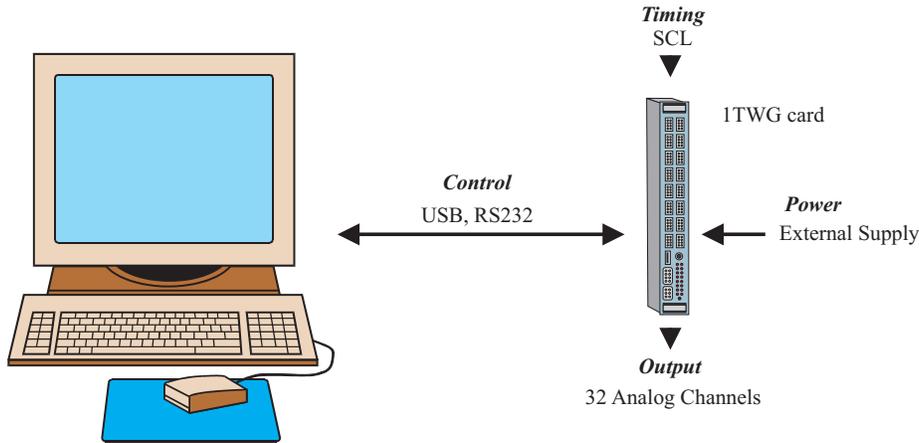


Figure 3.2, Test Waveform Generator single card system.

3.2.2 TWG 10 cards system

If more than one ADF card needs to be tested simultaneously the TWG standalone system can be expanded to a 10-card system hosted by a 6U VME64X subrack. In this case, the cards can be accessed through their RS-232 or USB interfaces. All 10 cards in the system can be accessed through the RS-232/USB interface of just one card that is configured to act as a master on the VME backplane bus.

Alternatively a VME subrack controller can be hosted in the subrack slot 1. This controller can provide the TWG system with additional interfaces to the outside world (Ethernet, MIL-STD 1553).

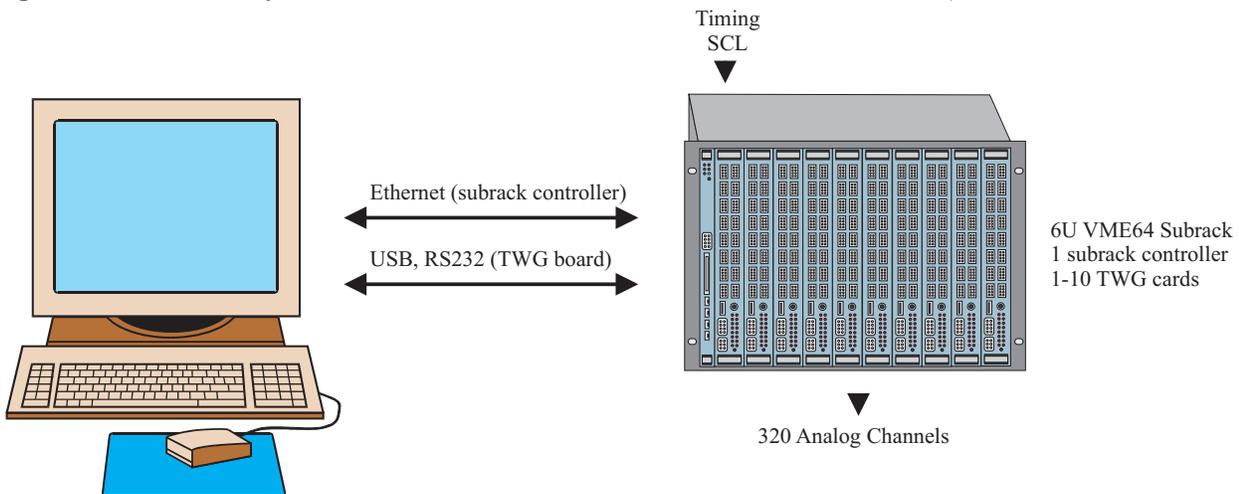


Figure 3.3, Test Waveform Generator system.

3.3 TWG card block diagram

Figure 3.4 provides a block diagram of a TWG board.

The board can be controlled through three different interfaces: RS-232 and USB (front panel) and VME (backplane).

The TWG card has two FPGAs. The “Control FPGA” handles the interfaces, the timing and the diagnostics; the “Data FPGA” handles the data flow operations. The FPGAs are configured at power-up by an on-board EEPROM. The Data FPGA manages the control signals and data for the Analog Data Output Interface daughter cards. The Data FPGA controls an on-board memory, which stores the data used to generate analog waveforms by the two Analog Data Output Interface daughter cards. On these daughter cards the digital signal from the memory is converted to differential analog signal and then amplified in two different stages.

A JTAG front panel connector provides access to both the FPGAs and their configuration EEPROM.

Timing information can be received by an SCR card installed on the general-purpose interface or by user-definable pins on backplane connector J2. If external timing is not available a 53MHz oscillator provides the Control FPGA with a time reference used to emulate the D0 timing signals.

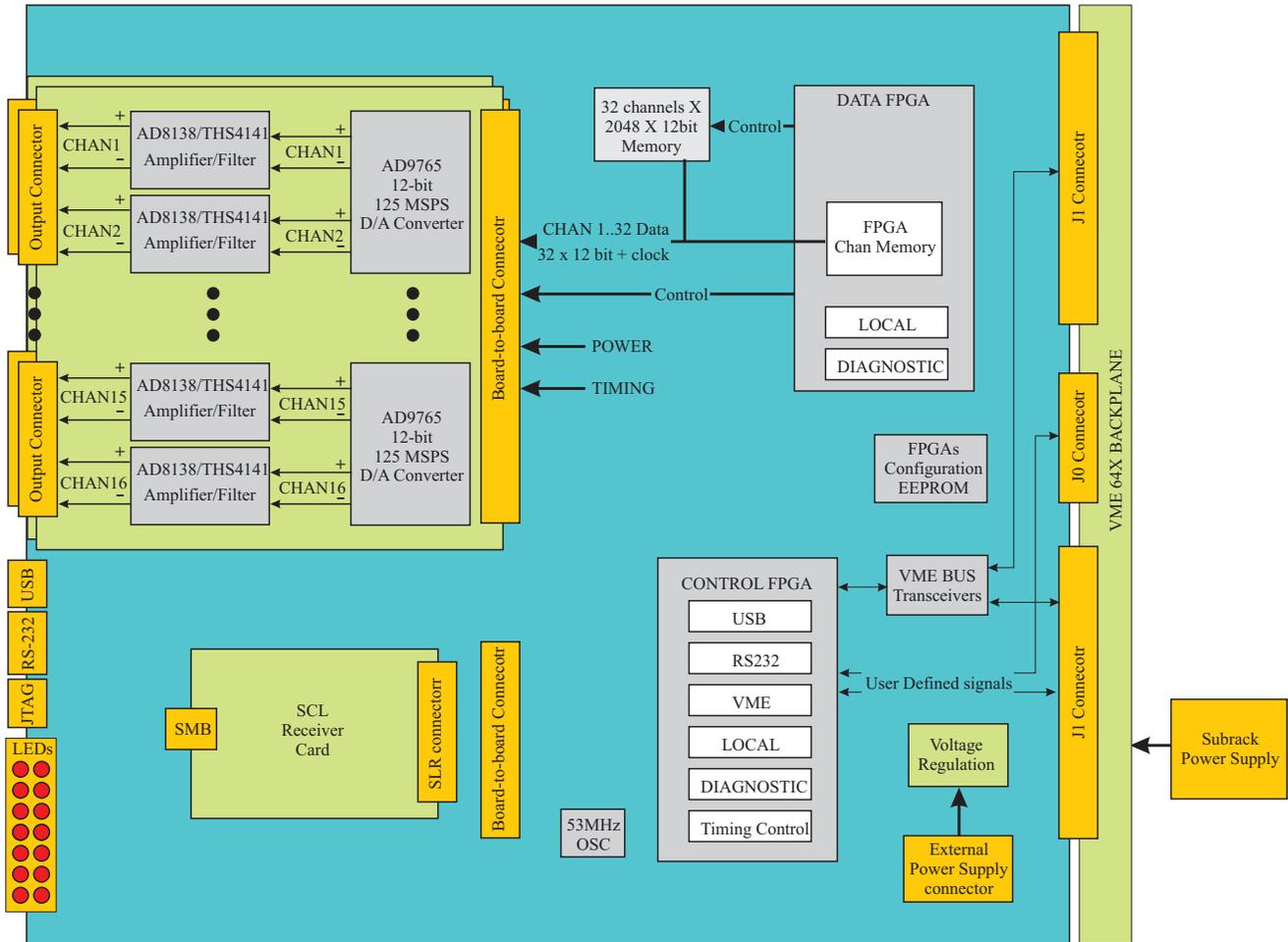


Figure 3.4, TWG Card block diagram

4 Interfaces

4.1 Backplane Interface

The TWG system will utilize the VME64X (VITA 1.1-1997) electrical and mechanical standard. The subrack will be 6U high by 160mm deep.

The VME64X standard and the 6U form factor were chosen to make the board compatible with the ADF subrack.

The VME64X standard utilizes 3 sets of connectors that plug into the backplane. They are a 95-pin connector J0/P0, and two 160-pin connectors, J1/P1 and J2/P2. Backplane interface pinouts are provided in Paragraph 7.

4.2 Power supply

During normal operation, the VME64X standard provides, via the J1/P1 and the J2/P2 connectors, ten pins of +3.3V and six pins of +5V. The current provided by these two voltages will be sufficient to power the digital section of the TWG system. However, each analog amplifier channel consumes approximately 100ma each of +12V and -12V (this includes the primary stage of amplification that uses +/-5V for it's rail voltages). The 32 channels used on the TWG system will consume 3.2 total amps of each voltage. The standard VME64X backplane connector provides 1 pin that supplies +12V, and 1 pin that provides -12V. Each pin is rated for 1.5 amps. Since the amperage available for the +/-12V is not sufficient, the +/-12V voltages will be provided by an external supply and fed through the user defined A and C rows of the J2/P2 connector. Each voltage will have 6 power pins and 6 GND pins reserved on the J2/P2 connector. The method used to provide these voltages on the A and C row the J2/P2 connector has not been decided. Either a separate printed circuit board with a +/-12V supply and a transition module J2/P2 connector will be used, or some type of supply cabled directly from a +/-12V supply to the J2/P2 connector will be employed. The +/-12V pins on the J1/P1 connector will not be used so as not to conflict with the power being supplied by the J2/P2 connector. There are 46 GND pins available on the J1/P1 and J2/P2 connectors. These will be sufficient for the TWG card.

The TWG card will also have Molex style power connectors that will provide all of the voltages necessary on the board for standalone operations.

The primary stage amplifiers use +/-5V for their rail voltages. The +/-12V supplies will be regulated down to these voltages. Since the heat generated within the regulators by this drop in voltage will be a significant factor, the regulators must be assembled with heavy-duty heat sinks.

4.3 Data Interface

The Data interface allows the TWG board to host and control two daughter cards through a high-density board-to-board connector. The interface connector provides also power and ground connections for the daughter cards components.

Data generation for the DAC daughter cards will be provided by two sources, 32 Cypress CY7C1021CV33-8 64K x 16 SRAM (one for each channel) on the motherboard or by direct connection through the Data Xilinx FPGA. Access time for the SRAM is 8ns. This will allow the TWG system to be operated at a board clock rate of 125Mhz., and a waveform maximum frequency of 62.5Mhz. Because the SRAM is 16-bits wide, 12 of the bits will be used for DAC data, and the other 4 bits will be control bits to the DAC daughter card.

4.3.1 DAC Daughter card

The TWG board host two DAC cards. Each of these cards drives 16 differential output channels.

DAC Resolution: 12 bits. This value determine the maximum dynamic range (ratio, in dB, between the largest and the smallest sine wave the DAC can output):

$$Dynamic\ Range = 20 \cdot \log_{10} 2^{DAC\ bits} = 72dB$$

Sample Clock rate: adjustable up to 125 MS/sec

Memory Samples: 64K

Low-pass Filter Poles: TBD.

Output Amplifier Voltage: 6 Volt pk-pk, 0 Volt common mode.

4.3.2 Interface with ADF card

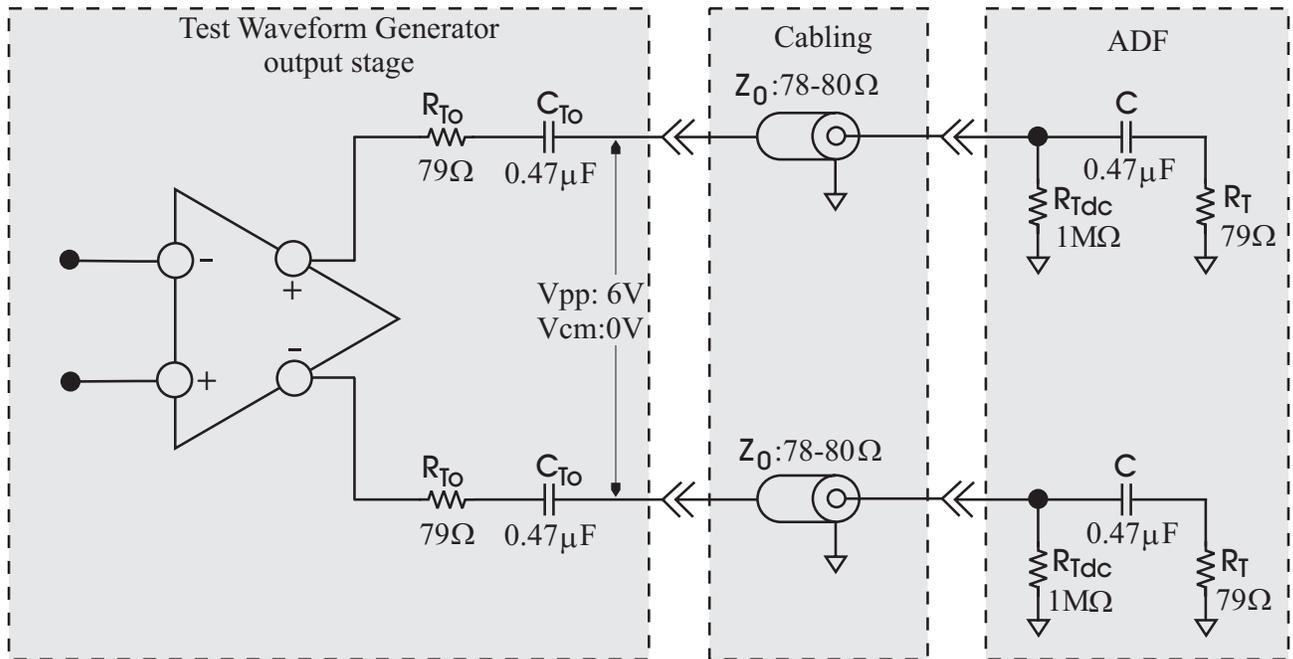


Figure 4.1, Electrical diagram of TWG-ADF interface

4.4 General Purpose Interface

The General Purpose interface consist of two types of connectors, one is designed to fit the footprint and pinout of the Serial Command Link Receiver. The second connector provides a more general interface for future expansion of board capabilities.

4.4.1 Serial Command Link daughter card

The Serial Command Link Receiver (SCLR) daughter card [Ref.14] receives serial trigger and timing information at 1.062Gbits/sec over LMR-200 coaxial cable. The SCLR card decodes and demultiplexes this information and provides it to the TWG board as 75-bit wide data at a 7.59MHz rate. The TWG board returns 8-bits of status information to the SCLR card which translates these signals to ANSI TIA/EIA 485 standard.

This card allow for the TWG to operate synchronously to the D0 timing distribution system.

The TWG system has two 64-pin connectors on it that will allow the addition of a Serial Command Link Receiver (SCLR). The TWG system can use the SCLR data from the D0 Trigger distribution system to trigger waveform output at user defined times.

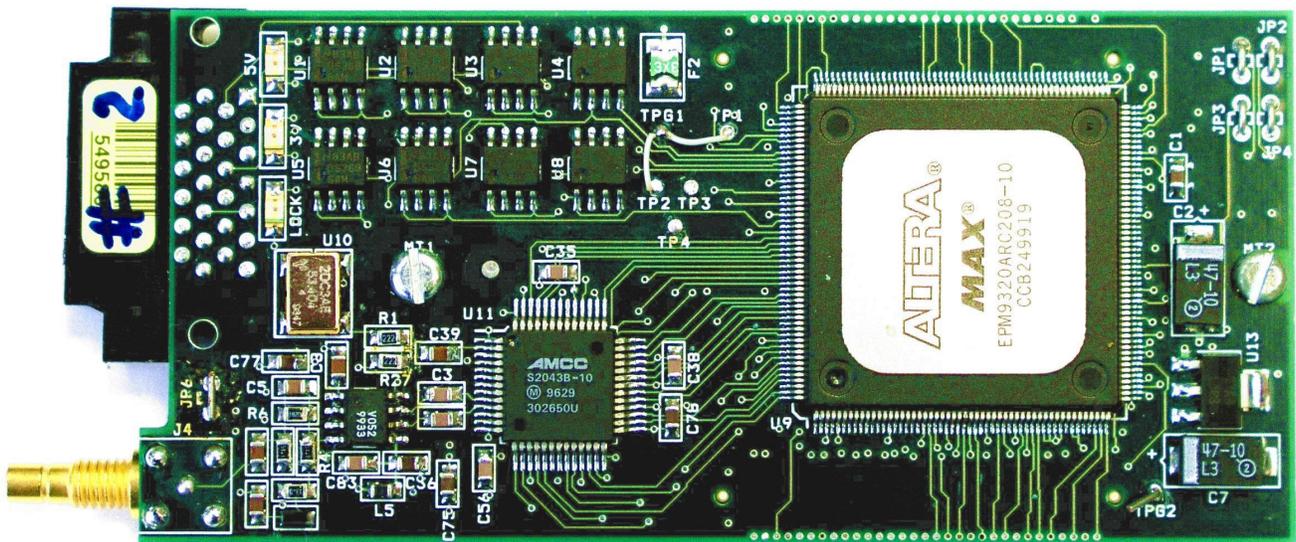


Figure 4.2, Serial Link Receiver (SLR) daughter card

4.5 RS-232 Interface

A Universal Asynchronous Receiver/Transmitter (UART) is implemented in Control FPGA. The UART allows interfacing the card with a computer having a serial port. The TWG uses an Analog Devices ADM3222 as RS-232 transceiver. The card behaves like a Data Communication Equipment (DCE) with adjustable settings. The default settings are the following: BAUD rate 115200, 1 start bit, 2 stop bits, no parity and no handshake.

4.6 USB Interface

A USB interface is implemented in the Control FPGA. The interface allows access to board control and diagnostics and in a multiple-board system to all the other board in the subrack (TWG board operate as a VME bus master).

4.7 JTAG Interface

See a description of JTAG in Paragraph 10. One four pin Test Access Port (TAP) is provided on the TWG card, it accesses the Control and Data FPGAs and their configuration EEPROM.

JTAG Chain		
Device #	Device Type	Notes
1	XC	In-System-Programmable Configuration EEPROM.
2	XV	Control FPGA
3	XV	Data FPGA

Table 4.1, JTAG Chain Devices

4.8 Logic Analyzer Connectors

For debugging/diagnostic purposes the TWG card has three Amp "Mictor 38" connectors (AMP 2-767004-2) to fit the Agilent (formerly HP) High Density adapter cables (Agilent E5346A). Each adapter cable fits two test pods of an Agilent 16550A Logic Analyzer allowing monitoring up to 38 signals.

4.9 Memory Map

The Memory mapping will allow access to board registers and memory through three different interfaces, VME, USB and RS232.

5 Board Configuration

5.1 Configuration through JTAG

For testing purposes the TWG board FPGAs can be programmed through the JTAG interface front panel connector.

5.2 Configuration through VME

At power-up both FPGAs (Control and Data) of the TWG card are configured with the content of the on-board EEPROM. The TWG card has the capability to accept configuration of the Data FPGA over the VME bus. The content of the EEPROM is not affected by a VME re-configuration of the Data FPGA.

6 Monitoring and diagnostic features

The TWG design includes several diagnostic features. Beside logic analyzer connectors on both the TWG board and daughter cards the user can access relevant information on board status from VME, USB and RS232 interfaces.

6.1 LED diagnostics

A simplified version of the diagnostic uses the reset push button and thirty-two bicolor LEDs on the TWG front panel. This allows the user to view in real-time the status on board signals, registers and flags scrolling through several “monitoring modes”. The reset button is used to select which mode is active.

7 Appendix A - Backplane Interface - connectors pinout

Pin#	Row Z	Row A	Row B	Row C	Row D
1	MPR (Bus Pause Request) [●]	D00 (Data Bus)	BBSY* (Bus Busy)	D08 (Data Bus)	VPC (Voltage Pre-Charge) [●]
2	GND (Ground)	D01 (Data Bus)	BCLR* (Bus Clear)	D09 (Data Bus)	GND (Ground)
3	MCLK (Module Clock) [●]	D02 (Data Bus)	ACFAIL* (AC Power Fail) [●]	D10 (Data Bus)	+V1 (auxiliary power) [●]
4	GND (Ground)	D03 (Data Bus)	BG0IN* (Bus Grant daisy-chain)	D11 (Data Bus)	+V2 (auxiliary power) [●]
5	MSD (Slave Data) [●]	D04 (Data Bus)	BG0OUT* (Bus Grant daisy-chain)	D12 (Data Bus)	ResvU (reserved Unbussed) [●]
6	GND (Ground)	D05 (Data Bus)	BG1IN* (Bus Grant daisy-chain)	D13 (Data Bus)	-V1 (auxiliary power) [●]
7	MMD (Module Data) [●]	D06 (Data Bus)	BG1OUT* (Bus Grant daisy-chain)	D14 (Data Bus)	-V2 (auxiliary power) [●]
8	GND (Ground)	D07 (Data Bus)	BG2IN* (Bus Grant daisy-chain)	D15 (Data Bus)	ResvU (reserved Unbussed) [●]
9	MCTL (Module Control) [●]	GND (Ground)	BG2OUT* (Bus Grant daisy-chain)	GND (Ground)	GAP* (Geographical Address Parity)
10	GND (Ground)	SYSCLK	BG3IN* (Bus Grant daisy-chain)	SYSFAIL* (System Fail) [●]	GA0* (Geographical Address)
11	RESP* (Response) [●]	GND (Ground)	BG3OUT* (Bus Grant daisy-chain)	BERR* (Bus Error)	GA1* (Geographical Address)
12	GND (Ground)	DS1* (Data Strobe)	BR0* (Bus Request)	SYSRESET* (System Reset)	Power:+3.3V
13	ResBus (Reserved Bussed) [●]	DS0* (Data Strobe)	BR1* (Bus Request)	LWORD* (Long Word)	GA2* (Geographical Address)
14	GND (Ground)	WRITE* (Read/Write)	BR2* (Bus Request)	AM5 (Address Modifier)	Power:+3.3V
15	ResBus (Reserved Bussed) [●]	GND (Ground)	BR3* (Bus Request)	A23 (Address Bus)	GA3* (Geographical Address)
16	GND (Ground)	DTACK* (Data Transfer Acknowledge)	AM0 (Address Modifier)	A22 (Address Bus)	Power:+3.3V
17	ResBus (Reserved Bussed) [●]	GND (Ground)	AM1 (Address Modifier)	A21 (Address Bus)	GA4* (Geographical Address)
18	GND (Ground)	AS* (Address Strobe)	AM2 (Address Modifier)	A20 (Address Bus)	Power:+3.3V
19	ResBus (Reserved Bussed) [●]	GND (Ground)	AM3 (Address Modifier)	A19 (Address Bus)	ResBus (Reserved Bussed) [●]
20	GND (Ground)	IACK* (Interrupt Acknowledge)	GND (Ground)	A18 (Address Bus)	Power:+3.3V
21	ResBus (Reserved Bussed) [●]	IACKIN* (Interrupt Acknowledge daisy-chain)	SERA (Serial Bus)[●]	A17 (Address Bus)	ResBus (Reserved Bussed) [●]
22	GND (Ground)	IACKOUT* (Interrupt Acknowledge daisy-chain)	SERB (Serial Bus)[●]	A16 (Address Bus)	Power:+3.3V
23	ResBus (Reserved Bussed) [●]	AM4 (Address Modifier)	GND (Ground)	A15 (Address Bus)	ResBus (Reserved Bussed) [●]
24	GND (Ground)	A07 (Address Bus)	IRQ7* (priority Interrupt request)	A14 (Address Bus)	Power:+3.3V
25	ResBus (Reserved Bussed) [●]	A06 (Address Bus)	IRQ6* (priority Interrupt request)	A13 (Address Bus)	ResBus (Reserved Bussed) [●]
26	GND (Ground)	A05 (Address Bus)	IRQ5* (priority Interrupt request)	A12 (Address Bus)	Power:+3.3V
27	ResBus (Reserved Bussed) [●]	A04 (Address Bus)	IRQ4* (priority Interrupt request)	A11 (Address Bus)	LI/I* [●]
28	GND (Ground)	A03 (Address Bus)	IRQ3* (priority Interrupt request)	A10 (Address Bus)	Power:+3.3V
29	ResBus (Reserved Bussed) [●]	A02 (Address Bus)	IRQ2* (priority Interrupt request)	A09 (Address Bus)	LI/O* [●]
30	GND (Ground)	A01 (Address Bus)	IRQ1* (priority Interrupt request)	A08 (Address Bus)	Power:+3.3V
31	ResBus (Reserved Bussed) [●]	Power: -12V	Power: +5VSTDBY [●]	Power: +12V	GND (Ground)
32	GND (Ground)	Power: +5V	Power: +5V	Power: +5V	VPC (Voltage Pre-Charge) [●]

Table 7.1. J1/P1 Pin Assignments

Pin#	Row Z	Row A	Row B	Row C	Row D
1	UD (User Defined)	UD (User Defined)	Power: +5V	UD (User Defined)	UD (User Defined)
2	GND (Ground)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)
3	UD (User Defined)	UD (User Defined)	RETRY* [●]	UD (User Defined)	UD (User Defined)
4	GND (Ground)	UD (User Defined)	A24 (Address Bus)	UD (User Defined)	UD (User Defined)
5	UD (User Defined)	UD (User Defined)	A25 (Address Bus)	UD (User Defined)	UD (User Defined)
6	GND (Ground)	UD (User Defined)	A26 (Address Bus)	UD (User Defined)	UD (User Defined)
7	UD (User Defined)	UD (User Defined)	A27 (Address Bus)	UD (User Defined)	UD (User Defined)
8	GND (Ground)	UD (User Defined)	A28 (Address Bus)	UD (User Defined)	UD (User Defined)
9	UD (User Defined)	UD (User Defined)	A29 (Address Bus)	UD (User Defined)	UD (User Defined)
10	GND (Ground)	UD (User Defined)	A30 (Address Bus)	UD (User Defined)	UD (User Defined)
11	UD (User Defined)	UD (User Defined)	A31 (Address Bus)	UD (User Defined)	UD (User Defined)
12	GND (Ground)	UD (User Defined)	Ground	UD (User Defined)	UD (User Defined)
13	UD (User Defined)	UD (User Defined)	Power: +5V	UD (User Defined)	UD (User Defined)
14	GND (Ground)	UD (User Defined)	D16 (Data Bus)	UD (User Defined)	UD (User Defined)
15	UD (User Defined)	UD (User Defined)	D17 (Data Bus)	UD (User Defined)	UD (User Defined)
16	GND (Ground)	UD (User Defined)	D18 (Data Bus)	UD (User Defined)	UD (User Defined)
17	UD (User Defined)	UD (User Defined)	D19 (Data Bus)	UD (User Defined)	UD (User Defined)
18	GND (Ground)	UD (User Defined)	D20 (Data Bus)	UD (User Defined)	UD (User Defined)
19	UD (User Defined)	UD (User Defined)	D21 (Data Bus)	UD (User Defined)	UD (User Defined)
20	GND (Ground)	UD (User Defined)	D22 (Data Bus)	UD (User Defined)	UD (User Defined)
21	UD (User Defined)	UD (User Defined)	D23 (Data Bus)	UD (User Defined)	UD (User Defined)
22	GND (Ground)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)
23	UD (User Defined)	UD (User Defined)	D24 (Data Bus)	UD (User Defined)	UD (User Defined)
24	GND (Ground)	UD (User Defined)	D25 (Data Bus)	UD (User Defined)	UD (User Defined)
25	UD (User Defined)	UD (User Defined)	D26 (Data Bus)	UD (User Defined)	UD (User Defined)
26	GND (Ground)	UD (User Defined)	D27 (Data Bus)	UD (User Defined)	UD (User Defined)
27	UD (User Defined)	UD (User Defined)	D28 (Data Bus)	UD (User Defined)	UD (User Defined)
28	GND (Ground)	UD (User Defined)	D29 (Data Bus)	UD (User Defined)	UD (User Defined)
29	UD (User Defined)	UD (User Defined)	D30 (Data Bus)	UD (User Defined)	UD (User Defined)
30	GND (Ground)	UD (User Defined)	D31 (Data Bus)	UD (User Defined)	UD (User Defined)
31	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	GND (Ground)
32	GND (Ground)	UD (User Defined)	Power: +5V	UD (User Defined)	VPC [●]

Table 7.2. J2/P2 Pin Assignments

Pin#	Row E	Row E	Row D	Row C	Row B	Row A	Row Z
1	GND (Ground)	LX0_T1_N (Link 0 Serial Data 1)	LX0_T1_P (Link 0 Serial Data 1)	GND (Ground)	LX0_T0_N (Link 0 Serial Data 0)	LX0_T0_P (Link 0 Serial Data 0)	GND (Ground)
2	GND (Ground)	LX0_TC_N (Link 0 Serial Data Clock)	LX0_TC_P (Link 0 Serial Data Clock)	GND (Ground)	LX0_T2_N (Link 1 Serial Data 2)	LX0_T2_P (Link 0 Serial Data 2)	GND (Ground)
3	GND (Ground)	LX0_T4_N (Link 0 Serial Data 4)	LX0_T4_P (Link 0 Serial Data 4)	GND (Ground)	LX0_T3_N (Link 0 Serial Data 3)	LX0_T3_P (Link 0 Serial Data 3)	GND (Ground)
4	GND (Ground)	LX0_T6_N (Link 0 Serial Data 6)	LX0_T6_P (Link 0 Serial Data 6)	GND (Ground)	LX0_T5_N (Link 0 Serial Data 5)	LX0_T5_P (Link 0 Serial Data 5)	GND (Ground)
5	GND (Ground)	GND (Ground)	GND (Ground)	GND (Ground)	GND (Ground)	GND (Ground)	GND (Ground)
6	GND (Ground)	LX1_T1_N (Link 0 Serial Data 1)	LX1_T1_P (Link 0 Serial Data 1)	GND (Ground)	LX1_T0_N (Link 1 Serial Data 0)	LX1_T0_P (Link 1 Serial Data 0)	GND (Ground)
7	GND (Ground)	LX1_TC_N (Link 0 Serial Data Clock)	LX1_TC_P (Link 0 Serial Data Clock)	GND (Ground)	LX1_T2_N (Link 1 Serial Data 2)	LX1_T2_P (Link 1 Serial Data 2)	GND (Ground)
8	GND (Ground)	LX1_T4_N (Link 0 Serial Data 4)	LX1_T4_P (Link 0 Serial Data 4)	GND (Ground)	LX1_T3_N (Link 1 Serial Data 3)	LX1_T3_P (Link 1 Serial Data 3)	GND (Ground)
9	GND (Ground)	LX1_T6_N (Link 0 Serial Data 6)	LX1_T6_P (Link 0 Serial Data 6)	GND (Ground)	LX1_T5_N (Link 1 Serial Data 5)	LX1_T5_P (Link 1 Serial Data 5)	GND (Ground)
10	GND (Ground)	GND (Ground)	GND (Ground)	GND (Ground)	GND (Ground)	GND (Ground)	GND (Ground)
11	GND (Ground)	LX2_T1_N (Link 0 Serial Data 1)	LX2_T1_P (Link 0 Serial Data 1)	GND (Ground)	LX2_T0_N (Link 2 Serial Data 0)	LX2_T0_P (Link 2 Serial Data 0)	GND (Ground)
12	GND (Ground)	LX2_TC_N (Link 0 Serial Data Clock)	LX2_TC_P (Link 0 Serial Data Clock)	GND (Ground)	LX2_T2_N (Link 2 Serial Data 2)	LX2_T2_P (Link 2 Serial Data 2)	GND (Ground)
13	GND (Ground)	LX2_T4_N (Link 0 Serial Data 4)	LX2_T4_P (Link 0 Serial Data 4)	GND (Ground)	LX2_T3_N (Link 2 Serial Data 3)	LX2_T3_P (Link 2 Serial Data 3)	GND (Ground)
14	GND (Ground)	LX2_T6_N (Link 0 Serial Data 6)	LX2_T6_P (Link 0 Serial Data 6)	GND (Ground)	LX2_T5_N (Link 2 Serial Data 5)	LX2_T5_P (Link 2 Serial Data 5)	GND (Ground)
15	GND (Ground)	GND (Ground)	GND (Ground)	GND (Ground)	GND (Ground)	GND (Ground)	GND (Ground)
16	GND (Ground)	CRATE_TO_SCLD_1_N (Crate to SCLD signal #1)	CRATE_TO_SCLD_1_P (Crate to SCLD signal #1)	GND (Ground)	CRATE_TO_SCLD_0_N (Crate to SCLD signal #0)	CRATE_TO_SCLD_0_P (Crate to SCLD signal #0)	GND (Ground)
17	GND (Ground)	SCL_LIVE_BX_N (SCL Live Beam Crossing)	SCL_LIVE_BX_P (SCL Live Beam Crossing)	GND (Ground)	SCL_INIT_N (SCL Initialization)	SCL_INIT_P (SCL Initialization)	GND (Ground)
18	GND (Ground)	SCL_BEGIN_TURN_N (SCL Begin of Turn Marker)	SCL_BEGIN_TURN_P (SCL Begin of Turn Marker)	GND (Ground)	SCL_BX_CLOCK_N (7.57MHz Beam Cross Clock)	SCL_BX_CLOCK_P (7.57MHz Beam Cross Clock)	GND (Ground)
19	GND (Ground)	SCLD_SPARE_P (Spare Signal)	SCLD_SPARE_P (Spare Signal)	GND (Ground)	SAVE_MONIT_DATA_N (Save Monitoring Data)	SAVE_MONIT_DATA_P (Save Monitoring Data)	GND (Ground)

Table 7.3. J0/P0 Pin Assignments

8 Appendix B - Main Board Components and Layout

8.1 Front Panel Layout

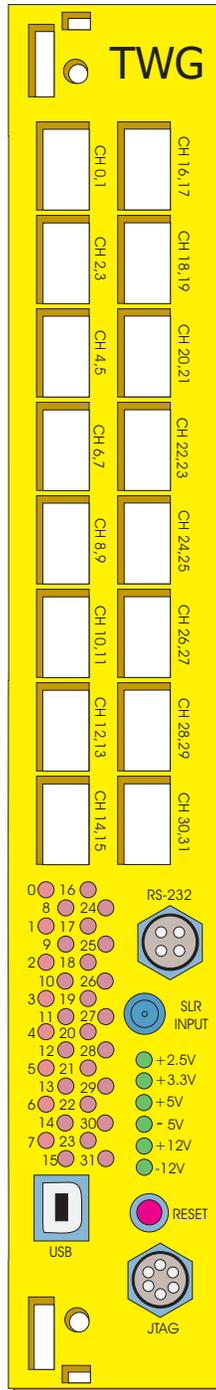


Figure 8.1, TWG front panel layout

9 Appendix C - D0 Level 1 Trigger System

Calorimeter

A component of the D0 detector experiment is a liquid argon calorimeter. The calorimeter is made by 55296 cells and consists of three units, the Center Calorimeter (CC), and the two End-cap Calorimeters (EC). The calorimeter readout system is being upgraded to improve its performance and the quality of the measurements.

Preamplifiers:

The charge from the calorimeter cells is integrated in the charge sensitive preamplifiers located on the calorimeter. The preamplifier input impedance is matched to the 30 Ω coaxial cables from the detector and the preamplifiers have compensated to match the varying detector capacitances.

BLS: Summer and Baseline Subtractor card.

The voltage signal generated by the preamplifier are then transmitted single ended on twisted-pair cable to the shaper and baseline subtractor (BLS) cards. The BLS process shapes the signal and removes slowly varying voltage offsets.

The signals from different depths in the electromagnetic and hadronic sections of the calorimeter are added with appropriate weights to form the “analog trigger tower sums”.

The BLS cards take care of the signal conditioning from pre-amplification to weighted sums. The cards are located in a limited access area directly beneath the detector (detector platform).

ADF: Analog to Digital converter and digital Filter board.

The 2560 “trigger tower sums” generated by the BLS cards are sent differentially over long ribbons of 80 ohm coaxial cables to the ADF (ADC and Digital Filter) boards. The Level 1 calorimeter trigger system, including the ADF sub-system, is located on the first floor of the moving counting house.

The ADF board performs the following functions:

Analog-to-Digital conversion of trigger pickoff signals, digital filtering, peak-detector, conversion from energy to transverse energy.

The Level 1 trigger system has 80 ADF boards distributed in 4 VME crates. An ADF board serializes the data and transmits it to the TAB (Trigger Algorithm Board) system over three 48-bit LVDS SER/DES links. These three links transmit exactly the same data to three different TAB boards.

Each ADF crate includes an interface to the Trigger Control Computer (TCC). This slow path is used for downloading, calibration and monitoring.

A timing distribution card connected to a Serial Control Link (SCL) receiver is in charge of distributing the necessary clocks, synchronization and control signals within the ADF system.

In order to perform preliminary test of the new L1 Calorimeter trigger system analog signal splitter cards have been designed. These cards duplicate the analog signals of several BLS's and connect to the CTFEs and the ADF cards being tested.

TAB: Trigger Algorithm Board. Each TAB connects to 30 LVDS input links from the ADF system. A TAB board runs the physics selection (sliding window) algorithms on one eighth of the

data produced by the ADF system. Results are transmitted to the Level 1 Global Algorithm Board (GAB), Level 2 / Level 3 and to the Calorimeter Track Match system.

GAB: Global Algorithm Board. Gathers results and computes global quantities such as missing transverse energy.

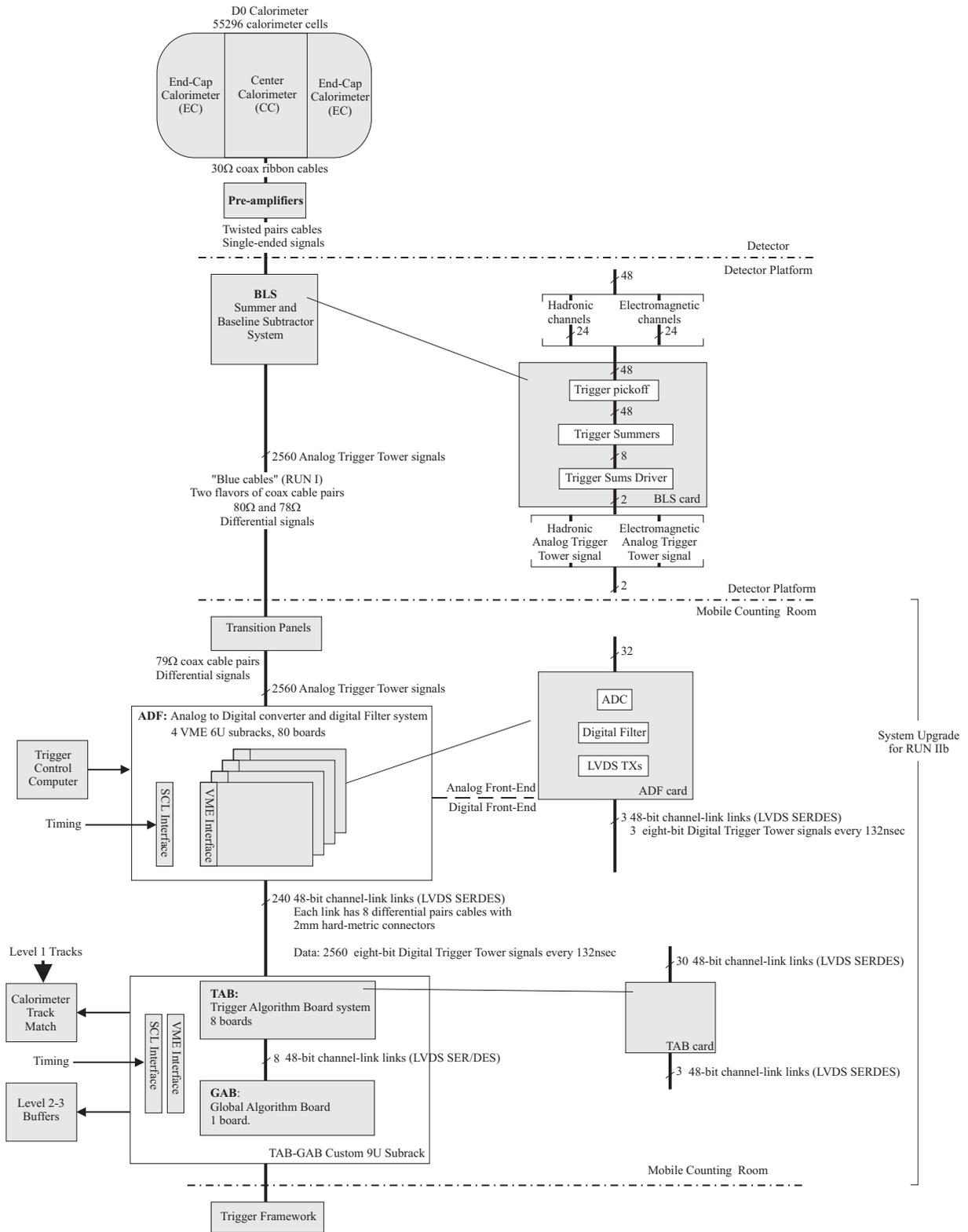


Figure 9.1, Calorimeter Level 1 Trigger block diagram

10 Glossary

ADF: Analog to Digital converter and Filter board. Component of the Run IIb D0 Level 1 Calorimeter System. See system diagram ().

BLS: Summer and Baseline Subtractor card. BLSs are a component of the Run IIb D0 Level 1 Calorimeter System. See system diagram ().

TAB: Trigger Algorithm Board. TABs are a component of the Run IIb D0 Level 1 Calorimeter System. A TAB run the physics selection algorithms on one eighth of the data produced by the ADF (Analog to Digital converter and Filter) boards. See system diagram ().

GAB: Global Algorithm Board. GABs are a component of the Run IIb D0 Level 1 Calorimeter System. See system diagram ().

SCL: Serial Command Link.

BSDL: Boundary Scan Description Language. IEEE 1149.1-1993b defines a language that describes IEEE 1149.1 architecture for an integrated circuit. This language is known as the Boundary Scan Description Language (BSDL). Updated BSDL files for the XILINX devices used on the Mixer Board can be found at:

http://support.xilinx.com/support/sw_bsdl.htm

EDIF: Electronic Data Interchange Format. Industry-standard for specifying a logic design in text (ASCII) form.

EM: Electromagnetic (calorimeter).

File types:

JEDEC files

JEDEC files are CPLD programming files generated by the CPLD fitter. They are ASCII text files containing programming information and, optionally, functional test vectors that can be used to verify the correct functional behavior of the programmed device. One JEDEC file is required for each device in the JTAG programming chain. The extension for JEDEC files is .jed.

BSDL Summary files

The Boundary-Scan Description Language (BSDL) files use a subset of VHDL to describe the boundary scan features of a device. The Xilinx JTAG Programmer automatically extracts the length of the instruction register from the BSDL file to place non-Xilinx devices in bypass mode. The JTAG Programmer locates Xilinx BSDL files automatically. The name of the BSDL file is assumed to be <device name>.bsd.

BIT Files

Bit files are Xilinx FPGA configuration files generated by the Xilinx FPGA design software. They are proprietary format binary files containing configuration information. One BIT file is required for each Xilinx FPGA in the JTAG boundary-scan chain. The extension for BIT files is ".bit".

(MCS/EXO) PROM Files

The Xilinx PROM file formatter generates PROM programming files. The files are ASCII text files used to specify configuration data. One PROM file is required for each Xilinx PROM in the JTAG boundary-scan chain. Use the device properties (Edit>Properties) dialog to specify the location of the MCS/EXO files for each Xilinx PROM. The required extensions for MCS and EXO files are ".mcs" and ".exo" respectively.

FPGA: Field Programmable Gate Array. An integrated circuit that contains configurable (programmable) logic blocks and configurable (programmable) interconnect between these blocks.

HD: hadronic (calorimeter).

IEEE: Institute of Electrical and Electronics Engineers, Inc. More information is available on the Internet:

<http://www.ieee.org/>

Jedec: The JEDEC Solid State Technology Association (once known as the Joint Electron Device Engineering Council) is the semiconductor engineering standardization body of the Electronic Industries Alliance (EIA), a trade association that represents all areas of the electronics industry. More information is available on the Internet:

<http://www.jedec.org/>

Jitter: The JEDEC Standard No. 65 (EIA/JESD65) defines jitter as the magnitude of the time deviation of a controlled edge from its nominal position.

JTAG: Joint Test Action Group. Older name for IEEE 1149.1 boundary scan, a method to test printed circuit boards and also integrated circuits. See also BSDL.

Design complexity, difficulty of loaded board testing, and the limited pin access of surface mount technology led industry leaders to seek accord on a standard to support the solution of these problems.

The standard defines a hardware architecture and the mechanisms for its use.

The standard itself defines instructions that can be used to perform functional and interconnect tests as well as built-in self-test procedures. Vendor-specific extensions to the standard have been developed to allow execution of maintenance and diagnostic applications as well as programming algorithms for re-configurable parts.

The top level schematic of the test logic defined by IEEE Std 1149.1 includes three key blocks:

The *TAP Controller*

This responds to the control sequences supplied through the test access port (TAP) and generates the clock and control signals required for correct operation of the other circuit blocks.

The *Instruction Register*

This shift register-based circuit is serially loaded with the instruction that selects an operation to be performed.

The *Data Registers*

These are a bank of shift register based circuits. The stimuli required by an operation are serially loaded into the data registers selected by the current instruction. Following execution of the operation, results can be shifted out for examination.

The *JTAG Test Access Port* (TAP) contains four pins that drive the circuit blocks and control the operations specified. The TAP facilitates the serial loading and unloading of instructions and data. The four pins of the TAP are: TMS (Test Mode Select), TCK (Test Clock), TDI (Test Data In) and TDO (Test Data Out). The function of each TAP pin is as follows:

TCK - this pin is the JTAG test clock. It sequences the TAP controller as well as all of the JTAG registers.

TMS - this pin is the mode input signal to the TAP Controller. The TAP controller is a FSM that provides the control logic for JTAG. The state of TMS at the rising edge of TCK determines the sequence of states for the TAP controller. TMS has an internal pull-up resistor on it to provide a logic 1 to the system if the pin is not driven.

TDI -this pin is the serial data input to all JTAG instruction and data registers. The state of the TAP controller as well as the particular instruction held in the instruction register determines which register is fed by TDI for a specific operation. TDI has an internal pull-up resistor on it to provide a logic 1 to the system if the pin is not driven. TDI is sampled into the JTAG registers on the rising edge of TCK.

TDO - this pin is the serial data output for all JTAG instruction and data registers. The state of the TAP controller as well as the particular instruction held in the instruction register determines which register feeds TDO for a specific operation. Only one register (instruction or data) is allowed to be the active connection between TDI and TDO for any given operation. TDO changes state on the falling edge of TCK and is only active during the shifting of data through the device. This pin is three-stated at all other times.

LVTTL: Low Voltage TTL. Is one of the several switching standards used in digital electronics.

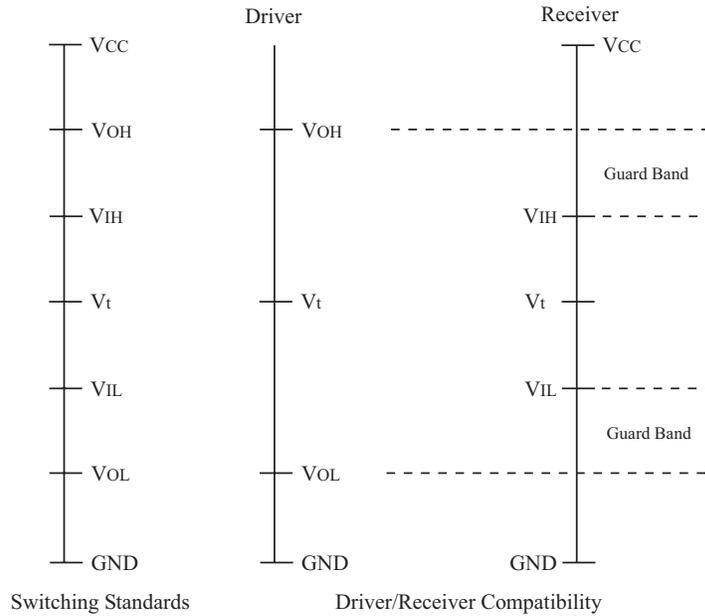


Figure 10.1, Switching standards.

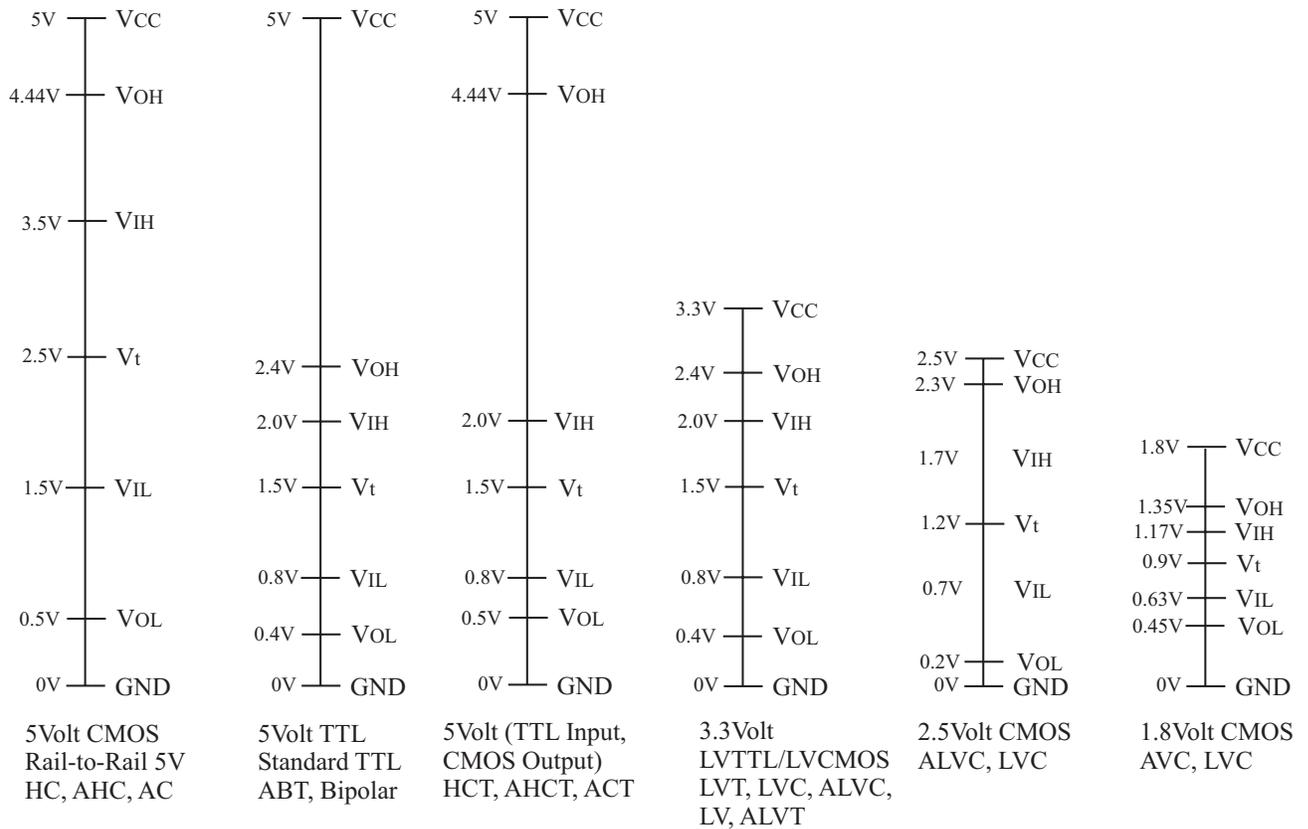


Figure 10.2, Comparison of switching standards.

MCU: Micro-Controller Unit.

Skew: The JEDEC Standard No. 65 (EIA/JESD65) defines skew as The magnitude of the time difference between two events that ideally would occur simultaneously.

VHDL: "V" stands for Very High Speed Integrated Circuit and "HDL" stands for Hardware Description Language.

VME/VME64X: [Ref.16] The VME (VERSAmodule Eurocard) standard was first defined in 1979 by Motorola Corporation. The VMEbus is an asynchronous bus that utilizes a *Master/Slave* architecture. The leftmost slot is the *Master*, and the remaining slots are *Slaves*. The VMEbus is composed of four sub-buses called the *Data Transfer Bus*, the *Data Transfer Arbitration Bus*, the *Priority Interrupt Bus*, and the *Utility Bus*. The original VMEbus standard maximum transfer speed is 40 Mbytes/sec. With the features of the newer VME64X standard described below, that transfer speed has quadrupled to 160 Mbytes/sec. Other features of VMEbus are:

-) 16, 24, or 32-bit addressing
-) 8, 16, 24, or 32-bit data path width
-) Allows unaligned data transfers
-) Error detection through *BERR signal
-) 7 levels of interrupts
-) System diagnostic capability using the *SYSFAIL signal
-) Mechanical standard allows 3U, 6U, or 9U printed circuit boards

The VME64X standard is a superset of the VME standard. Some of the added abilities for VME64X are:

-) Larger 64-bit data and address paths for 6U boards
-) 4 times the bandwidth (160 Mbytes/sec)
-) Cycle retry capability
-) Bus LOCK cycles
-) First slot detector
-) Automatic 'plug and play' features
-) A new 160-pin connector family
-) A 95-pin J0 connector
-) 3.3V supply pins
-) Geographical addressing
-) 141 more user-defined I/O pins

The VME64X standard utilizes 3 sets of connectors that plug into the backplane. They are a 95-pin connector J0/P0, and two 160-pin connectors, J1/P1 and J2/P2.

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