

Report on the 3 rd BTeV Workshop on Electronics and Associated Software  
Report date: 22 November 2000  
Report author: Michael Haney

The following timetable for the Muon Trigger development is also provided in the answers to the workshop questions:

Fortran (and/or C) description of muon trigger algorithm:	Dec 2000
C-code for DSP (full algorithm, assuming R-tracker done in DSP)	Mar 2001
HDL for R-tracker for FPGA implementation	Mar 2001
Decision point: can Pixel Trigger hardware be used by the muon trigger?	Jun 2001
Write up detailed cost/people/schedule details	Nov 2001

This timetable does not call for specific prototyping or electronic design activities, as none will be required unless the Pixel Trigger is found to be incompatible with the needs of the Muon Trigger. This evaluation will be made next summer, as indicated above. This should allow a suitable amount of time to make a preliminary design which can be "written up" in November, also as indicated.

Michael Haney will be responsible for the first drafts of the Muon Trigger requirements and preliminary specifications documents. It is not known at this time whether the Muon Trigger requires finer granularity than one of each. This work will be done in conjunction with the Pixel Trigger, to maximize the likelihood that the two subsystems can share hardware designs.

The highest priority issues for the Muon Trigger at this time are:

- an optical data source and receiver for end-end testing, or the commitment that one will be available
- DSP code development tools, and training
- the identification of standards, templates, and other common resources that the Muon Trigger will be expected to follow/use

The following pages address the specific questions from the workshop.

3 rd BTeV Workshop on Electronics and Associated Software

Session 2 - Thursday November 2, 2000 (1:00 - 4:30 PM)

Partial List Of Questions To Be Answered For Electronics & Associated Software Activities Prior To Baseline Review

(Electronics & software R&D plans and needs (including test beam needs) for Stage II approval)

**Answers with respect to the Muon Trigger  
Michael J. Haney, 22 November 2000**

**1) All Front-End Systems**

a) Milestones & Schedules: What are your milestones and schedule leading up to the February, 2002 Baseline review?

**see question 11 below**

b) Development and/or Test Beam Electronics and Associated Software:

(1) Tests:

(a) List all the tests (radiation, resolution measurements, beam, etc.) needed to be done along with the needed equipment

**none required if the Muon Trigger is located outside of the experiment hall**

**If portions of the Pixel Trigger are located in the experiment hall, then the Muon Trigger will share the same radiation concerns as the Pixel Trigger, and as such, limited radiation sensitivity testing may be called for. Specifically, placing prototype electronics in a location near a test beam, similar to the proposed site(s) in the experiment hall may be appropriate.**

(b) Do any tests involve combining detectors (e.g., beam test telescope may combine pixels & silicon strips)?

**only dose/rate information is expected to be relevant, if any testing is done at all**

(2) Needs: What is needed and when for testing front-end detectors and/or sensors at the bench and/or in a test beam: Include triggers, telescopes, etc?

**not applicable to the Muon Trigger**

(a) What hardware needs to be developed and tested?

(b) What commercial electronics needs to be assembled and tested?

(c) What software needs to be developed and tested?

(d) What work can be done in common with other systems?

(e) What Fermilab personnel and other resources are needed to accomplish pre-Baseline goals?

c) Custom ICs: What custom IC prototypes are needed prior to the February, 2002 Baseline review and by when?

**not applicable to the Muon Trigger**

d) BTeV-Standard Test Stands Or Not:

i) Fermilab has proposed a standard "test stand" using a PCI module to emulate a DCB for FEB testing. Are you likely to use this or would you be more inclined to use existing in-house test equipment?

**I would much prefer to use a standard test stand, if it were applicable to the needs of the Muon Trigger. However, it appears that the proposed test stand (the surrogate DCB) will not be applicable, and no plans appear to exist to provide other support (see below)**

ii) What is the latest date that a standard test stand could be available & still be useful?

iii) If you wanted to use the above test stand:

(1) When is the earliest that it and software for it would be needed?

(2) What software would be required?

(3) To both do the work and develop a more common FEB/DCB interface, what is the list of control, monitoring and readout functions to be performed on your FEB (see "Prototype Front-End Board Analog Section Needs")?

iv) Muon Trigger Testing:

(1) Will Fermilab provide support for muon trigger testing?

(a) Mock FEB/DCB/switch?

**No. The proposed teststand will be a surrogate DCB, and as such, will be of little or no value to the Muon Trigger development.**

(b) Simple optical data source?

**No. At this time, there appears to be no plans for Fermi to provide test infrastructure relevant to the needs of the Muon Trigger. Specifically, the Muon Trigger receives multiple optical data streams, and produces multiple optical data streams; an optical data source, and "reader" is vital for end-end testing. There are no apparent plans for these to be available from Fermi.**

**The Muon Trigger group has access to a 48-bit wide, 64K word deep, 42 ns cycle time pattern generator (Pulsar) from the CLEO-III trigger. It may be possible to develop a simple LVDS-optical interface to be driven by this device to produce a crude optical data source. However, there is a significant concern with respect to the SERDES and optical driver electronics.**

**If there is to be a "standard" footprint for such opto-electronics, supplied by/to the collaboration, then it would be extremely valuable for our interface to use this footprint.**

(2) If Fermilab is not supporting a trigger test stand, will the pixel trigger project develop a data source for test purposes? Will the muon trigger project develop a data source? Can they be the same?

**It should be possible for both the Pixel Trigger and Muon Trigger to use the "same" test hardware, and differ only in the software/content of the data streams.**

**However, it is unclear whether this will be developed by the Pixel Trigger group, or the Muon Trigger group, or at all.**

(a) What are the requirements?

**It is necessary to produce one or more optical data streams which will emulate the output function of the DCB(s) and switch(es). As such, the DCB-trigger protocol must be decided,. Further, if a standard SERDES-optical footprint will be made available for BTeV, this should be done prior to the implementation of the trigger test equipment.**

**Finally, an optical receiver would be of value, to interpret the results.**

(b) Who will do it?

**unknown. Perhaps UoFI. Perhaps it will not be done at all**

(c) When (timetable)?

**If prototype hardware is built for the (Pixel or Muon) Trigger, it would be valuable to have this data source in hand prior to or at that time**

e) Simulations of Electronics:

i) What, if any, simulation work needs to be done prior to the February, 2002 Baseline review?

**The Muon Trigger will be simulated by "conventional physics" means (Fortran) to determine efficiency and efficacy. HDL implementations will be simulated using the native design tools of the/an FPGA supplier (see question 10 below). DSP code will be emulated by the development tools, and may be evaluated on a vendor supplied EVM module.**

(1) Models, Analysis, and Simulations, (could possibly be deferred until Session 5): For the sake of using words consistently, "analysis" refers to means of

estimating/computing/determining parameters, whereas "simulation" emulates/reveals behavior which may be influenced by those parameters. "Models" describe (and sometimes, define) behavior, and may be applicable to either analysis or simulation, but it is unlikely that the same model would be applicable to both. "Validation" is the process of confirming that an implementation/model does what you want or expect; "verification" is the process of confirming that an implementation (lower level of abstraction) reflects the intent of a model (higher level of abstraction). "Functional closure" is the validation of the time-insensitive operation of implementation/model; "timing closure" is the validation of the time-sensitive aspects.

(a) What subsystems require queueing-type analysis to determine buffer depths or other parameters?

**Both the Pixel and Muon Triggers will benefit from a queueing analysis for the planning of buffer depths at various points along the processing path**

- (i) What other parameters?
- (ii) How will these analyses be performed? (Languages, tools, people, timetable)

**unknown at this time. The Pixel Trigger may perform an analysis; the Muon Trigger may be able to benefit from the Pixel Trigger group efforts. The Muon Trigger group does not have the tools or resources to perform a system or subsystem level queueing analysis at this time.**

(b) Is a system-level queueing-type analysis required? How will it be performed? (Languages, tools, people, timetable)

**It would be "better" if the entire BTeV Trigger/DAQ system were analyzed in some coherent manner, by people with expertise in this area. It is not known whether such people (or tools) are available.**

- (c) Where will analysis models come from? ,
  - (i) Written by the same people who do the analysis? (perhaps unwise)
  - (ii) Purchased from vendor? (for commercial elements, like network switches)
- (d) How sensitive is the system-level analysis to the trigger performance?
  - (i) What system requirements (e.g. buffer depths) are dictated by the trigger?

**unknown, but this may be important to the DAQ**

(ii) What trigger requirements (e.g. latency distribution) are dictated by the system?

**unknown, but this may be important to the Pixel/Muon Trigger**

- (e) What levels of simulation will be employed?
  - (i) FPGA level? (almost certainly)

**the Muon Trigger will perform HDL simulations of all FGPAs, using FPGA vendor supplied tools (see question 10 below).**

(ii) Chip-chip level, between FPGAs?

**see iii below**

(iii) Board level, including all FPGAs and glue?

**the Muon Trigger will perform Verilog (VHDL, only if required) board-level simulation of any boards developed for the trigger. This will include chip-chip level simulation.**

(iv) Interboard level, between boards?

(v) Subsystem level, including all boards?

(vi) Inter-subsystem level, between subsystems?

(vii) System level, including all subsystems?

**higher level simulation(s) are not planned at this time, but will be considered**

(viii) In what language(s)? Verilog, VHDL, C?

**Verilog (VHDL, only if required)**

(ix) What tools?

**Mentor Graphics Expedition Series tools (previously known as VeriBest)**

(x) Where will the simulation models come from:

1. Autogenerated for FGPAs?
2. Written by the designers? (perhaps unwise)
3. Purchased? (perhaps expensive)

**yes, yes, no (too expensive)**

(f) Will models be used to describe/define (sub)systems?

**no. Time, tools, and people power do not permit**

(i) If models will be used to define (sub)systems (specification by description), what is the timetable needed to complete the definitions?

**no**

(ii) Will simulation be used to verify that the implementations are consistent with the (sub)system description?

**no**

(iii) Will formal methods be used (instead of simulation) for verification? Which tools?

**no**

- (g) How will functional closure be achieved?
- (i) By simulation? At what level(s)?
  - (ii) By prototyping and revision?

**simulation will be used for board-level and below. At present, the Muon Trigger is thought to consist of at most one board-type distinct from the Pixel Trigger. The Muon Trigger will benefit from any prototyping efforts of the Pixel Trigger, but will probably not produce any prototypes of their own.**

- (h) How will timing closure be achieved?
- (i) By analysis? Which tools? Where will the models come from?
  - (ii) By simulation? Which tools? Where will the models come from? And where will the test vectors come from? Will test coverage be computed? Will there be "target level" of test coverage provided/required for each?

**timing closure will be assumed by FPGA simulation using the vendor tools, validated by time-testing of Pixel Trigger prototypes.**

- f) Prototype Front-End Board Analog Section Needs: (to be continued in Session 5):
- i) What is the required noise (in-) sensitivity?
  - ii) What slow and fast controls are required (e.g., individually-controlled threshold per channel, bunch crossing edge, charge injection)?
  - iii) What monitoring is required (e.g., read back of each analog threshold, temperature)?
  - iv) Must the monitoring information be returned via the data read back path or can it be via a separate link?
  - v) How many channels are to be read back?
  - vi) What read back information is required per channel?
  - vii) What is the average expected occupancy over the detector in a given area or over all detectors (e.g., planes) in your system?
  - viii) What are the expected fluctuations in occupancy over the detector in a given area or over all detectors (e.g., planes) in your system?
  - ix) What are the voltage and current requirements (levels and noise)?

**not applicable to the Muon Trigger**

## **2) Pixels:**

- a) Away From The Baseline Design: We have now moved away from the Proposal Baseline design as outlined in the Proposal.

- i) Are we in a position to have a new baseline design?
- ii) If so, what is the plan to verify that this change will work for us? iii) What are the fallback options?
- b) Data Controller or Data Compression IC or Not:
  - i) Do we need a controller chip or data-compression IC?
  - ii) If yes, do we need this for the baseline review?
- c) RF Pickup:
  - i) What level of RF pickup is acceptable in the pixel system?
  - ii) What are the tests we need to do and when should we expect to get some answers?
  - iii) Can we consider using shielding with given mass constraints?
- d) Grounding: What are the possible grounding strategies?
- e) Electronics Outside The Vacuum Vessel:
  - i) What is the radiation level?
  - ii) Can conventional electronics be used in this level of radiation?
- f) Single-Event Upsets:
  - i) What is the rate of SEUs
  - ii) What is the effect on electronics?
  - iii) How do we know SEUs occur?
  - iv) How long does it take to reset (or reload) from a SEU?
- g) Pixel Readout IC Documentation: When can a thorough specification be completed including architecture simulation results and studies of possible data losses and their sources?
- h) Laser Link Testing:
  - i) What is the scheduled completion date for all laser driver, PIN diode and optical link tests including a market survey, components testing before and after irradiation, and effect of SEW
  - ii) What is yet to do?

**(mostly) not applicable to the Muon Trigger. The only area of sensitivity is the "Laser Link Testing" as it relates to the development of end-end test infrastructure for the Muon (and Pixel) Trigger. See question 1(d) above.**

### **3) Particle ID (RICH):**

The baseline design calls for the use of HPD's, and most of the work in the next year and a half will focus on developing HPD readout. What, if any, work needs to be done on fallback or alternative solutions in the next year and a half

**not applicable to the Muon Trigger**

### **4) EM Calorimetry:**

**not applicable to the Muon Trigger**

### **5) Muons:**

#### **a) ASDQ IC:**

i) How can we be sure that the ASDQ IC is the right choice for the Muon front- end? What tests have been done and what are planned?

- ii) Will the ASDQ IC be able to be made when production quantities are needed or will its technology be obsolete and not available such that a new IC development is needed?
- iii) Who will do the ASDQ testing to insure that its operation matches or exceeds the requirements for the Muon system?
- iv) Are people aware of the new University of Pennsylvania ASD IC development? Who is to communicate with Penn regarding our requirements? This effort should be coordinated with Straw people?

**not applicable to the Muon Trigger**

**6) Straws:**

- a) ASDQ IC:
  - i) How can we be sure that the ASDQ IC is the right choice for the Straw front- end? What tests have been done and what are planned?
  - ii) Will the ASDQ IC be able to be made when production quantities are needed or will its technology be obsolete and not available such that a new IC development is needed?
  - iii) Who will do the ASDQ testing to insure that its operation matches or exceeds the requirements for the Muon system?
  - iv) Are people aware of the new University of Pennsylvania ASD IC development? Who is to communicate with Penn regarding our requirements? This effort should be coordinated with Muon people?
- b) TDC IC: Does the TDC IC need to be developed before the February, 2002 baseline review?
- c) Test Beam Electronics:
  - i) What PREP electronics is needed and when?
  - ii) What electronics needs to be developed?

**not applicable to the Muon Trigger**

**7) Strips:**

- a) The BTeV proposal says that the silicon strip detector readout will use the same scheme as used for pixel readout. This was understood to mean readout from front-end integrated ICs to a radiation-hard data combiner/serializer IC, whose output would be input to a VCSEL, which would drive an optical fiber. Similarly, control information was assumed to arrive at the edge of the silicon strip detector on fibers. It appears that the baseline pixel readout will soon be redefined to move the fiber interfaces out of the high radiation area. What does this mean for the silicon strip detector readout?
- b) How much functionality will be integrated into the front-end IC?
- c) What alternatives to the baseline design will be explored in the near term (for example, DC coupling)?

**not applicable to the Muon Trigger**

**8) Data Acquisition:**

- a) Will the trigger (silicon, Muon) contribute to the event data stream? How?

**the Muon Trigger should contribute intermediate information to the event data stream to support in-system diagnostics. An important mechanism for evaluating the trigger function is to have the actual input conditions (available from the L1 buffers) as well as various intermediate results produced along the trigger compute path. This feature must be controllable, at least to the extent of being turned off.**

**9) Control/Monitoring & Timing:**

a) Milestones & schedules: What are your milestones and schedule leading up to the February, 2002 Baseline review?

**not applicable to the Muon Trigger**

**10) Pixel Trigger:**

a) Milestones & schedules: What are your milestones and schedule leading up to the February, 2002 Baseline review?

b) Overall:

i) How different/similar are the Muon trigger needs? Where can we share tasks and how can we partition tasks to make effective use of both groups? -

**it may be possible for the Muon Trigger to be implemented using identical hardware recycled from the Pixel Trigger design. In one scenario, the Muon Trigger may be implemented entirely in DSP code, in which case the "FPGA Tracker" used by the Pixel Trigger could be reconfigured as a simple pass-through. All of the Muon Trigger function would be executed in a copy of the "tracker-farm". In a second scenario, the R-Tracker function of the Muon Trigger may lend itself to being implemented in the FPGA Tracker chip, off-loading work from the DSP farm(s).**

**In a worst-case scenario, the Pixel Processor/FPGA Tracker may be so completely different (mostly due to input data stream connections) from the needs of the Muon Trigger that an equivalent board (or boards) must be built for the Muon Trigger. Even in this case, however, it is fully expected that the tracker-farm and vertex-farm (or composite farm, if implemented as such by the Pixel Trigger group) will provide a more-than-sufficient resource for performing the remaining Muon Trigger function.**

ii) Where physically do the pieces of the trigger need to be?

**to avoid radiation issues, it is preferable for the Muon Trigger to be located outside of the experiment hall.**

**for "symmetry" reasons, the Muon Trigger should probably be co-located with the Pixel Trigger. If the Pixel Trigger is half-in/half-out, this may be appropriate for the Muon Trigger as well...**

iii) What fault tolerance needs to be built in? This is also an issue for the entire experiment.

**unless the Muon Trigger hardware is located in the experiment hall (where radiation effects are a concern), "fault tolerance" is the wrong way to think about the issues. Faults will not be "tolerated" (in general) by active redundancy and voting. It will be vital to detect faults quickly (checksums, CRCs, progress indicators), and to reroute (optical) trigger data to other electronics as quickly as possible in response to detected faults. It is unwise to think in terms of "rescheduling" a trigger decision by reissuing repeated data to a new DSP chip to take over for a failed one. The latency requirements placed upon the rest of the DAQ system could be prohibitive. (This should be evaluated quantitatively before making the design specification.) In the event of a failure, that event decision (and hence, that event) is forfeit. The key to performance will be to prevent a large series of forfeit events due to a single point failure, by rerouting as soon as possible. Early detection and available resources (hot spares, with optical cables attached) are critical.**

c) FPGA Pixel Processor:

- i) What sorting and tagging can be done here in order to simplify later processing?
- ii) What degree of cluster finding processing can we afford?
- iii) How do we select the best programmable chip architecture? Do there need to be specific simulations just for this section?

**It is not necessary to select the "best" architecture, or best device, either for the Pixel Trigger or for the Muon Trigger. What is vital is to develop the necessary trigger function in Verilog/VHDL/other, to implement that function on at least one member of an FPGA family. Given that baseline, one can safely assume that later FPGAs will be larger and faster.**

**This does imply one design requirement, however. It is vital that designs be relatively insensitive to device speed increases. This is often a painless constraint, which can be met by external timing elements (if time is critical).**

d) Track Finder & Processor Farm:

- i) What simulations need to be run to winnow candidate algorithms?

**at present there is only one Muon Trigger candidate algorithm; however, there are several parameters which have strong influence over the implementation. The effect of these parameters will be examined the by the Fortran simulations mentioned above (question 1(e)).**

- ii) What prototype tests need to be run to validate the processor simulations and how much prototyping needs to be done to support this?

**it would be appropriate to prototype the Muon Trigger "R-Tracker" FPGA to confirm that actual devices are better than the simulation-predicted speeds. It**

**is likely that this test could be performed using prototypes developed for the Pixel Trigger.**

iii) How do we select the processor hardware?

**DSP hardware should be chosen based on the tools available to effectively map high level (C) code for the trigger algorithm(s). The processor itself is a secondary consideration. If the tools are not usable, or you can not achieve the required performance using the tools, then it is irrelevant that DSP-A is "faster" than DSP-B. It is only relevant that DSP-B works...**

iv) What is the operating environment? (NT, Linux, VxWorks)

**some level of RTOS/scheduler/other will be needed to provide supervisory (and debug) support for the DSPs. It may be possible to write our own. The choice will critically depend on the I/O channel used from the DSP to the "slow control" or other communications system. If this channel is ethernet, for example, then writing a home-made TCP-stack may be foolish compared to buying one.**

v) Should we separate the track finding and the vertex finding or make cuts on the segments?

**not applicable to the Muon Trigger**

### **11) Muon Trigger:**

a) Milestones & schedules: What are your milestones and schedule leading up to the February, 2002 Baseline review?

<b>Fortran (and/or C) description of muon trigger algorithm:</b>	<b>Dec 2000</b>
<b>C-code for DSP (full algorithm, assuming R-tracker done in DSP)</b>	<b>Mar 2001</b>
<b>HDL for R-tracker for FPGA implementation</b>	<b>Mar 2001</b>
<b>Decision point: can Pixel Trigger hardware be used by the muon trigger?</b>	<b>Jun 2001</b>
<b>Write up detailed cost/people/schedule details</b>	<b>Nov 2001</b>

### **12) Software - Test/Development & System:**

a) Milestones & schedules: What are your milestones and schedule leading up to the February, 2002 Baseline review?

b) Have all people accepted the Front-End Board (FEB)/Data Combiner Board architecture proposal?

c) What are the schedule and milestones for your FEB prototype/production cards

d) Do any of the FEB diagnostics need to be accessible in the final data acquisition system?

e) Would you use the standard BTeV test stand to test the production quantities of your FEBs? Is this architecture sufficient for those quantities?

f) As FEBs are being developed and tested, will they be integrated in a "mixed architecture" environment - e.g., CAMAC, VME, etc? (editor's note: sure hope not!)

**as indicated above in question 1, the current test stand is not applicable to the needs of the Muon Trigger.**

g) Have people started to think about the amount of slow control data for each subsystem. What are the order of magnitudes?

**as indicated in question 10 above, some channel from the DSPs to slow control (or other) will be important, probably for initialization (code download), and certainly for debug.**

h) For Stage II milestones that include test beam activities, please provide the configuration of your test beam DA and data requirements (rates, storage, etc). Where will these DAs be brought up before moving to the final location?

i) How are people sharing their development work now? Is there a central CVS repository for BTeV software development (or is it only for offline)?

**unknown. I know where mine is... (i.e., we have a problem here)**

### **13) System Maintenance:**

a) Will Fermi provide space for test stands to allow board test/repair on site?

**unknown**

b) Will test stands be required on site?

**if sufficient hot-cabled-spares are in place, then remote servicing at home institutions is acceptable.**

### **14) Documentation Standards:**

a) What standards, if any will be required for:

i) (sub)system function?

ii) (sub)system performance?

iii) (sub)system programming?

iv) (sub)system test?

v) (sub)system repair?

**Question not asked: are there standards already that we should be following? Electrical? Mechanical? Safety? If so, where can they be found?**

3rd BTeV Workshop on Electronics and Associated Software

Session 5 - Friday November 3, 2000 (11:00 AM - 3:30 PM)

Partial List Of Questions To Be Answered For Post-Baseline Electronic & Associated Software Activities

(Production system electronics and software systems engineering issues)

**Answers with respect to the Muon Trigger  
Michael J. Haney, 22 November 2000**

**1) All Systems:**

a) Initial Requirements Documents: What are the initial requirements documents and preliminary specifications documents that should be written and reviewed for your system, its interfaces and its components?

**the Muon Trigger will produce requirements and specification documents in collaboration with the Pixel Trigger. One objective is to insure that the requirements of the Muon Trigger can be met by the specifications of the Pixel Trigger, and vice versa, if hardware design is to be shared.**

**Michael Haney is responsible for the first drafts of the Muon Trigger requirements and preliminary specifications documents.**

b) Laboratory Requirements For Fermilab Experiments (Session 4 Talk):

i) What issues discussed in the Session 4 talk are pertinent to your system?

**electrical, mechanical, safety. It will be vital for "someone" to decide which standards shall be mandated, and which are recommended, and to get this information posted to a common site (e.g. the BTeV web pages) as soon as possible so we all know the rules. Otherwise, we will all be making them up as we go...**

ii) Are there any other issues that were not discussed in the talk that pertain to your system?

**unknown. As I have not designed electronics for Fermi in the past, I don't have native experience in dealing with as-yet-unknown Fermi rules. The sooner these are enumerated, the better.**

iii) Based on the presentation of Session 4, what other support systems (e.g., ES&H) are needed for your system?

**the Muon Trigger should require essentially the same support as the Pixel Trigger, whatever that may be**

## 2) All Front-End Systems:

### a) Edge-To-Edge Timing:

- i) For acquiring data what bunch-crossing edge-to-edge timing accuracy is needed within a given front-end system, between your front-end system and other front-end systems?
- ii) How many different copies of the bunch-crossing clock will be used in your system?
- iii) List the places that will be responsible for adjusting the phase of the beam- crossing clock. How fine will the phase adjustment increments need to be?
- iv) How will the proper phases be determined?

**for the Muon Trigger, the data must correspond to a 132 ns bucket. I can not answer beyond that, as I don't fully understand the question.**

### b) Data Combiner Board (DCB) Placements On The Detector:

- i) Where (physically) on the detector can DCB modules be placed?
- ii) Are these locations easily accessible?
- iii) What is the overall MTBF requirement?

**not applicable to the Muon Trigger**

### c) Production Custom ICs:

- i) What are the major required features of your custom ICs?
- ii) When are production quantities of custom ICs needed?
- iii) Who will be doing production testing?

**not applicable to the Muon Trigger**

- d) Common Electronics To Minimize Costs: Are there areas where production costs can be reduced by coordinating work between various subgroups?

**most if not all of the Pixel Trigger will be recyclable for the Muon Trigger. The worst-case at this point is that the Pixel Processor/FPGA Tracker board may need to be different for the Muon Trigger.**

### e) Prototype & Production Front-End Board Analog Section Needs:

- i) Continuation Of Questions From Session 2
- ii) What requirements might be common to other front-end systems?

**not applicable to the Muon Trigger**

- f) Constraints & Other Issues In Putting Electronics On The Detector (continued from Session 1 talk by Chuck Brown):

- i) What are the space, vacuum, radiation vs. radial distance, radiation vs. downstream distance from collision point, temperature, etc. constraints of mounting electronics on the detector?
- ii) What are the distance limitations from sensors to FEB analog ICs?
- iii) What are the constraints due to cabling, support and-other mechanical issues?

- iv) What are the EMI issues, both those due to your system radiating noise into other systems and other systems radiating noise into your system?
- v) What special powering requirements do you have (e.g., high common-mode and/or EMI nearby, vacuum, radiation)?
- vi) Discuss grounding and shielding issues for the FEB electronics, the sensors and the detector itself
- vii) Where does electronics for each front-end system reside?
- viii) Support Systems:
  - (1) For each front-end system, what is the list of support systems requiring commercial and/or developed electronics?
- ix) Monitoring 'Points':
  - (1) What is the list of front-end and support electronics that need to be monitored?
- x) Powering & Cooling: What are the powering and cooling issues associated with your front-end system?

**not applicable to the Muon Trigger, unless the Pixel Trigger chooses to locate hardware in the experiment hall**

g) Readout Methodology:

- i) Problems & Issues: Discuss the problems and issues (e.g., noise, space, number of cables from FEBs, reliability) dealing with the following readout methodologies:
  - (1) FEBs with (shielded) analog sections, data combiner logic and, for example, 16-bit word readout to Data Combiner Boards (DCBs)
  - (2) FEBs with only analog sections and translators for driving data to DCBs (e.g., 32-channel boards will have 64 wires {32-pair} to a DCB)
  - (3) FEBs with (shielded) analog sections, data combiner logic and 100s of MHz serializers to send data to DCBs (e.g., 16-pairs {16-bit words} at 53 MHz vs. 2-pairs {2-bit words} at 8 x 53 MHz) (editor's comment: please give this readout methodology extra consideration as it may have significant advantages with respect to. reliability and cost; separating digital readout noise from the analog section should be able to be accomplished without needing extraordinary measures)
  - (4) Should all front-end system electronics other than pixels and perhaps strips be subrack-based? What would be the advantages and disadvantages in doing so?

**not applicable to the Muon Trigger**

h) System Reliability & Maintainability:

- i) Do you plan to do a mean-time-to failure (MTTF) analysis of system components?

**not at this time**

- ii) Do you plan for any type of redundancy?

**hot spares, attached to extra optical cables, may allow quick reallocation of duties simply by changing destination addresses (switch routing).**

- iii) Do you plan to do an analysis of failure modes?

**not planned at this time. However, it is planned to study fast fault-detection schemes, to promote early problem identification.**

iv) How much of your system can fail & still produce acceptable physics?

**unknown. It is expected that the Muon trigger will be fully inter-octant independent. Hence, a worst-case point failure will result in 1/8 of an arm (1/16 of the system) being unable to contribute triggers.**

v) How easily will your system be maintained in the field?

**it will be no worse than the Pixel Trigger**

i) BTeV Grounding: The experiment as a whole should work out a common grounding strategy. Discuss this issue and give feedback regarding a grounding strategy in your report.

**if the Muon Trigger is not located in the experiment hall, it will be connected by optical links, and as such, only local grounding will be relevant. Grounding will not be a critical issue. Shielding, on the other hand, could be critical, due to the high speed signals being serviced.**

### **3) Pixels & Strips - Electronics Commonality:**

Why can't pixel and strip front-end electronics control, monitoring and/or data readout be similar or identical in many respects to each other?

**not applicable to the Muon Trigger**

### **4) Strips & Straws - Strip Readout Over Straw Detectors; Mechanical Supports, etc:**

What issues are there in strip electronics control, monitoring, and powering cabling, cooling 'pipes', etc. running passed straw detectors?

a) Is it possible that the mechanical interface and supports between the two can be shared to help both system's electronics and powering issues? Is this desirable in that it may 'connect' the two systems during development, installation and commissioning in a way that adds cost and/or time to the project?

b) What are the current thoughts regarding some Forward Tracker planes having no straws or having larger straws, or having more strip area?

**not applicable to the Muon Trigger**

### **5) Pixels:**

a) Specification needed:

i) When can we have a system and electrical specification that includes?

(1) Types of ICs including technology; is Peter Denes IC not going to be used?

(2) How many COTS parts?

(3) What is the expected radiation dosage?

(4) What are the operating conditions (including power supplies and the various other components)?

(5) Noise and uniformity of the various parts, links?

(6) What is the number of links and their bandwidths?

(7) How many cables per module and half-plane?

**not applicable to the Muon Trigger**

b) Interface to Pixel Trigger:

i) What is the pixel electronics to pixel trigger interface?

ii) Do we need a pixel Data Combiner Board that collects and processes pixel data from multiple MCMs (shingle hybrids) & sends data optically to the pixel trigger?

iii) What processing functions might be included on the Data Combiner Board?

iv) How close will the Data Combiner Board be located to the detector? Where? v) What is the best architecture to minimize signals going to the trigger processor?

**although not asked, the Muon Trigger does have an interface sensitivity. Since the Muon Trigger will be octant-specific, it will be vital that all-and-only octant-specific data streams be made available. If the data combiners (DCBs) improperly couple multiple octants of data for the sake of bandwidth, it will be absolutely necessary to invert that mixing at the earliest possible stage. It is therefore strongly recommended that the DCBs "waste" bandwidth and fibers, as needed, to preserve octant specificity.**

c) Commonality with Strip Readout: Do we plan to use the same data combiner board or do we still plan to use a data compression IC?

**not applicable to the Muon Trigger**

d) Commonality With Pixel Readout: Why can't strip front-end electronics control, monitoring and/or data readout be similar or identical in many respects to that of pixels?

**not applicable to the Muon Trigger**

**6) Particle ID (RICH):**

**not applicable to the Muon Trigger**

**7) EM Calorimetry:**

a) Possible Modification To Proposal Conceptual Design Readout: EM Calorimetry electronics was packaged in subracks for costing purposes. Is there any reason that this electronics cannot be packaged without using subracks as was done on all other front-end systems?

**not applicable to the Muon Trigger**

## 8) Muon:

a) Cost: We've discussed a lot of options for reading out the detectors and at one point there was supposed to be a cost comparison of the various techniques. If we are to answer one of the most important considerations for the Muon detector in this meeting, any proposed solution other than the baseline should be accompanied by a cost estimate for the suggestion.

**the Muon Trigger needs (per octant) a list of the wires that are hit during the "current" 132 ns window. If this is met, the above is not otherwise applicable to the Muon Trigger.**

b) Noise & Radiation Damage: The question of needed signal to noise ratio is a tougher one to tackle in a detector where you expect radiation damage. There is some worry that we will try to cut our margin to save a few dollars and regret that decision when the detectors start to get damaged. From the Muon system standpoint, this means raising our gain to compensate for a higher noise floor. Sure we can do it, but the tubes run at higher gain and the higher the gain in the gas volume, the faster the damage accrues (see 'Heat' below).

**not applicable to the Muon Trigger**

c) Heat: This is probably not a big problem for the Muons system (1.2 Watts/plank), but we might want to start thinking about the overall heat budget for CO. (Especially with all the conventional magnets in there too!) Perhaps low- power components should be used where possible. Also we should try to keep down the number of auxiliary power modules such as voltage regulators and DC- DC converters. Can we use conventional cooling at all in CO? For silicon, at least in FOCUS/E83 1, temperature was a very important if we wanted to keep the detector quiet.

**not applicable to the Muon Trigger**

d) Space: Where are we going to put all the DC we need?

**not applicable to the Muon Trigger**

e) Magnets: We have many magnets.

i) Will the electronics work in their environment?

ii) Are we going to get the famous 100s of kHz noise from these, magnets? Is this in our noise budget?

**not applicable to the Muon Trigger**

## 9) Straws:

a) ASDIC: What are the requirements of the Straw ASD IC?

**not applicable to the Muon Trigger**

## 10) Strips:

a) Strip IC:

- i) What are the requirements of the strip readout IC?
- ii) When are prototypes of the IC needed?

**not applicable to the Muon Trigger**

**11) Data Acquisition (All also "Front-End Systems" questions):**

a) Trigger Data From Other Front-End Systems: The L1 Trigger uses pixel and Muon data. Is there a possibility that data from any of the other four detectors will ever be needed at Level 1?

**not applicable to the Muon Trigger**

b) More Common Front-End Board / Data Combiner Board Interface:

i) There are currently several versions of Data Combiner Boards (DCB) proposed, one for each detector. Can the number of channels per Front-End Board (FEB) or the number of FEBs per DCB be adjusted slightly to allow common DCB designs?

ii) Some subsystems use parallel links for the FEB to DCB connection. Is this an absolute requirement based on cost or noise issues?

iii) Can the FEB output be serialized (at 106 or 212 Mbps) on one or more links?

iv) If serialization is an option, can the channel count per FEB be adjusted to better match the link speed?

v) If digital noise is a concern, can the FEB prototype be designed with both parallel and (removable) serial output logic?

vi) If serialization logic is present on the FEB, can/should data-sparsification be done there also?

**not applicable to the Muon Trigger, except to the extent that the octant-specificity of the Muon Trigger may call for "wasted" DCB/fiber resource, so as to keep all-and-only octant-specific data on individual channels.**

c) No Prototype Data Acquisition System: We currently have no plans to produce a prototype of the final DAQ system for use in beam tests. This allows the DAQ development to proceed in parallel and at the same rate as the detector development. Are there objections to this?

**no objections**

**12) Control/Monitoring & Timing (All also "Front-End Systems" questions):**

The timing component of the Control/Monitoring and Timing system (CMT) will provide, at a minimum, a synchronous clock (53 or 106 MHz) with a bunch-crossing signal:

a) Does any front-end system require more precise timing information?

b) Can these signals be generated locally (on the FEB) using the basic CMT signals? c) If not, what resolution is required?

**not applicable to the Muon Trigger. If faster clocks are required, they can be self-derived (PLLs). They are not relevant to timing measurement, but only to allowing multiple pipe-steps per 132 ns.**

### 13) Pixel Trigger:

### 14) Muon Trigger:

as indicated above, the Muon Trigger is octant-specific (8-fold symmetric, per arm). It is necessary that the trigger data be delivered in this form. Further, per 132 window, a list/bitmap/other of hit wires is needed.

**It is expected that the Muon Trigger will have been implemented using Pixel Trigger hardware, with at most one replacement for the Pixel Processor/FPGA Tracker. If this is true, then most of the infrastructure, support, and maintenance requirements of the Pixel Trigger will be shared/common with the Muon Trigger.**

### 15) Software - Test/Development & System:

Some software requires a large lead time for development. This schedule needs to be incorporated into hardware milestones:

- a) The switch?
- b) Configuration management of thousands of DSP or Intel processors or other?
- c) Slow controls. It doesn't seem to me that there is a responsible person from BTeV for this piece yet it is not a small effort.

**Questions not asked: DSP development environment? DSP RTOS? A significant amount of infrastructure must be built and maintained for and around the "firmware" of the system. This will need to be done sooner rather than later...**

### 16) System Maintenance:

**most of the Muon Trigger maintenance should be board-swap. If faults are detected quickly and tasks are rerouted to already-cabled spares, then front-line maintenance is reduced to pulling and replacing the faulty board. Back-room diagnosis and repair, however, will require better testing infrastructure, which is only hinted at in this report.**

### 17) Documentation Standards:

**I should hope so...**