

BTeV RICH Front End electronics report

Date: 11/21/00
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From: Marina Artuso
RE: BTeV RICH front end electronics

Introduction

The BTeV Ring Imaging Cherenkov Detector (RICH) baseline design adopts HPD's as photosensitive devices. To achieve the desired spatial resolution, DEP will develop a custom made HPD including 163 pixels within a surface area of 200 cm^2 . Its design is based on the 61 channel HPD now commercially available, where the signals are brought out of the vacuum enclosure with pins organized in rows with 0.1 inch centerline separation.

The HPD signal properties that are relevant for the front end electronics design are the low level of the expected analog signal and the relatively high maximum occupancy expected in the hottest region of the detector. The expected signal level is about 5,000 electrons. Thus a low noise front end electronics is necessary. Although the average occupancy of the BTeV RICH detector is very small (0.34% hits/pixel), in the hottest HPD the number of hits in an event can be as high as 46, with 10 % of the events having more than 12 hits per tube, according to a Monte Carlo simulation based on our present projection for the interaction rate in our experiment. We have decided to address the needs of the high occupancy region in our initial R&D effort. The design that is discussed below is geared towards the maximum expected hit rate.

Milestones towards the baseline

We have identified the following important milestones to be accomplished prior to the BTeV Lehman review.

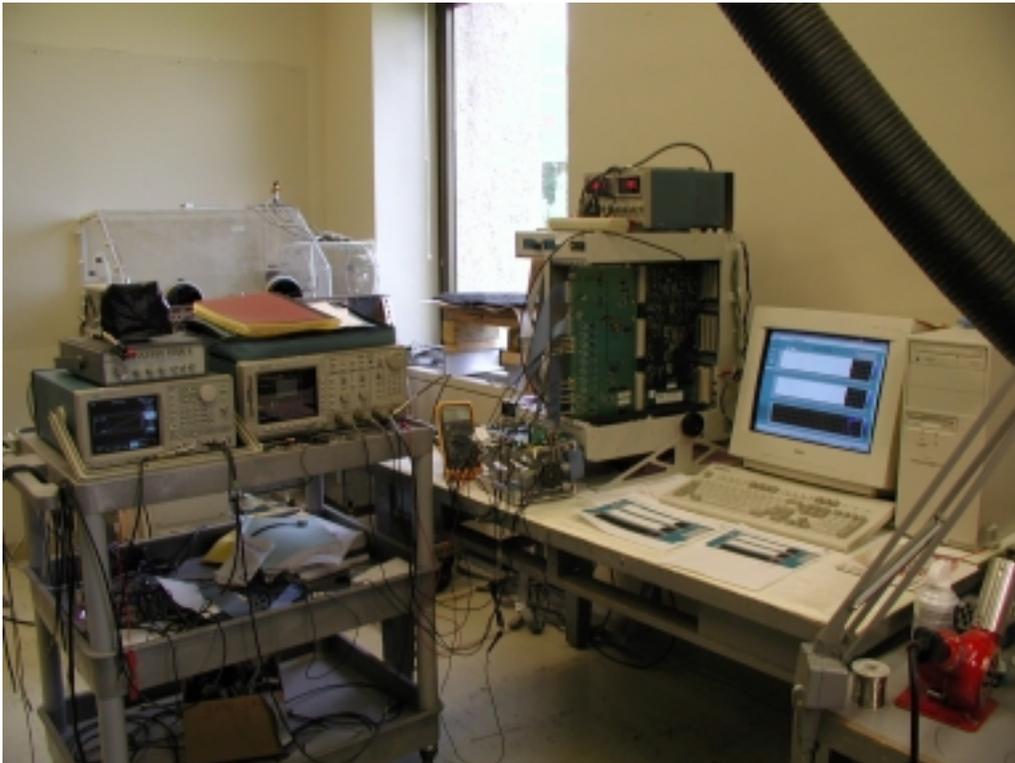
1. We need to test the analog performance and data transfer procedure of the VA-BTeV front end hybrids described in Appendix I. Towards this goal we have ordered 2 prototype hybrids to be delivered between April and July of 2001. In order to provide timely feed-back to IDE AS, that will produce the front end ASICs and the hybrids for us, the Syracuse group is planning to develop a test stand comprising a PC using Labview as data acquisition and visualization software and a Fermilab prototype PCI test cards, emulating some of the functions to be implemented in the data combiner boards. The testing procedure will involve a separate test of the front end electronics system using the calibration procedure described in Appendix I, followed by a bench test of the whole system.

2. We would like to finalize the choice of high voltage power supplies. The most promising candidates are the power supplies being developed by CAEN, but we are looking also into promising alternatives.
3. We would like to get a preliminary design of the routing of the different cables, choose the type of cables to be employed in signal transmission, low voltage and high voltage power distribution. This goal has different facets. We need to have a preliminary design of the support structure for the front end electronics hybrids, addressing the issues of strain relief of the circuit and connectors involved and of access to individual areas needing inspection. In addition we need to choose a suitable location for the power supply distribution boxes and data combiner crates. The cable plant needs to be scrutinized not only in terms of the mechanical reliability of the whole apparatus, but also in terms of electrical performance of the power distribution system. We need to finalize the multiplexing of the power supplies used, the grounding scheme, as multiple grounds are involved and a clean reference is necessary for the low noise front end electronics. In addition the multiplexing scheme needs to be studied for reliability and potential efficiency loss for individual power supply line failure.

The hybrid test set-up at Syracuse University

The high energy physics group at Syracuse University has a long experience in qualifying analog front end devices, both in terms of performance and of reliability. The system shown in Fig. 1, presently including a PC driving a VME crate with a LABVIEW based data acquisition system, will be modified to include a LABVIEW based data acquisition system including the PCI test card being developed at Fermilab. One important optimization issue that we need to address in the first evaluation phase of the front end electronics is how to structure the "intelligence" included both in the front end hybrids and in the data combiner boards. The Syracuse group is planning to work in close consultation with IDE AS and Fermilab to achieve the most efficient partition between these two functions.

Fig. 1 The FPIX test stand at Syracuse



Post Lehman review issues

Spring 2002 test beam

We are planning a test beam at Fermilab in the spring of 2002, involving about 25 HPD units instrumented with VA-BTeV front end hybrids. It is not crucial to accomplish this goal prior to the Lehman review, as we are planning to use proven technologies adapted to our goals. However it is important to get an early experience in the issues involved in obtaining optimal performance of the system that we are proposing. To this purpose we will need in a relatively quick time scale to produce enough HPD's and front end devices to satisfy our goals. In addition, we need to make sure that we will have a data acquisition system suitable for this application.

Testing procedure

We will need to define carefully the testing methodology and how to assess the reliability of the individual components. In particular we will investigate burn in procedures, temperature failure modes and other tests that will insure reliable performance in the course of the experiment lifetime. This is very important because even in the best scenario it will be hard to have frequent access to individual HPD units.

APPENDIX I

The VA-BTeV hybrid

The conceptual design of the VA-BTeV front end hybrid is shown in Fig. 2. It is based on a rigid-flex hybrid. One rigid section hosts the analog front end and a level translator chip. They are both described below. In view of the expected maximum occupancy, this section has a binary parallel output, that is linked via a flex section to a local FPGA based processor cluster. This generates a time stamp and serializes the information to be transmitted to the data combiner boards to be developed at Fermilab. These data combiner boards are processing the information received from 6 HPD's and are located in the vicinity of the detector. In the present design, the data are expected to be transmitted as differential digital signals via a ~ 1m copper cable.

The Va-BTeV chip

The key element to achieve the desired performance of the front end system is the Va-BTeV chip. It features a low noise analog section, a discriminator with individually tunable thresholds and parallel digital current output. The electrical specifications of this device are summarized in Table I. This chip has no clocked digital signals and current outputs, thus minimizing cross talk and digital feedthrough. It is shielded from the subsequent section that is mostly digital.

Table I - Specifications of the analog performance of the VA-BTeV chip

Noise	ENC = 500 e ⁻ at C _{in} =10 pf
Peaking time	75 ns
Fall time (@ 10%)	200 ns ¹
Threshold uniformity	±200 e ⁻
Threshold nominal value	3000 ²

¹ The important constraint as far as timing is concerned is **that the hit is associated only with the right beam crossing (no double firing) and that it takes no more than 1 additional beam crossing to be ready to record the next hit.**

² We would like to be able to scan the threshold over the whole dynamic range of the front end to be able to measure the electronics noise. An item for discussion should be the transfer characteristics of the DAC responsible for the threshold tuning.

The bias currents and voltages determining the chip performance and the individual thresholds will be tuned with internal DACs, to be initialized with control streams coming from the data combiner boards. The protocol of the initialization sequence will be finalized in collaboration with Fermilab.

The Level Translation ASIC

This chip is a simple parallel in-parallel out level translator taking the current output from the channels hit and transforming them in digital levels suitable for the FPGA section downstream.

The FPGA section

In order to cope with the maximum rate envisaged for the inner portion of the BTeV RICH, it is necessary to introduce a local digital section that will decode the address of the channel hit, attach a time stamp and send the information to the data combiner board in asynchronous fashion. The proposed data structure is a header data word including a time stamp and a string of addresses corresponding to the pads having a signal. In addition we would like to include in the hybrid a local memory to identify the hybrid in the data acquisition system database. It is important to identify in this initial R&D phase the optimal partitioning of logical functions between the data combiner boards and the front end hybrids. We would like to include a local memory for electronic book-keeping purposes.

Communication with the data combiner boards

The data combiner boards combines data from 6 HPDs for further processing. In addition, it provides a synchronization clock to enable the digital section to issue a time stamp for the data, and drives the initialization sequence and performs other ancillary slow control functions to monitor the status of the analog front end. We should define a pinout for these prototypes that allows us to use commercially available cables and connectors (e.g. 50 pin cable/connector units) that include three group of signals:

1. Data i/o signals (for instance 16 data lines that transmit the channel hit information to the data combiner board in data acquisition mode and initialization pattern from data combiner board to the chip). These lines can be used also to reprogram the fpga in the chip.
2. Mode lines that define which operation needs to be performed:
 - a. Initialization
 - b. Chip ID interrogation
 - c. FPGA reprogramming
 - d. Reset
 - e. Data taking
3. BCO clock for chip time stamp.

The hybrid needs also good quality analog voltages, the reverse bias for the silicon sensor in the hpd cable.

We need to discuss the communication protocol for all the modes of operation together with IDE AS to obtain the most efficient solution to work with their standard initialization protocol. We need to simulate the data taking protocol to insure that the only loss of information occurs in the very unlikely case of having a channel being hit during two consecutive beam crossings.

Figure 2:
Conceptual diagram of
BTeV RICH front end
hybrid

