

DAQ Summary - Session 2

The goal of the workshop, with regard to the DAQ system, was to resolve questions of commonality in the detector interface and placement of downstream components. These decisions are needed before any additional functional specifications or cost estimates can be generated. Options for a common Data Combiner Board were discussed with each detector group.

Developing a BTeV standard test card (DCB emulator) for use in production testing of front-end modules was also discussed. There was some interest in making this available earlier, for prototype testing. If this is the case, the interface will be a generic parallel cable...not necessarily the final DCB input standard.

The issue of slow controls has not received much attention prior to the workshop. This will be a major effort, especially in software development.

For fast control, most subsystems need only the crossing clock and a "bunch zero" reference for start/stop synchronization of counters and beam gap location.

Session 2 Questions:

Will the L1 trigger contribute to the event data stream? Answer: Yes. Intermediate results may be captured to allow verification of L1 operation and to provide a "head-start" for L2 processing.

Schedule and Milestones through the end of 2001.

The DAQ design is based on commercially available digital components. There are no custom integrated circuits or unproven technologies. For this reason, we expect to do only minimal prototyping before starting production designs. In most cases, extensive simulation will be done in place of prototyping.

Functional Specification - July,2001

Single document containing a description of general system operation (system architecture, data and control flow) and functional specifications for each component.

Preliminary Simulation Results - November,2001

Single document containing simulation results for components of the architecture which directly affect the cost estimates. For example, simulations of buffer operation to determine minimum FPGA size/speed requirements and memory width.

Prototyping - Informal, no milestones.

We plan to evaluate parallel optical links, DDR SDRAM and high density FPGAs (most likely using a vendor evaluation board). The main goal will be to have all the necessary development and test tools in place before production designs start.

DAQ Summary - Session 5

Session 5 Questions:

Is there a possibility that data from any of the other four detectors (RICH, calorimeter, straws, strips) will be needed at Level 1? Answer: Yes, straws and strips may be used to refine the pixel trigger. Calorimeter data may be used in a separate trigger.

Can the number of different Data Combiner Board designs be reduced? Answer: Doesn't appear likely. If anything, the DCB requirements seemed to diverge even more during the workshop.

Can FEB to DCB data be serialized (more than currently proposed)? Answer: Serialization requires some level of sparsification at the FEB. There is reluctance to do this, mainly because some FEBs will suffer very high occupancy and sparsification would do little to reduce the data rates from these boards. The present choice then, is to design the FEB-DCB links for "worst case" (non-sparsified) data rates. Links will then be organized so that there is a balance of high and low occupancy FEBs driving each DCB, and sparsification will be done in the DCB. This results in approximately 500K wires and 1M connector pins for FEB-DCB connection, so alternatives should still be considered.

The DCBs will probably remain application specific. FEB designers seem willing to consider a standard, serial input DCB, but in each case it would require some sort of intermediate module to convert FEB data to the standard DCB format. This adds another level of hardware, which would be no more efficient than designing different DCBs for each front-end.

A second issue was placement of the L1 Buffers, especially for subsystems not involved in the L1 trigger. An often asked question is why this data is being transmitted a long distance over fiber links and then discarded, instead of simply discarding it at the source. The justification is that the data may indeed be used at some future point in the L1 Trigger. Also, accessibility of L1 Buffers seems to be a concern.