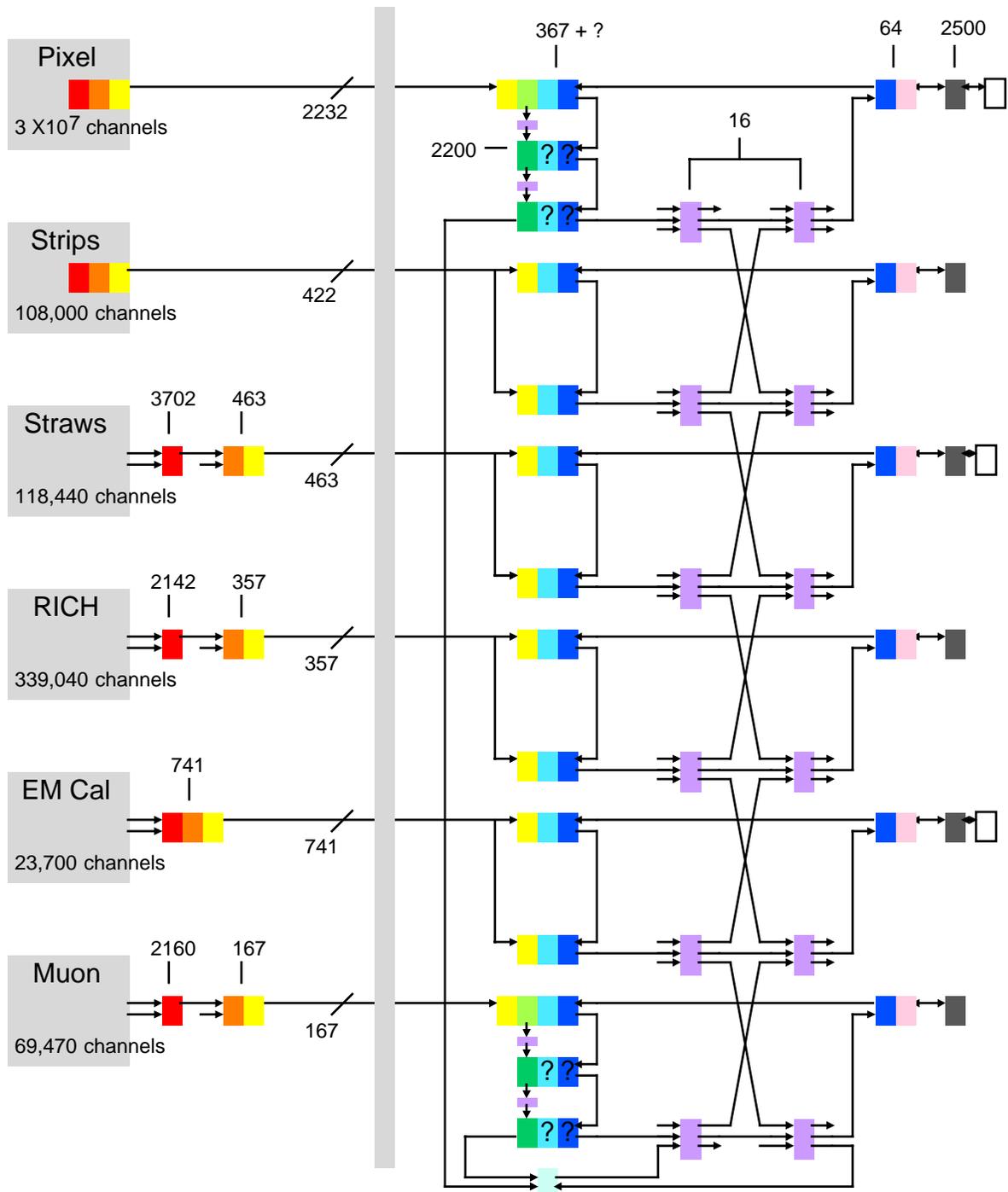
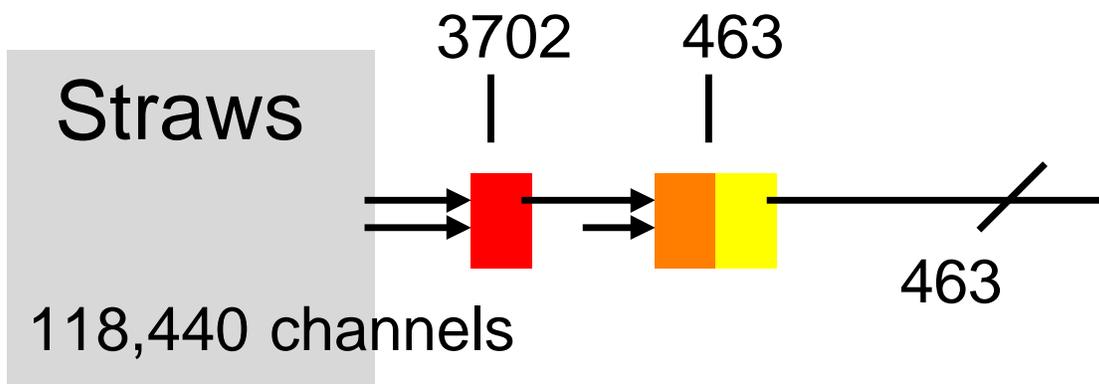
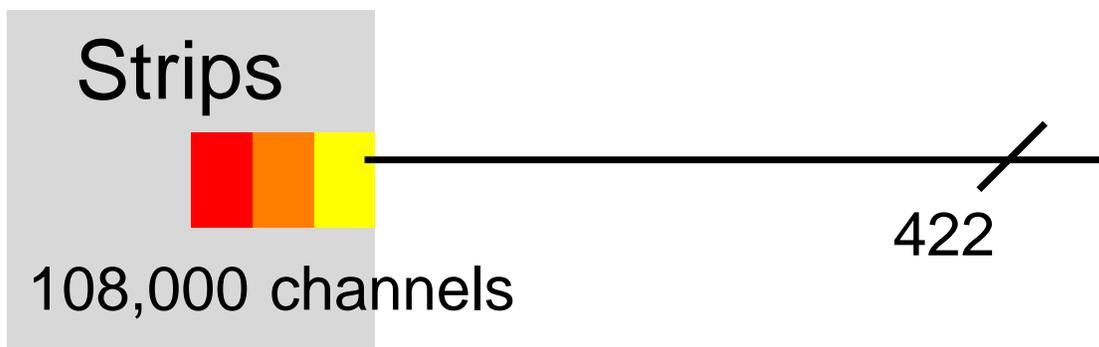


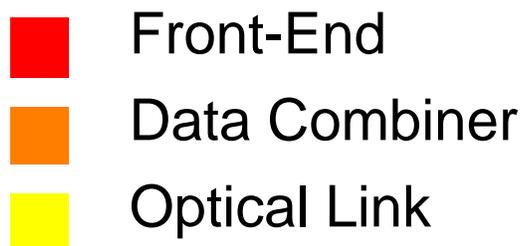
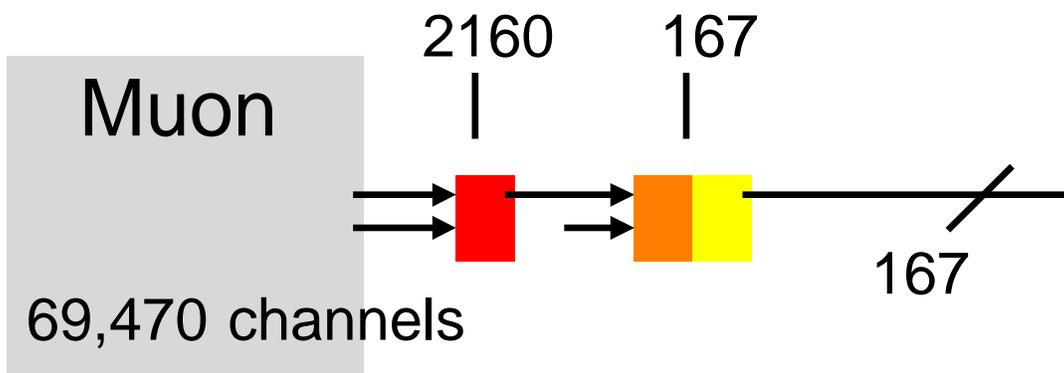
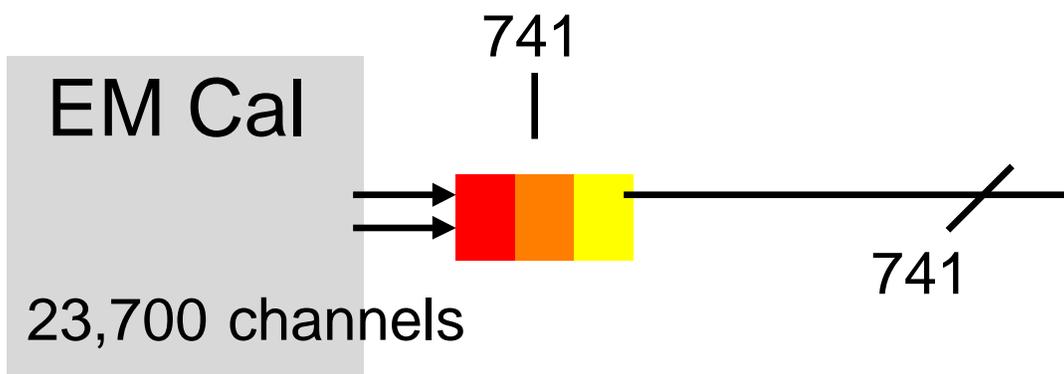
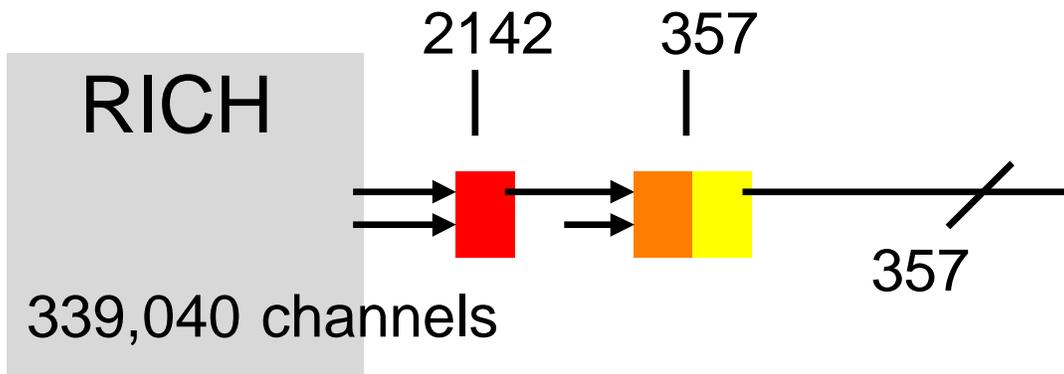
Simplified Baseline DAQ/Trigger



- | | |
|---|--|
| ■ Front-End | ■ Event Supervisor & Monitor (Global Trigger) |
| ■ Data Combiner | ■ Switch Buffer |
| ■ Multichannel Optical Link | ■ Switch |
| ■ L1 Trigger (FPGA stage) | ■ L2 Buffer |
| ■ L1 Trigger (DSP stage) | ■ L2/3 Processor |
| ■ L1 Buffer | Storage |



- Front-End
- Data Combiner
- Optical Link



DCB Consolidation

Data Combiner Boards (DCBs) have been defined for several subsystems.

Proposal used different DCB designs for each subsystem to match data rate and detector pitch.

Goals

- 1) reduce number of different DCB designs.
- 2) increase serialization of data from FEBs to DCBs to reduce cables.

Can prototype FEBs be designed with both parallel and serial outputs to prove that digital noise is or isn't a problem?

DCB Consolidation

The 3 subsystems currently using DCBs each have different FEB outputs.

Muon 32 bits x 7.5 MHz,
 13 links/DCB

RICH 12 bits X 106 MHz

Straws 32 bits X 53 MHz

Total signal lines/connector pins > 500K/1M

Can some sparsification be done at the FEB?

Can we define a standard FEB to DCB serial link?

DCB Consolidation

Pixel and Strip subsystems are considering DCBs.

One suggestion is a DCB per quadrant or half-plane with 4 or 8 output links per DCB.

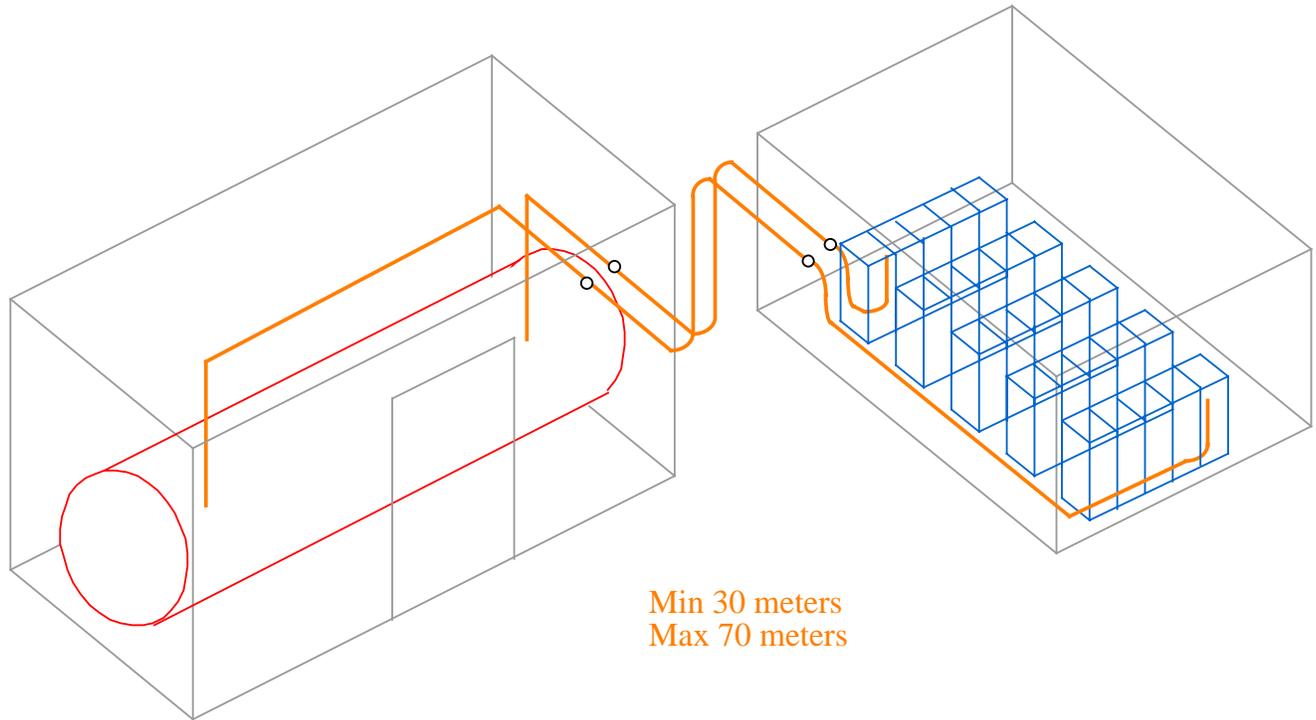
Multiple outputs allows use of less expensive multi-channel optical drivers.

Reduces optical links by factor of > 2 .

Same optical links for all subsystems (simplifies L1 Buffer).

Can RICH, Straws and Muon subsystems use a higher density DCB?

Optical Links



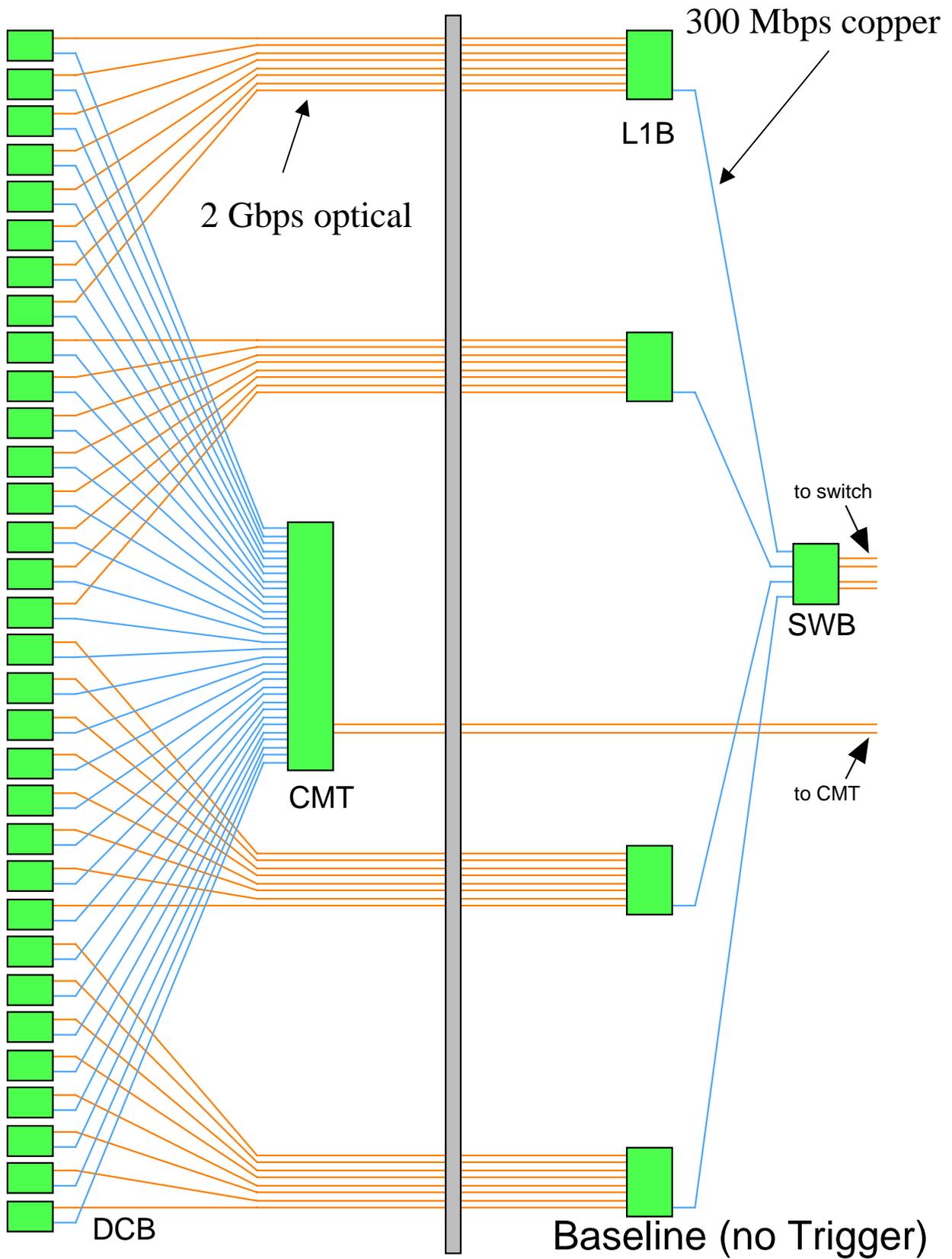
Baseline design has ~4400 optical links (mixture of 1 and 2 Gbps).

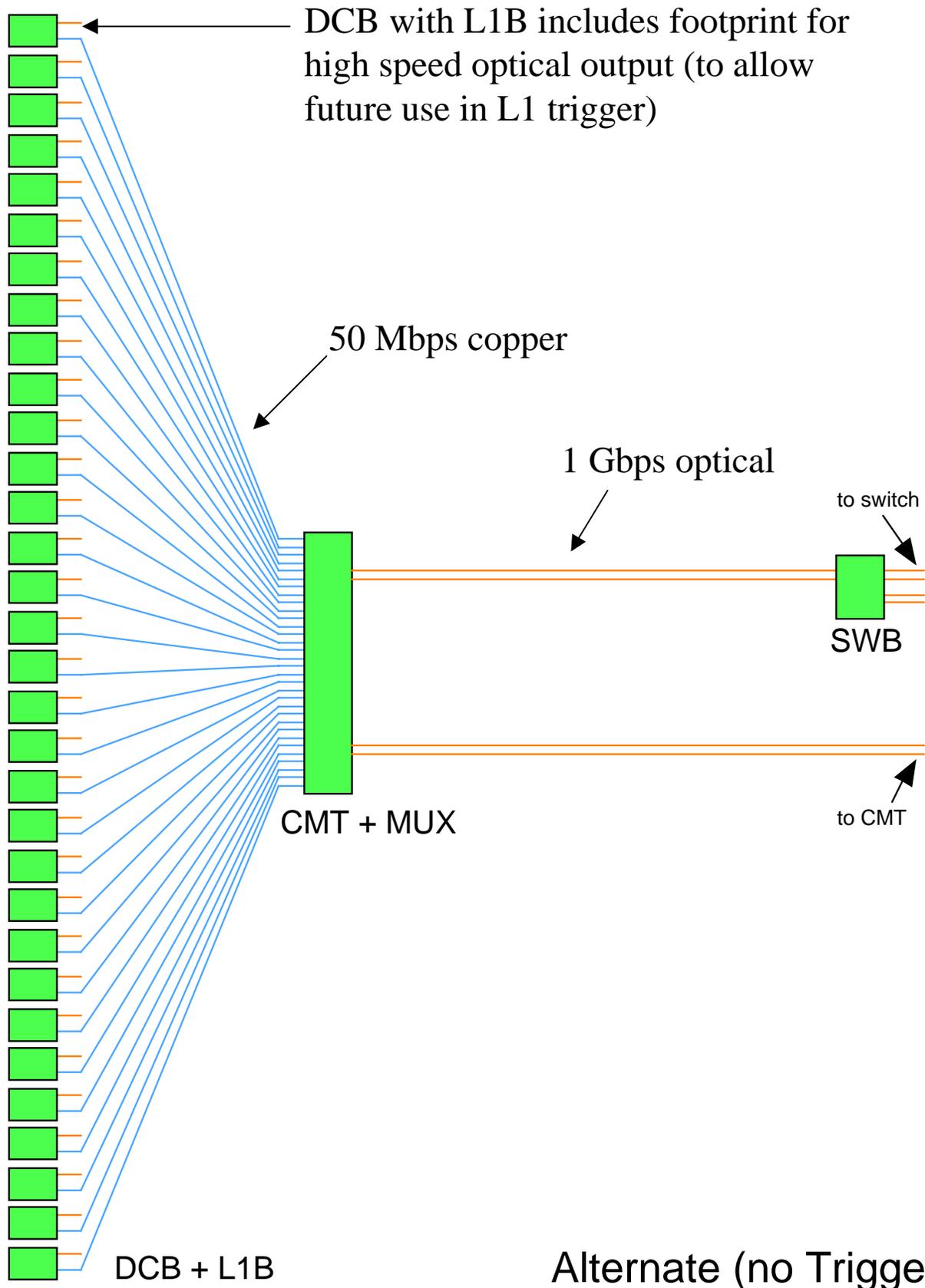
Average distance from detector to Counting Room is 50 meters...too far for copper at 1 Gbps.

Optical links are same price as copper at a distance of 50 meters.

Optical links provide isolation.

Common question - for subsystems not involved in the L1 Trigger, why is all of the data transmitted to the Counting Room?





Alternate Design

(move L1 Buffers to DCBs)

No problem with space or reliability -

Two DRAM chips replace one optical transmitter (same space).

MTTF of two DRAM chips = one VCSEL (same reliability).

BUT

What is DRAM SEU rate in DCB radiation environment?

Is this a problem for SRAM based FPGAs also?

Alternate Design

Expected error rate due to data links @ 10^{-15}
BER per link..... 400/day.

Expected error rate due to DRAM SEU
(cosmic rays) at Counting Room.... 25/day.

Moving L1 Buffers to DCBs

1) reduces data link BER by half

=> 200 fewer errors/day.

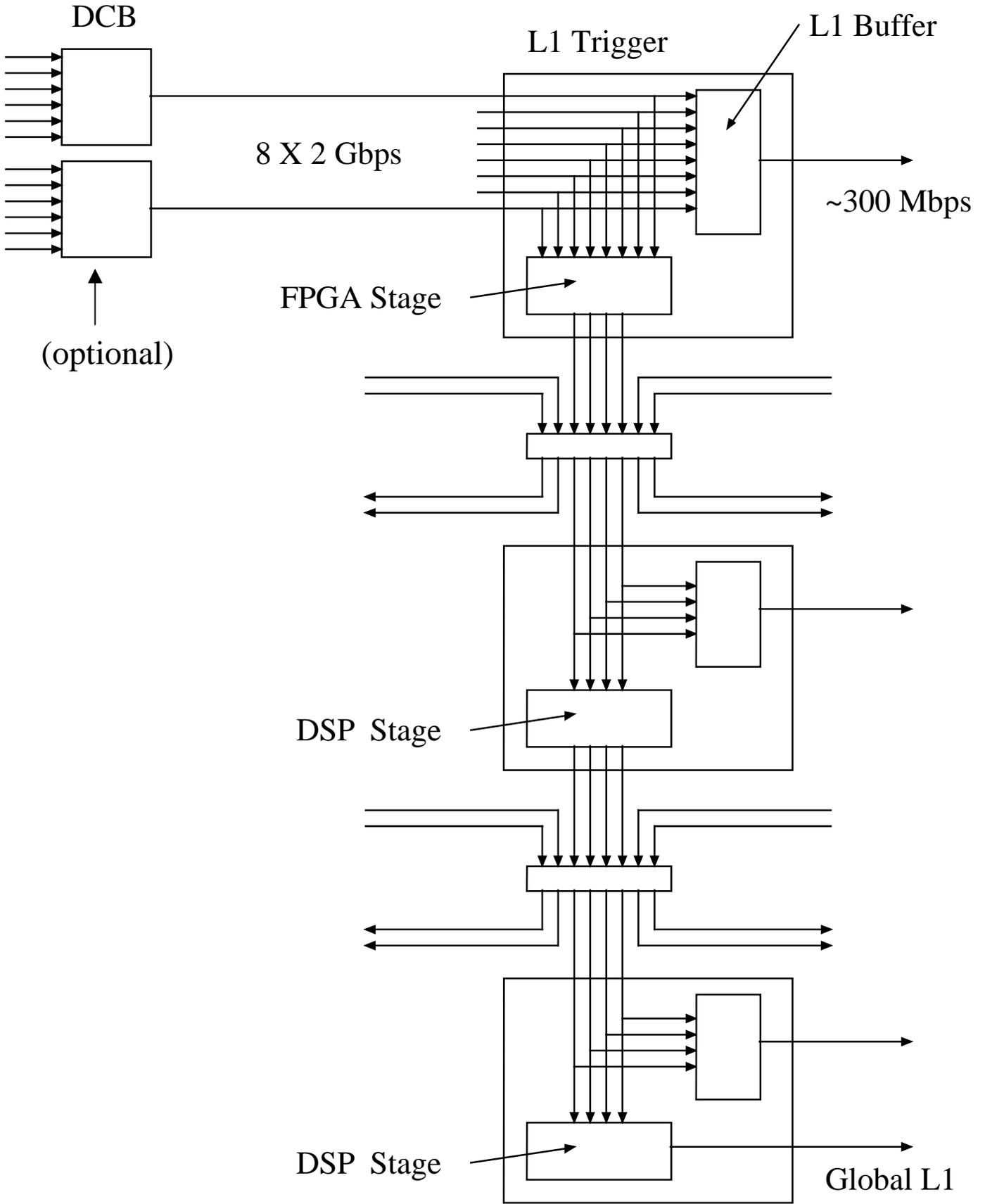
2) increases DRAM SEU rate by ?

=> ? more errors/day without ECC

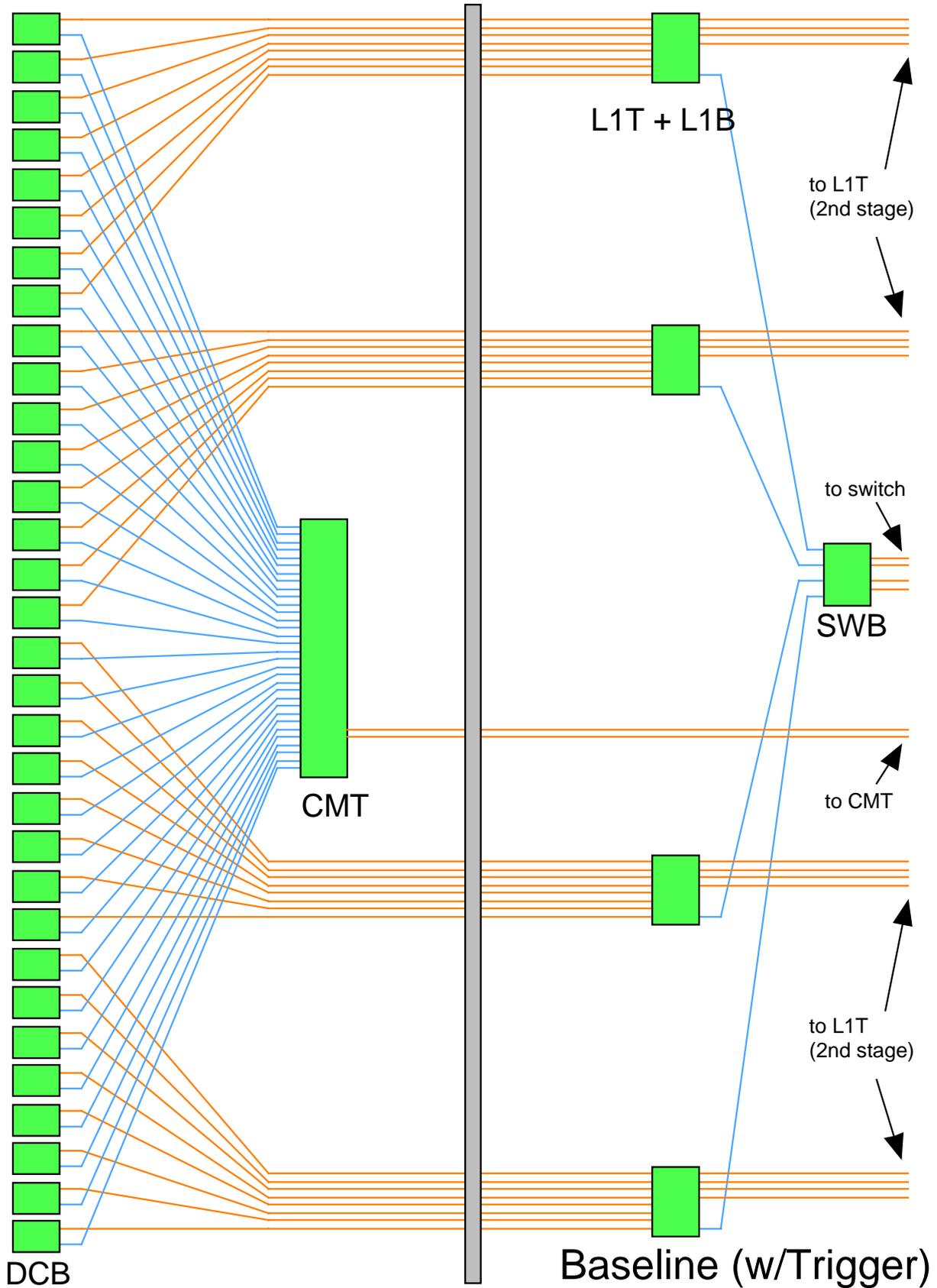
=> ? more errors/day with ECC

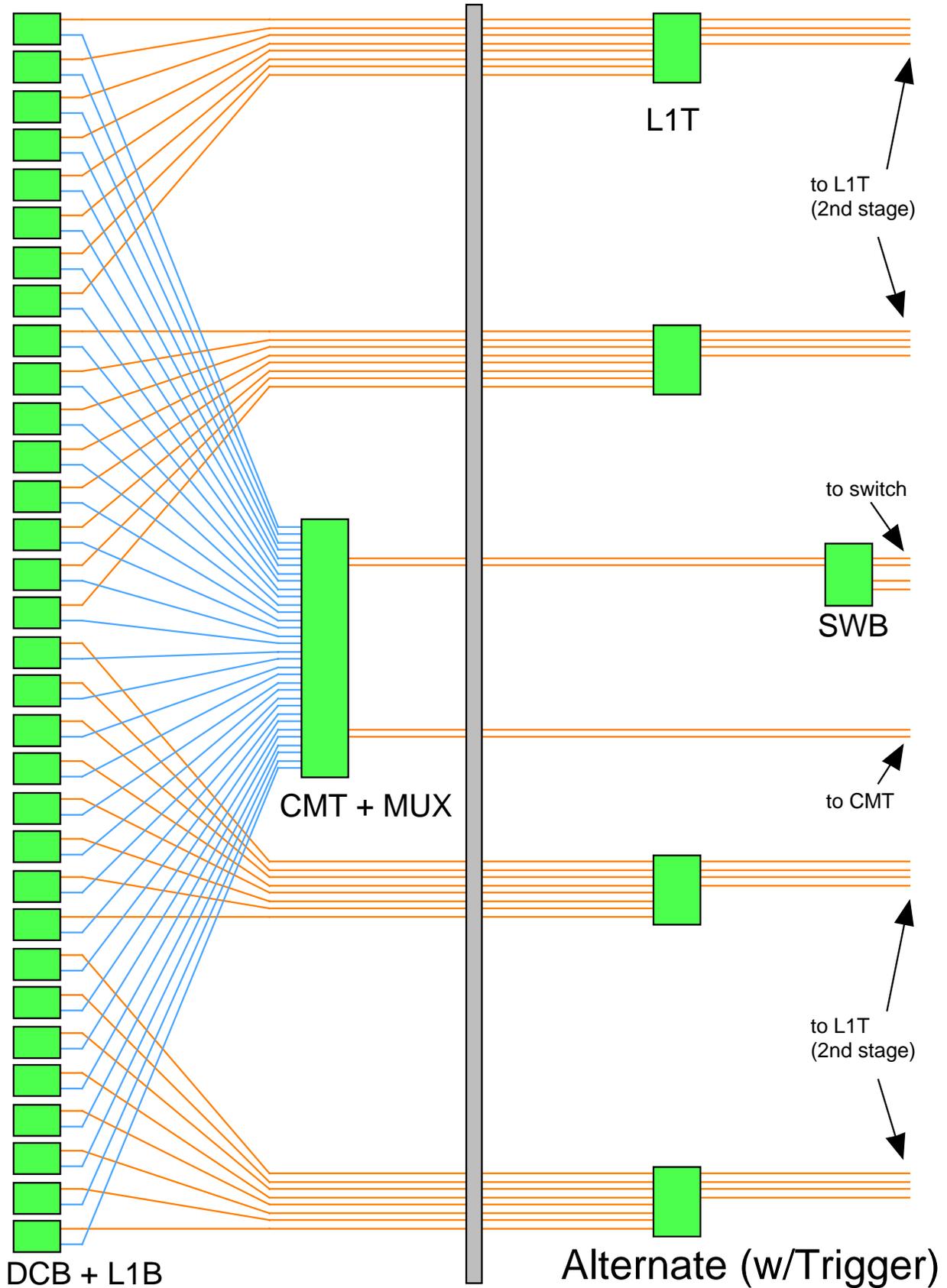
cost of 2000 data links.... ~\$300K

cost of ECC memory/logic.... ~\$50K

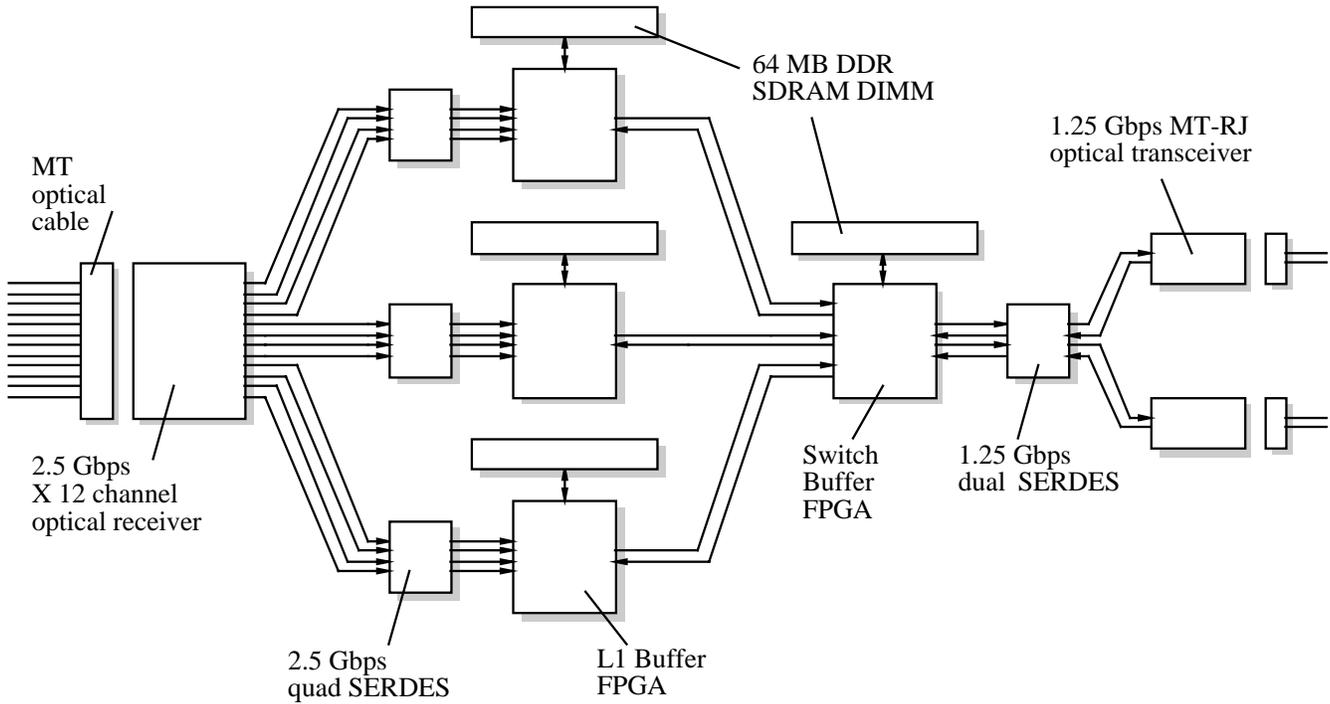


L1 Trigger (interface to DCBs and L1 Buffers)





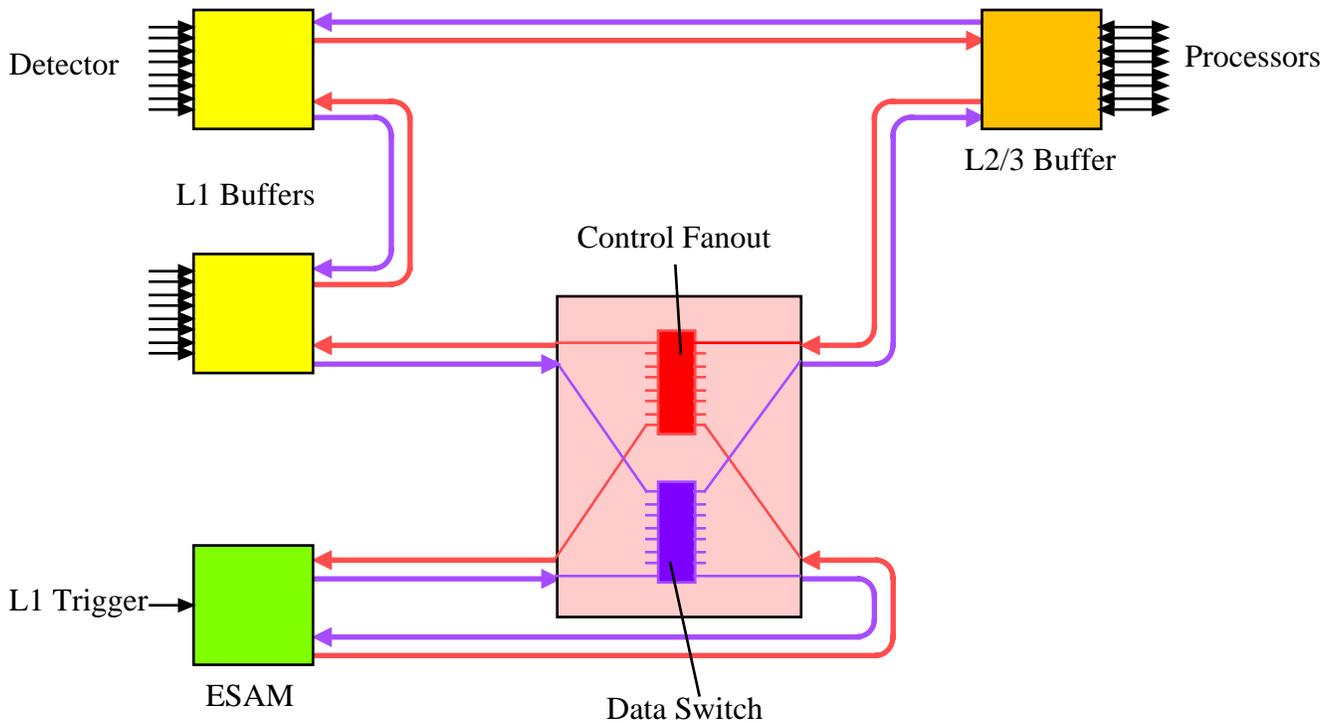
Baseline Level 1 Buffer (L1B)



Possible changes -

- 1) 8 input links instead of 12
- 2) split L1B and Switch Buffer functions
(to allow repositioning of L1B to DCB and/or Trigger modules)

Buffer Ring Architecture

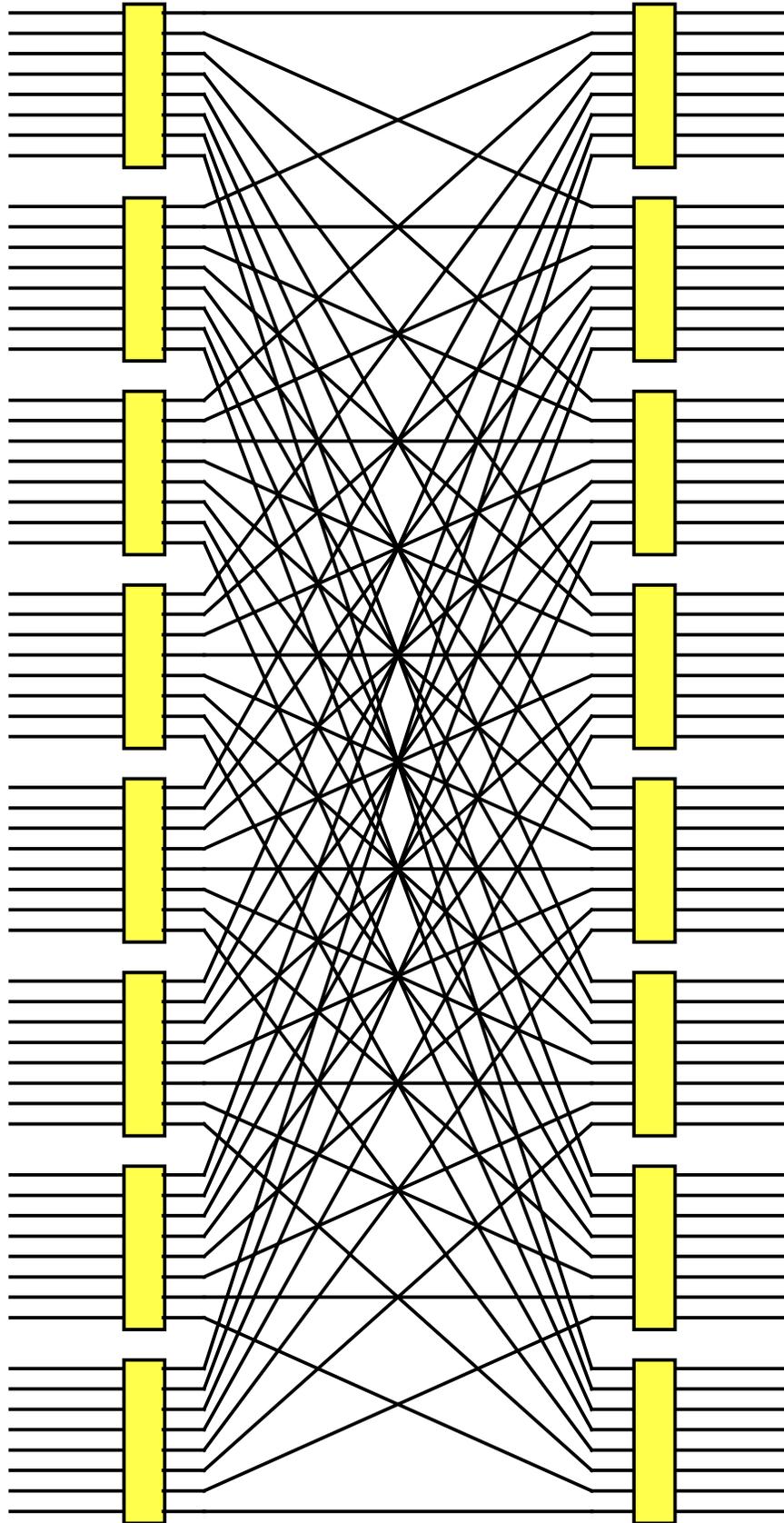


Multiple L1 Buffers per ring allows rate balancing based on input rate and L2 data request rate.

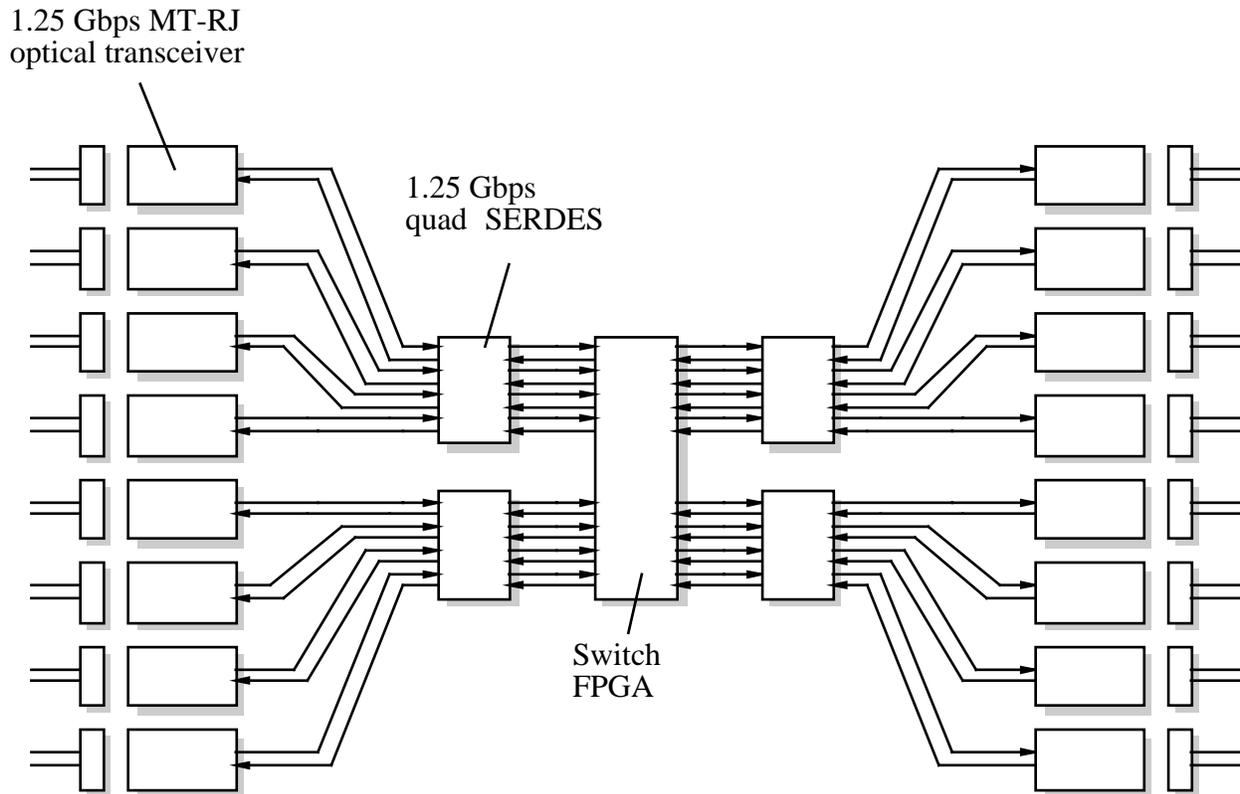
Dual counter-rotating rings for data and control.

Control path is 1:N broadcast. Data path is N:N crossbar.

Switch Expansion



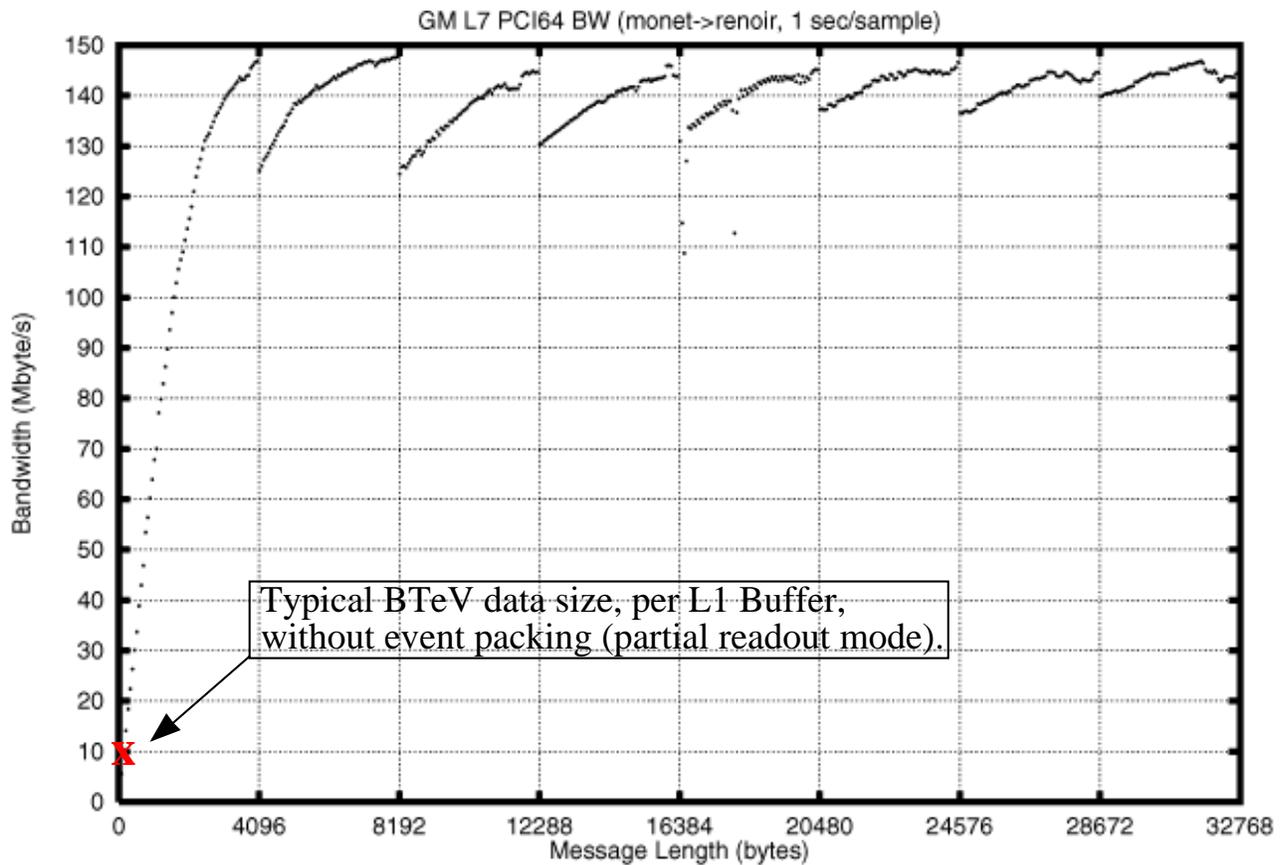
Baseline Switch Module



Possible changes -

- 1) Copper I/O instead of optical (optical not necessary)

Why Not a Commercial Switch?

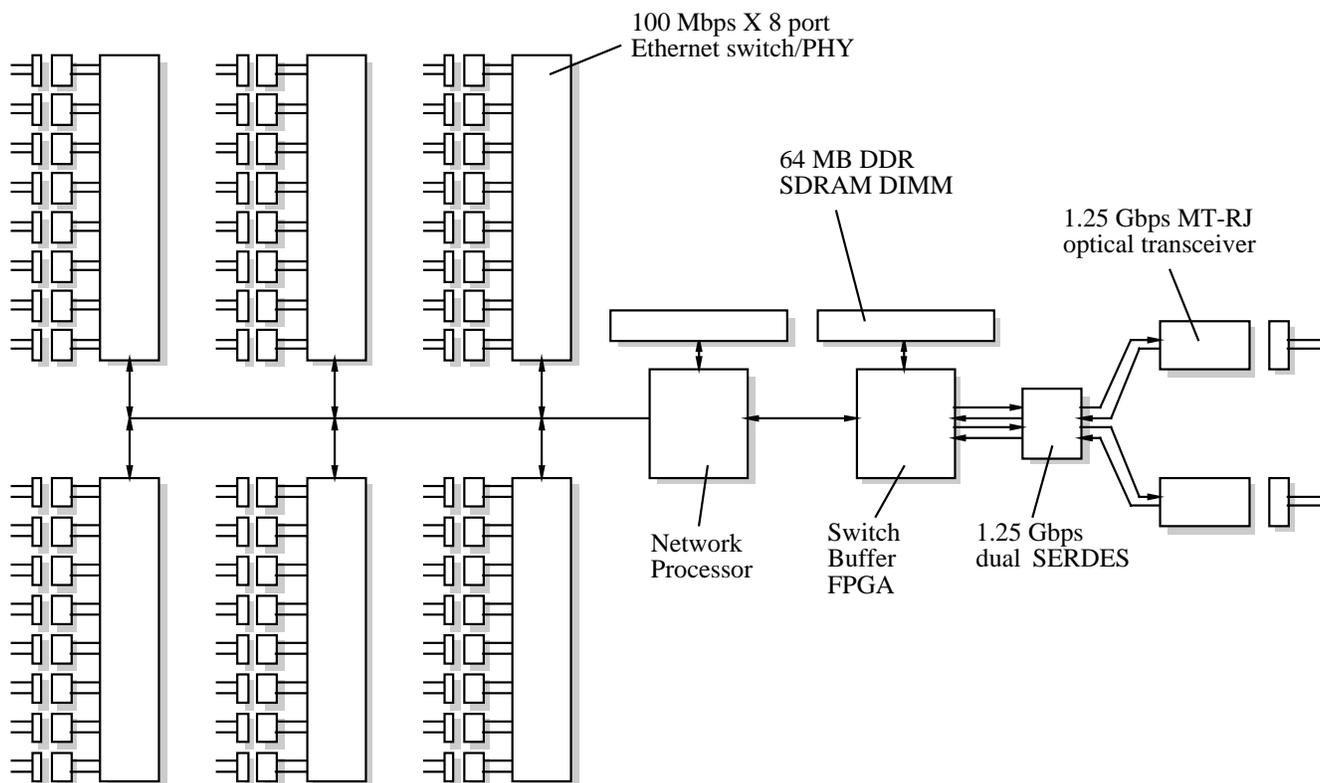


Myrinet Bandwidth

Commercial switches are optimized for packets of 2KB or larger. Current BTeV proposal is for selective L2 readout (average packet size = 200 Bytes).

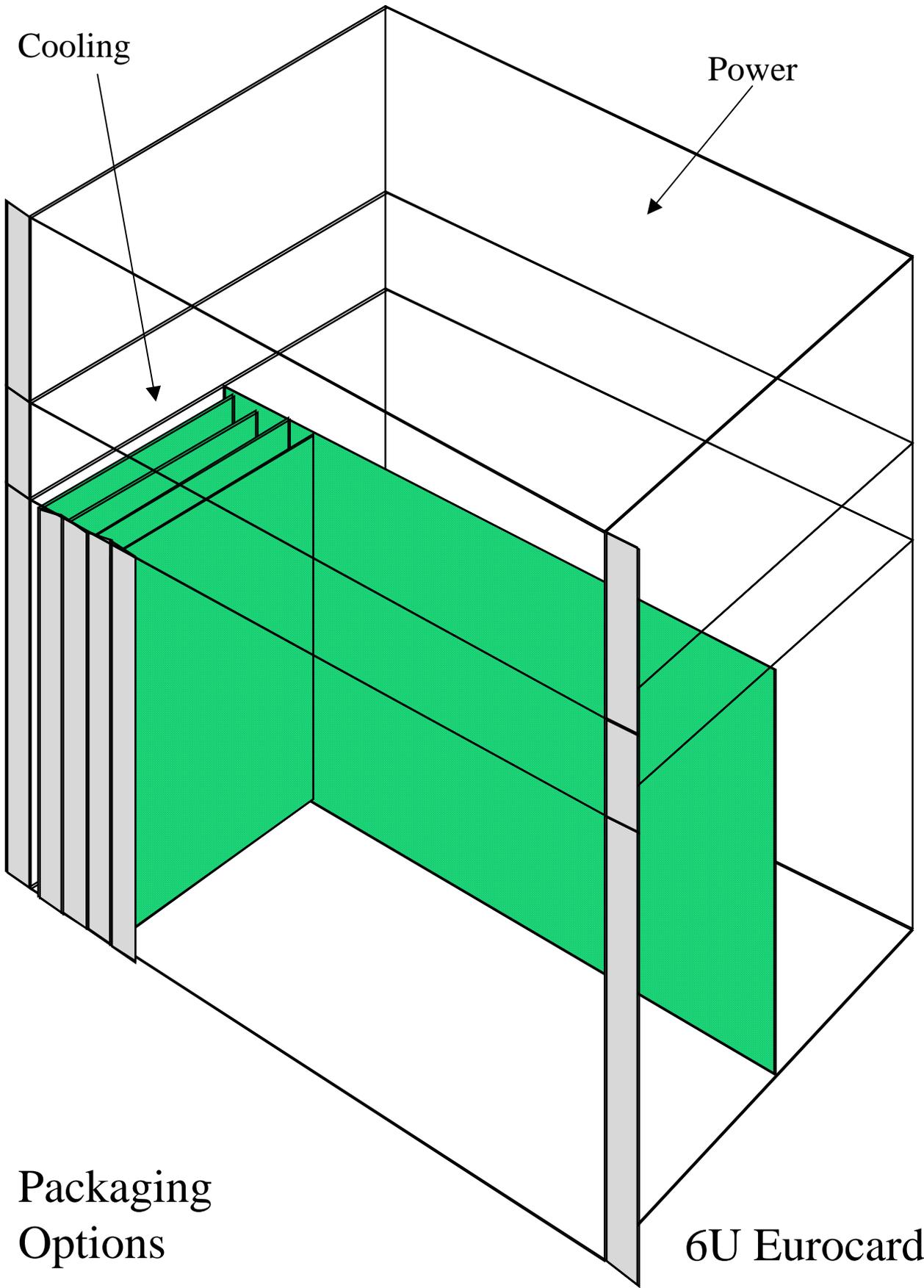
Cost of a switching network is in the network adapters (L1B), not in the switch. The switch design is trivial.

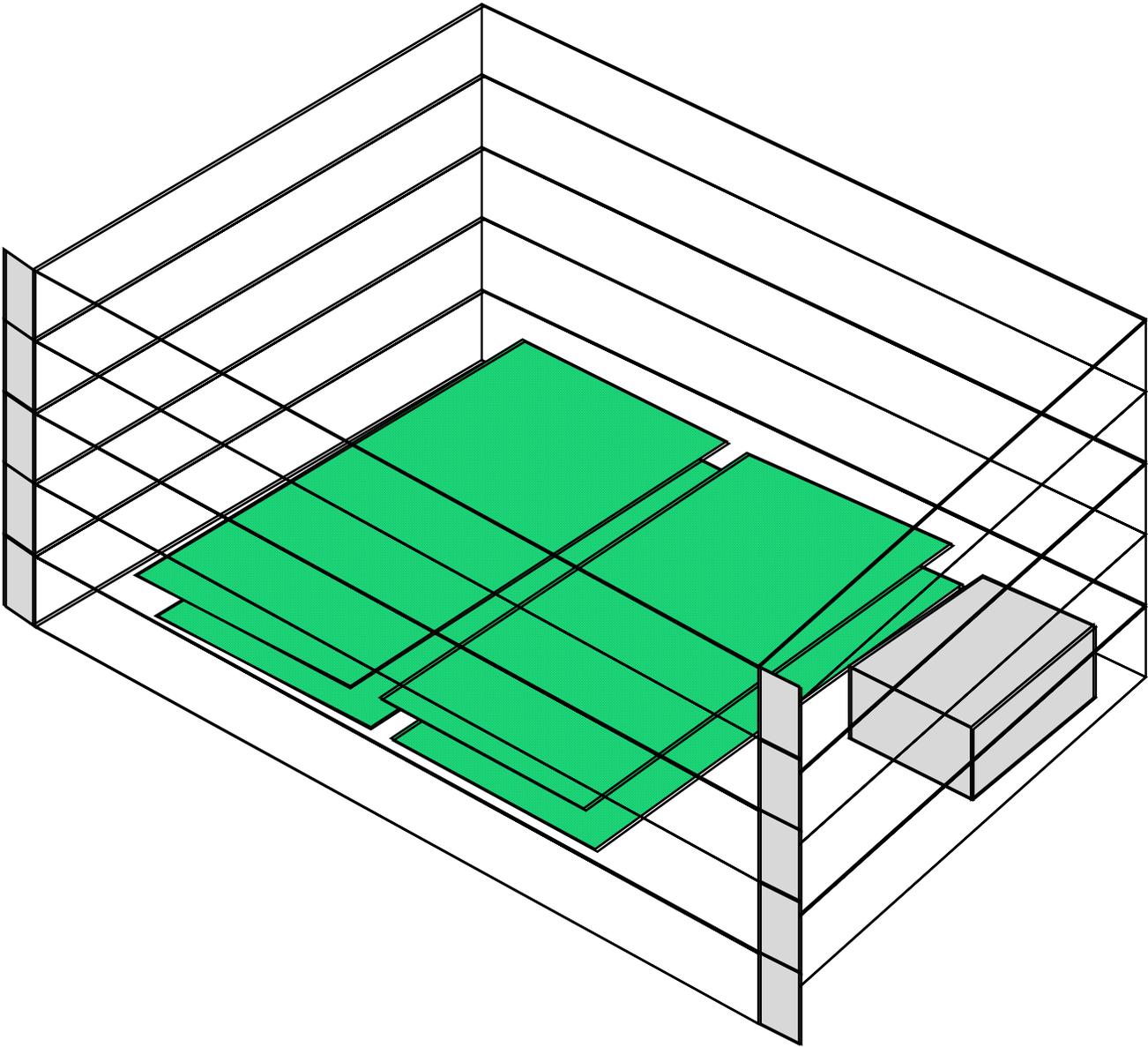
Baseline L2/3 Buffer



Possible changes -

- 1) direct DMA interface instead of Ethernet
- 2) separate processor interface from Switch Buffer to allow common L1 and L2 Switch Buffer.





Packaging
Options

1U rackmount with
integrated power and
cooling

Conclusion

Several simplifications and cost reductions are still possible in the current baseline design.

Questions we would like to focus on in this workshop;

Can FEB to DCB links be serialized at higher rates?

Does this cause a problem with noise or cost?

Can existing DCB designs be merged?

Should Pixel & Strip detectors add DCBs to allow common data link and L1B designs?

Does the detector environment allow the use of DRAM (or SRAM) in DCBs?

Not discussed...

Control, Monitoring and Timing (CM/T), Diagnostics,
Slow Controls