

Towards the baseline design review

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The electronics team:

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Outline:

- Goals
- Implementation
- What we need from Fermilab

Our goals

- Single photon detector element to determine that all the elements involved work well together:
 - 163 channel HPD
 - HPD high voltage
 - Front end chips being designed
 - Digital interface in front end hybrids and prototype data combiner board

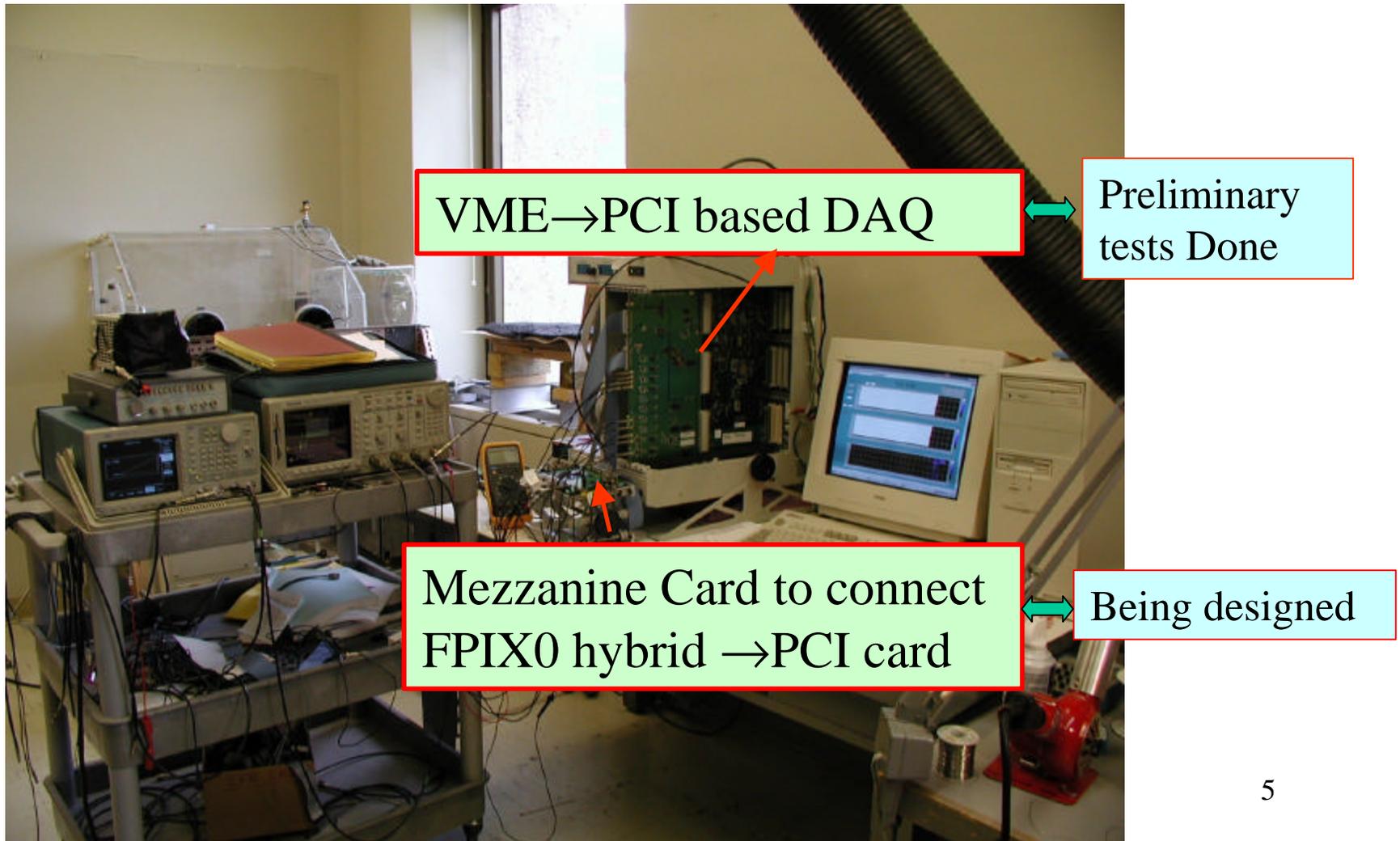
The electronics needs

- We need to develop a test stand capable of performing the required measurements to assess whether the system that we propose to implement satisfies our needs, including:
 - Data acquisition system capable of 2-way communication with the front end electronics
 - Efficient software to perform the planned tests

The strategy

- Use the pixel PCI based test stand as a starting point, capitalizing on our previous experience with FPIX0-FPIX1 electronics
- Translate this experience into a similar test stand optimized for VA-BTeV initialization and readout

Pixel Readout Test Setup at Syracuse



What we need NOW

- More information on the software included in this PCI board.
 - In particular the code residing in ALTERA chip
 - Protocol to communicate with on board elements (memory...)
 - Design architecture and optimal way to integrate our specific subroutines in the overall software structure
 - Implementation of code changes (JAM player, other??)
 - Labview routines and documentation

What we will need in a couple of months (hardware)

- 1 additional PCI board to be used in the BTeV-RICH test stand set-up (from Fermilab)
- 1 new mezzanine card for this application (we will do that)

Needs to finalize the tests

- A firmer definition of the overall back-end implementation (location, segmentation) so we can do a realistic check of the quality of:
 - the power supply distribution,
 - High Voltage effects,
 - noise environment,
 - grounding scheme